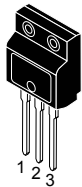
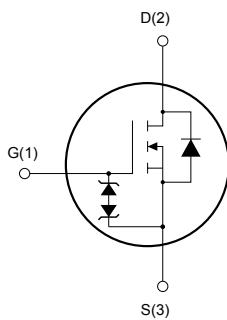


## N-channel 600 V, 0.550 $\Omega$ typ., 7.5 A MDmesh™ M2 EP Power MOSFET in an I<sup>2</sup>PAKFP package


 I<sup>2</sup>PAKFP (TO-281)


AM15572v1\_no\_tab

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STFI11N60M2-EP	600 V	0.595 $\Omega$	7.5 A

- Extremely low gate charge
- Excellent output capacitance (C<sub>OSS</sub>) profile
- Very low turn-off switching losses
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 enhanced performance (EP) technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance, optimized switching characteristics with very low turn-off switching losses, rendering it suitable for the most demanding very high frequency converters.

#### Product status

STFI11N60M2-EP

#### Product summary

<b>Order code</b>	STFI11N60M2-EP
<b>Marking</b>	11N60M2EP
<b>Package</b>	I <sup>2</sup> PAKFP (TO-281)
<b>Packing</b>	Tube

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	7.5	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	4.7	A
$I_{DM}^{(1)}$	Drain current (pulsed)	30	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	25	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t = 1\text{ s}$ , $T_C = 25\text{ }^\circ\text{C}$ )	2.5	kV
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 7.5\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS\ peak} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$
3.  $V_{DS} \leq 480\text{ V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	5	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	$^\circ\text{C}/\text{W}$

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	2.4	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	115	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}, T_C = 125\text{ °C}^{(1)}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 3.75\text{ A}$		0.550	0.595	$\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	390	-	pF
$C_{oss}$	Output capacitance		-	22	-	pF
$C_{rss}$	Reverse transfer capacitance		-	0.7	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}, V_{GS} = 0\text{ V}$	-	49	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0\text{ A}$	-	9	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 7.5\text{ A}, V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	12.4	-	nC
$Q_{gs}$	Gate-source charge		-	2.1	-	nC
$Q_{gd}$	Gate-drain charge		-	6	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching energy**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{(off)}$	Turn-off energy (from 90% $V_{GS}$ to 0% $I_D$ )	$V_{DD} = 400\text{ V}, I_D = 1\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$	-	2.5	-	$\mu\text{J}$
		$V_{DD} = 400\text{ V}, I_D = 3\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$	-	9	-	$\mu\text{J}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 3.75\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	9	-	ns
$t_r$	Rise time		-	5.5	-	ns
$t_{d(off)}$	Turn-off-delay time		-	26	-	ns
$t_f$	Fall time		-	8	-	ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		7.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		30	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 7.5\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 7.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	192		ns
$Q_{rr}$	Reverse recovery charge		-	1.32		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	$I_{SD} = 7.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	13.8		A
$t_{rr}$	Reverse recovery time		-	262		ns
$Q_{rr}$	Reverse recovery charge		-	1.74		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	13.3		A

1. Pulse width is limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics curves

Figure 1. Safe operating area

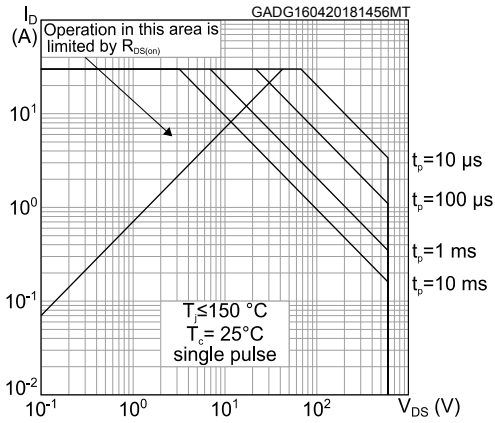


Figure 2. Thermal impedance

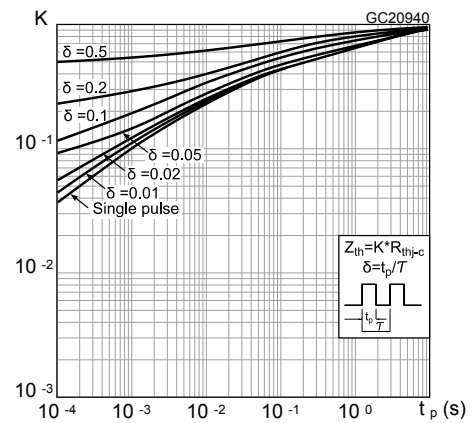


Figure 3. Output characteristics

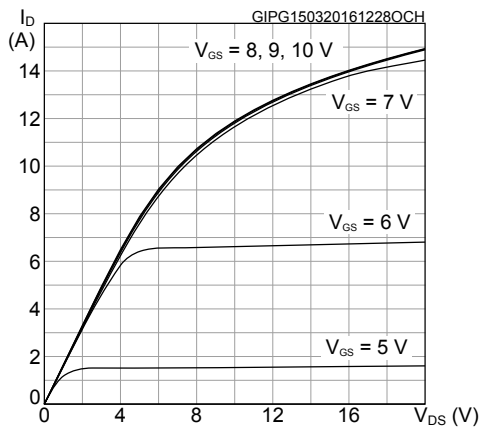


Figure 4. Transfer characteristics

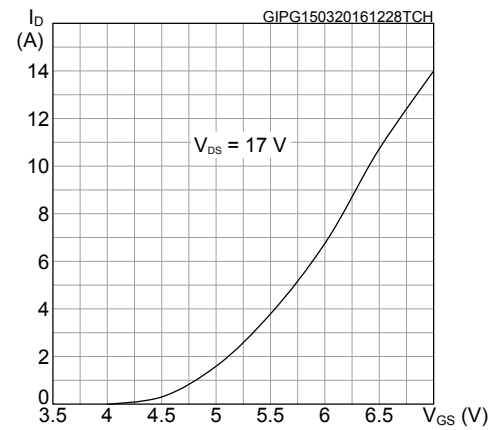


Figure 5. Gate charge vs gate-source voltage

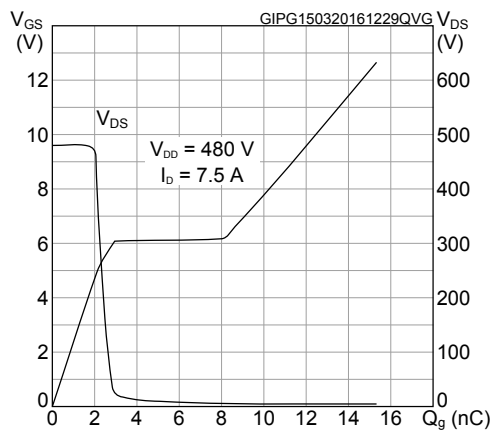


Figure 6. Static drain-source on-resistance

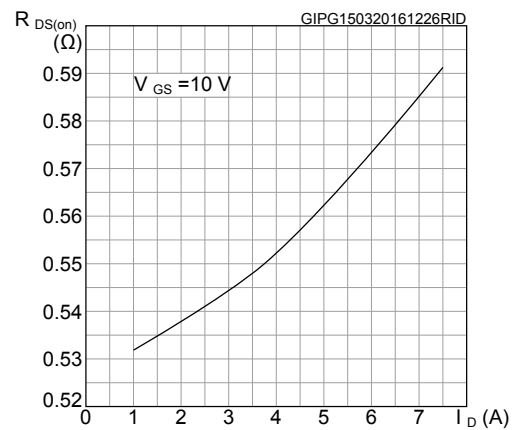


Figure 7. Capacitance variations

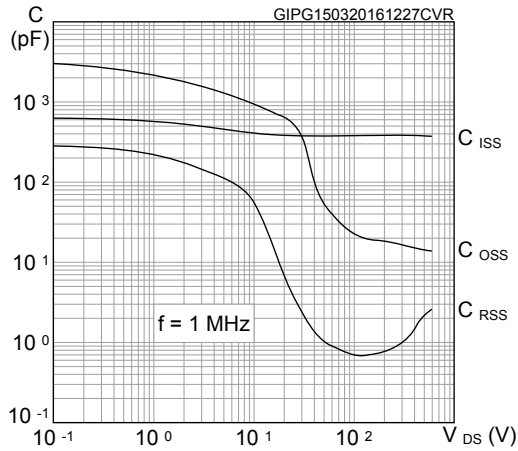


Figure 8. Turn-off switching energy vs drain current

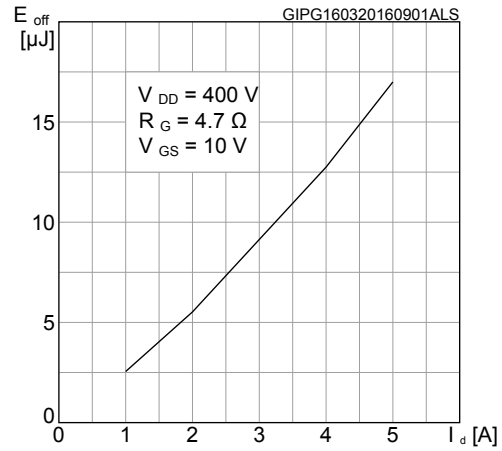


Figure 9. Normalized gate threshold voltage vs temperature

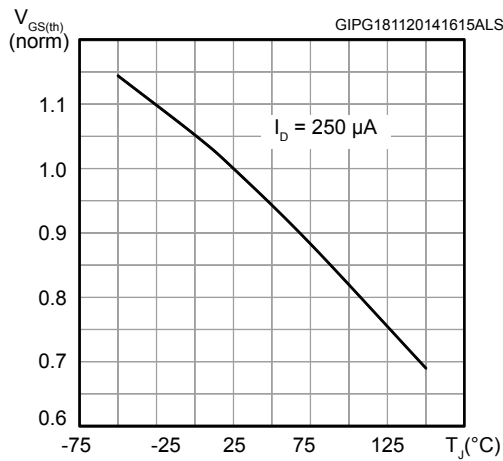


Figure 10. Normalized on-resistance vs temperature

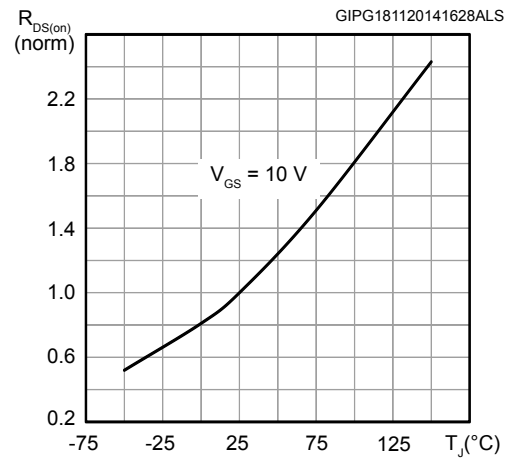


Figure 11. Normalized  $V_{(BR)DSS}$  vs temperature

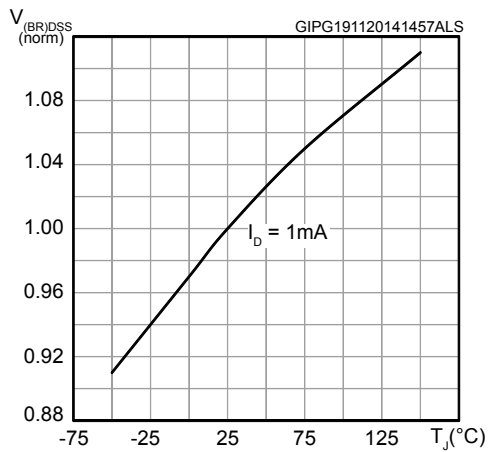
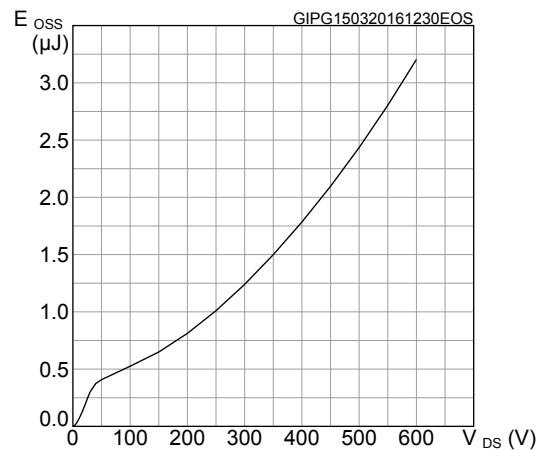
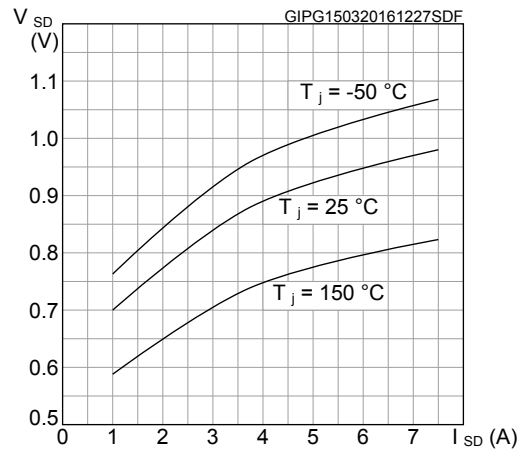


Figure 12. Output capacitance stored energy



**Figure 13. Source-drain diode forward characteristics**



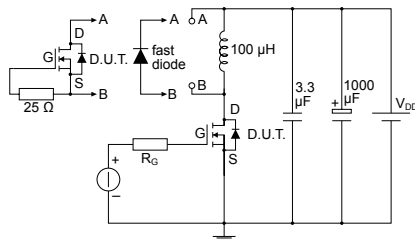
### 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**

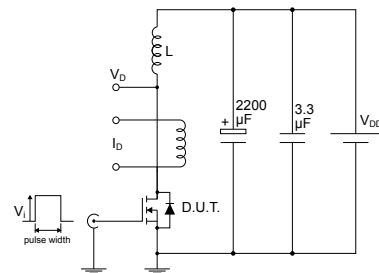

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**Figure 15. Test circuit for gate charge behavior**


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**Figure 16. Test circuit for inductive load switching and diode recovery times**


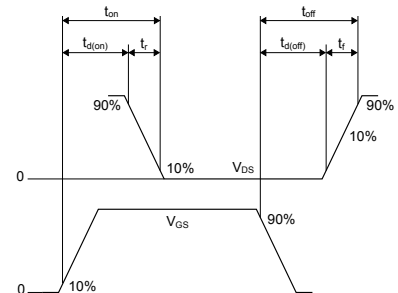
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**Figure 17. Unclamped inductive load test circuit**


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**Figure 18. Unclamped inductive waveform**


AM01472v1

**Figure 19. Switching time waveform**


AM01473v1

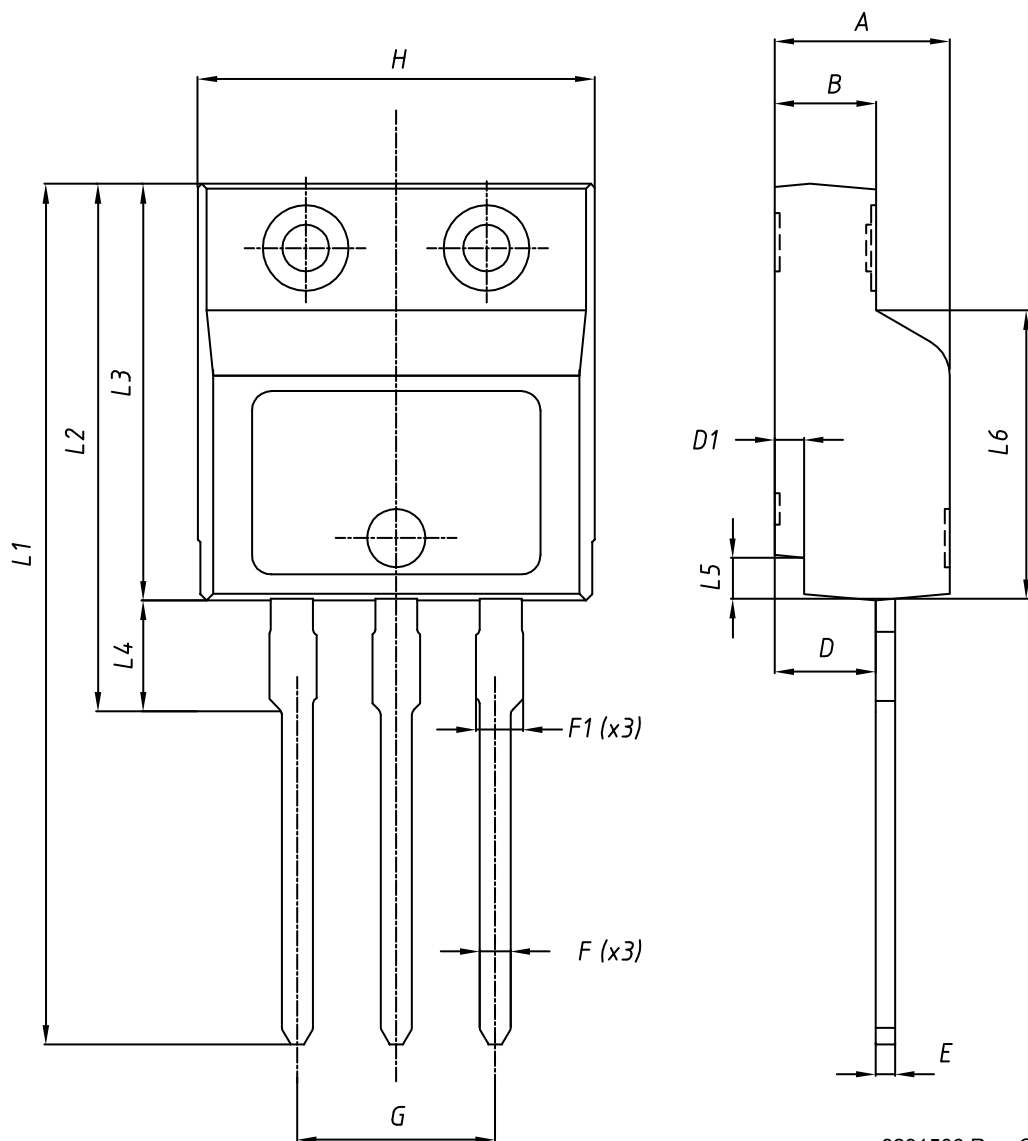


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 I<sup>2</sup>PAKFP (TO-281) package information

Figure 20. I<sup>2</sup>PAKFP (TO-281) package outline



8291506 Rev. C

**Table 9. I<sup>2</sup>PAKFP (TO-281) mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.50	7.60	7.70

## Revision history

**Table 10. Document revision history**

Date	Revision	Changes
12-Apr-2016	1	First release.
07-Oct-2016	2	Document status changed from preliminary to production data.
14-May-2018	3	Removed document maturity status from cover page. Updated <a href="#">Section 1 Electrical ratings</a> , <a href="#">Section 2 Electrical characteristics</a> and <a href="#">Section 2.1 Electrical characteristics curves</a> . Minor text changes

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