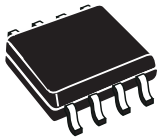
L6395

High voltage high and low-side driver

Datasheet - production data



SO-8

Features

- High voltage rail up to 600 V
- dV/dt immunity ± 50 V/ns in full temperature range
- Driver current capability:
  - 290 mA source
  - 430 mA sink
- Switching times 75/35 ns rise/fall with 1 nF load
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Integrated bootstrap diode
- Compact and simplified layout
- Bill of material reduction
- Effective fault protection
- Flexible, easy and fast design

Applications

- Motor driver for home appliances
- Factory automation
- Industrial drives and fans

Description

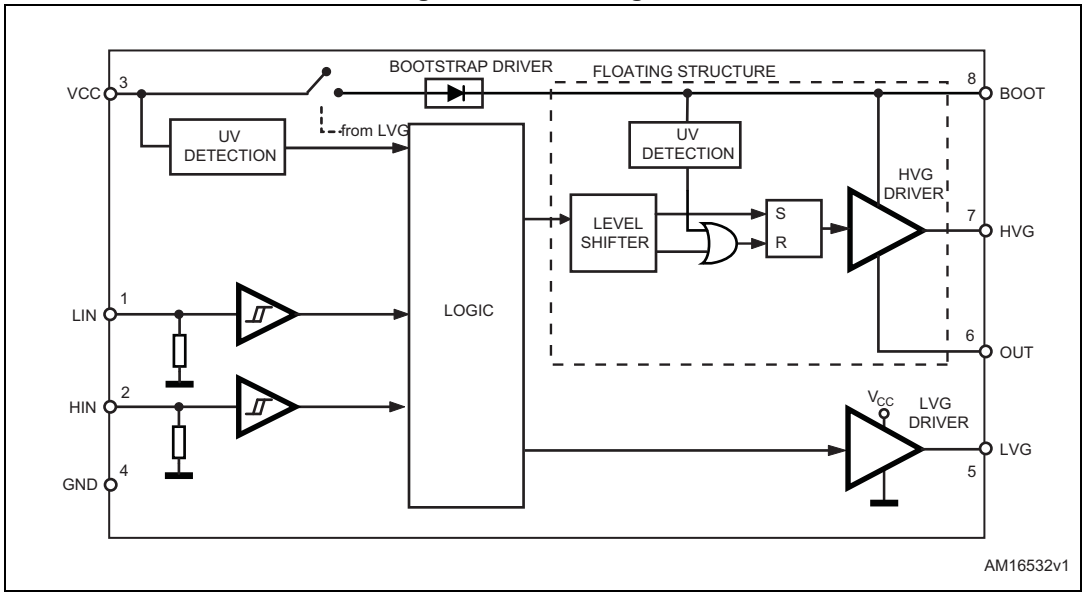
The L6395 is a high voltage device manufactured with the BCD™ “offline” technology. It is a single-chip high and low-side gate driver for N-channel power MOSFETs or IGBTs.

The high-side (floating) section is designed to stand a voltage rail up to 600 V. The logic inputs are CMOS/TTL compatible down to 3.3 V for the easy interfacing microcontroller/DSP.

Contents

1 Block diagram

Figure 1. Block diagram



2 Pin connection

Figure 2. Pin connection

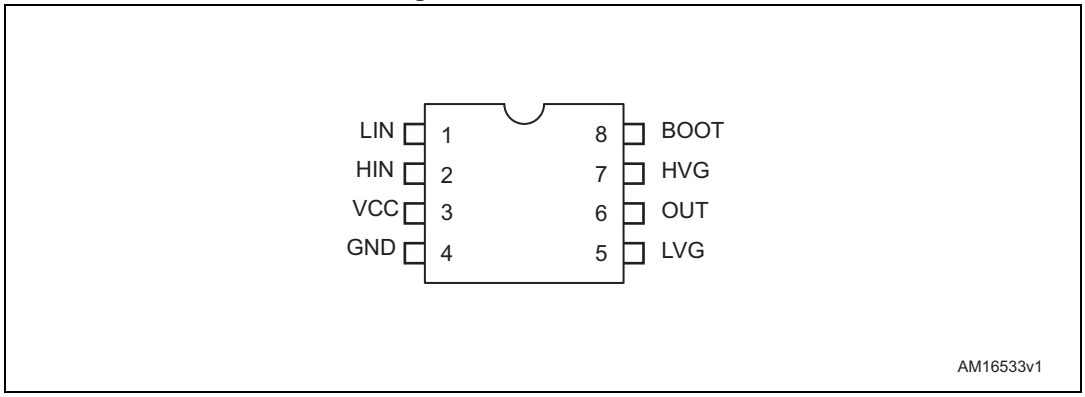


Table 1. Pin description

Pin	Pin name	Type	Function
1	LIN	I	Low-side driver logic input (active high)
2	HIN	I	High-side driver logic input (active high)
3	VCC	P	Lower section supply voltage
4	GND	P	Ground
5	LVG(1)	O	Low-side driver output
6	OUT	P	High-side (floating) common voltage
7	HVG(1)	O	High-side driver output
8	BOOT	P	Bootstrapped supply voltage

1. The circuit guarantees less than 1 V on the LVG and HVG pins (at I_{sink} = 10 mA), with V_{CC} > 3 V. In this manner, the “bleeder”, resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low, is omitted.

3 Truth table

Table 2. Truth table

Input		Output	
LIN	HIN	LVG	HVG
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H

4 Electrical data

4.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{CC}	Supply voltage	- 0.3	21	V
V_{OUT}	Output voltage	V_{BOOT} - 21	V_{BOOT} + 0.3	V
V_{BOOT}	Bootstrap voltage	- 0.3	620	V
V_{hvg}	High-side gate output voltage	V_{OUT} - 0.3	V_{BOOT} + 0.3	V
V_{lvg}	Low-side gate output voltage	- 0.3	V_{CC} + 0.3	V
V_i	Logic input voltage	- 0.3	15	V
dV_{OUT}/dt	Allowed output slew rate		50	V/ns
P_{tot}	Total power dissipation (T_A = 25 °C)		800	mW
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	-50	150	°C
ESD	Human body model	2		kV

4.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	SO-8	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	150	°C/W

4.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Value		Unit
				Min.	Max.	
V_{CC}	3	Supply voltage		10	20	V
V_{BO}(1)	8 - 6	Floating supply voltage		9.4	20	V
V_{OUT}	6	Output voltage(1)		-11(2)	580	V
f_{SW}		Switching frequency	HVG, LVG load C_L = 1 nF		800	kHz
T_J		Junction temperature		-40	125	°C

1. $V_{BO} = V_{BOOT} - V_{OUT}$.
2. LVG off. V_{CC} = 10 V. Logic is operational if V_{BOOT} > 5 V.

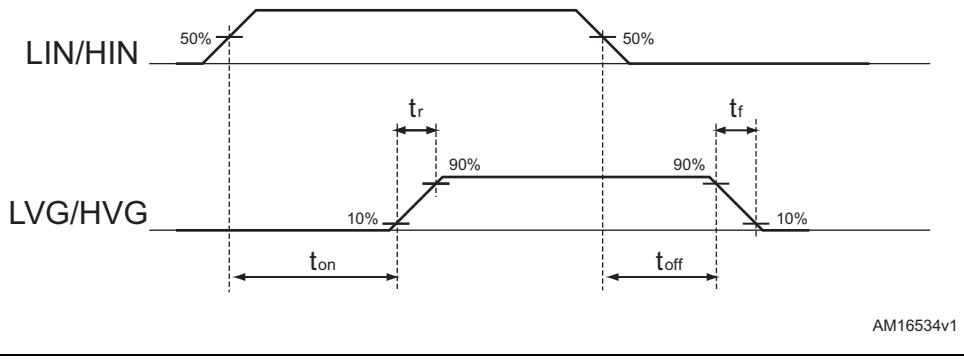
5 Electrical characteristics

5.1 AC operation

Table 6. AC operation electrical characteristics (V_{CC} = 15 V; T_j = +25 °C)

Symbol	Pin	Parameter	Test condition	Value			Unit
				Min.	Typ.	Max.	
t_{on}	1,2 vs. 5, 7	High/low-side driver turn-on propagation delay	V_{OUT} = 0 V V_{BOOT} = V_{CC} C_L = 1 nF V_{IN} = 0 to 3.3 V See *Figure 3*	50	125	200	ns
t_{off}	1,2 vs. 5, 7	High/low-side driver turn-off propagation delay	V_{OUT} = 0 V V_{BOOT} = V_{CC} C_L = 1 nF V_{IN} = 3.3 V to 0 See *Figure 3*	50	125	200	ns
t_r	5, 7	Rise time	C_L = 1 nF		75	120	ns
t_f	5, 7	Fall time	C_L = 1 nF		35	70	ns

Figure 3. Timing



5.2 DC operation

(V_{cc} = 15 V; T_j = +25 °C)

Table 7. DC operation electrical characteristics

Symbol	Pin	Parameter	Test condition	Value			Unit
				Min.	Typ.	Max.	
Low supply voltage section							
V_{CC_hys}	3	V_{CC} UV hysteresis		0.6	0.7	0.8	V
V_{CC_thON}	3	V_{CC} UV turn ON threshold		9	9.5	10	V
V_{CC_thOFF}	3	V_{CC} UV turn OFF threshold		8.3	8.8	9.3	V
I_{qccu}	3	Undervoltage quiescent supply current	V_{CC} = 7 V LIN = 5V; HIN = GND;	40	90	150	µA
I_{qcc}	3	Quiescent current	V_{CC} = 15 V LIN = 5 V; HIN = GND;	100	220	350	µA
Bootstrapped supply voltage section(1)							
V_{BO_hys}	8	V_{BO} UV hysteresis		0.5	0.6	0.7	V
V_{BO_thON}	8	V_{BO} UV turn ON threshold		7.9	8.6	9.4	V
V_{BO_thOFF}	8	V_{BO} UV turn OFF threshold		7.3	8	8.7	V
I_{QBOU}	8	Undervoltage V_{BO} quiescent current	V_{BO} = 7 V LIN = GND; HIN = 5 V	10	30	60	µA
I_{QBO}	8	V_{BO} quiescent current	V_{BO} = 15 V LIN = GND; HIN = 5 V;		190	220	µA
I_{LK}	8	High voltage leakage current	$V_{hvg} = V_{OUT} = V_{BOOT}$ = 600 V			10	µA
$R_{DS(on)}$		Bootstrap driver on-resistance(2)	LVG on		120		Ω
Driving buffer section							
I_{so}	5, 7	High/low-side source short-circuit current	$V_{IN} = V_{ih}$ (t_p < 10 µs)	200	290		mA
I_{si}	5, 7	High/low-side sink short-circuit current	$V_{IN} = V_{il}$ (t_p < 10 µs)	250	430		mA
Logic inputs							
V_{il}	1, 2	Low level logic threshold voltage		0.8		1.1	V
V_{ih}	1, 2	High level logic threshold voltage		1.9		2.25	V

Table 7. DC operation electrical characteristics (continued)

Symbol	Pin	Parameter	Test condition	Value			Unit
				Min.	Typ.	Max.	
I_{HINh}	2	HIN logic “1” input bias current	HIN = 15 V	10	40	100	µA
I_{HINl}	2	HIN logic “0” input bias current	HIN = 0 V			1	µA
I_{LINh}	1	LIN logic “1” input bias current	LIN = 15 V	10	40	100	µA
I_{LINl}	1	LIN logic “0” input bias current	LIN = 0 V			1	µA

1. $V_{BO} = V_{BOOT} - V_{OUT}$.
2. $R_{DS(on)}$ is tested in the following way: $R_{DS(on)} = [(V_{CC} - V_{BOOT1}) - (V_{CC} - V_{BOOT2})] / [I_1(V_{CC},V_{BOOT1}) - I_2(V_{CC},V_{BOOT2})]$ where I_1 is the pin 8 current when $V_{BOOT} = V_{BOOT1}$, I_2 when $V_{BOOT} = V_{BOOT2}$.

6 Typical application diagram

Figure 4. Application diagram

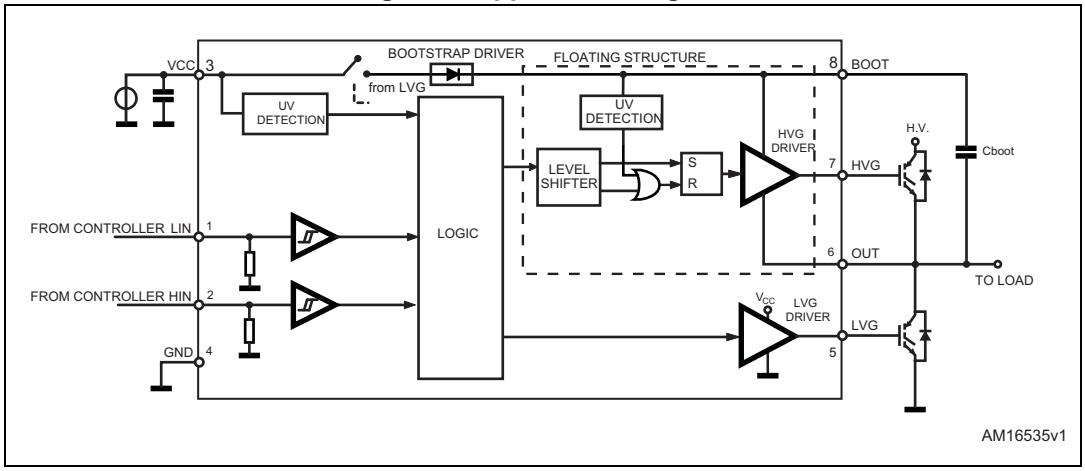
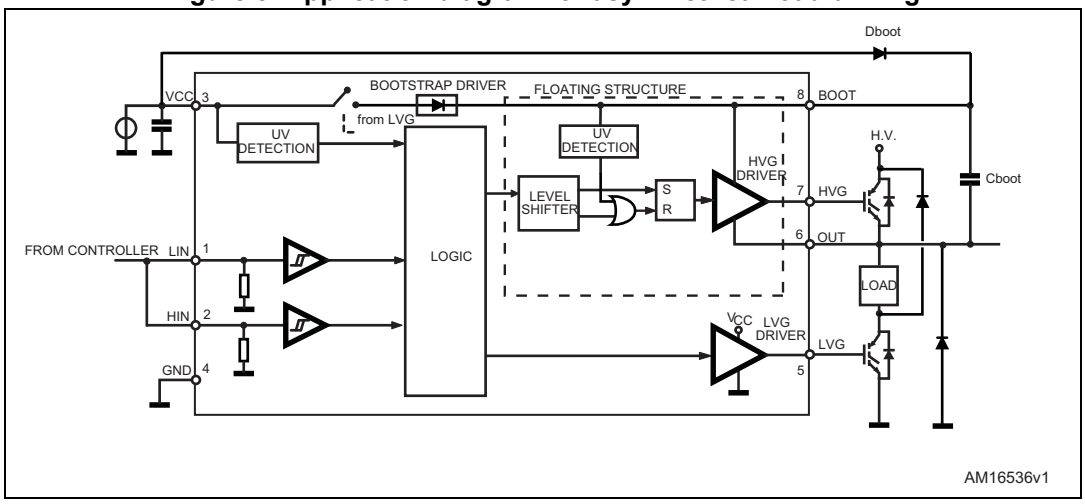


Figure 5. Application diagram for asymmetrical load driving



7 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished using a high voltage fast recovery diode (*Figure 6*). In the L6395 device a patented integrated structure replaces the external diode. It is implemented using a high voltage DMOS, driven synchronously with the low-side driver (LVG), with a diode in series, as shown in *Figure 7*. An internal charge pump provides the DMOS driving voltage.

C_{BOOT} selection and charging

To select the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss.

It must be:

Equation 2

$$C_{BOOT} \gg C_{EXT}$$

E.g.: if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop is 300 mV.

If HVG needs to be supplied for an extended period, the C_{BOOT} selection has to take into account also the leakage and quiescent losses.

E.g.: HVG steady state consumption is lower than 220 µA, so if HVG T_{ON} is 5 ms, C_{BOOT} must supply 1.1 µC to C_{EXT}. This charge on a 1 µF capacitor means a voltage drop of 1.1 V.

The internal bootstrap driver offers some important advantages: the external fast recovery diode can be avoided (it usually has a high leakage current).

This structure can work only if V_{OUT} is close to GND (or lower) and, at the same time, the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS $R_{DS(on)}$ (typical value: 120 Ω). At low switching frequency, this drop can be neglected but, operating at high switching frequency, it should be taken into account.

The following equation is useful to compute the drop on the bootstrap DMOS:

Equation 3

$$V_{drop} = I_{charge} \cdot R_{DS(on)} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} \cdot R_{DS(on)}$$

where Q_{gate} is the gate charge of the external power MOSFET, $R_{DS(on)}$ is the on-resistance of the bootstrap DMOS and T_{charge} is the charging time of the bootstrap capacitor.

For example: using a power MOSFET with a total gate charge of 30 nC, the drop on the bootstrap DMOS is about 1 V, if the T_{charge} is 5 µs.

Equation 4

$$V_{drop} = \frac{30_{nc}}{5_{\mu s}} \cdot 120\Omega \cong 0.7V$$

V_{drop} must be taken into account when the voltage drop on C_{BOOT} is calculated: whether this drop is too high, or the circuit topology does not allow a sufficient charging time, an external diode can be used.

Figure 6. Bootstrap driver with high voltage fast recovery diode

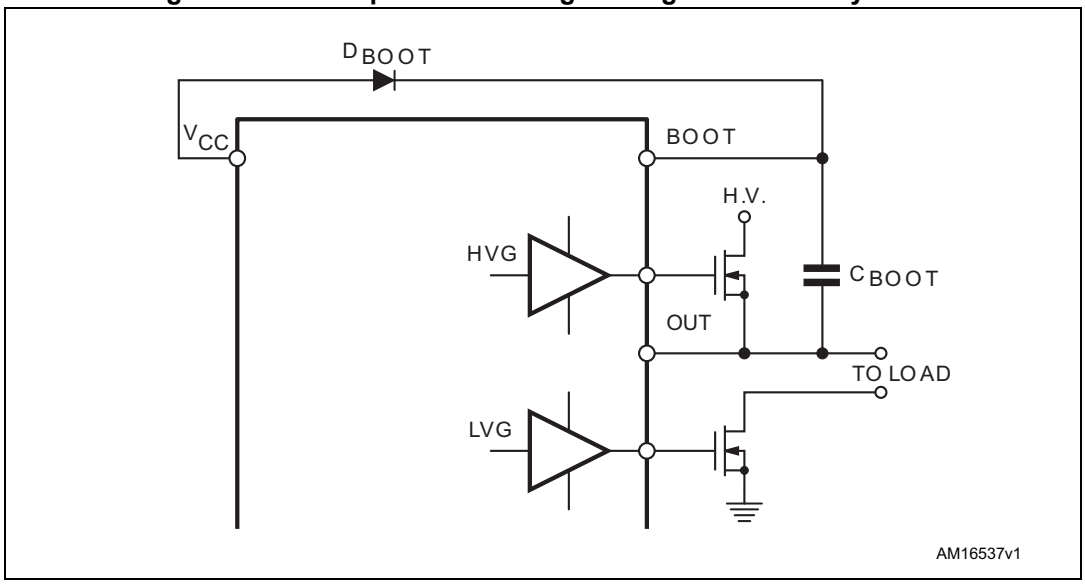
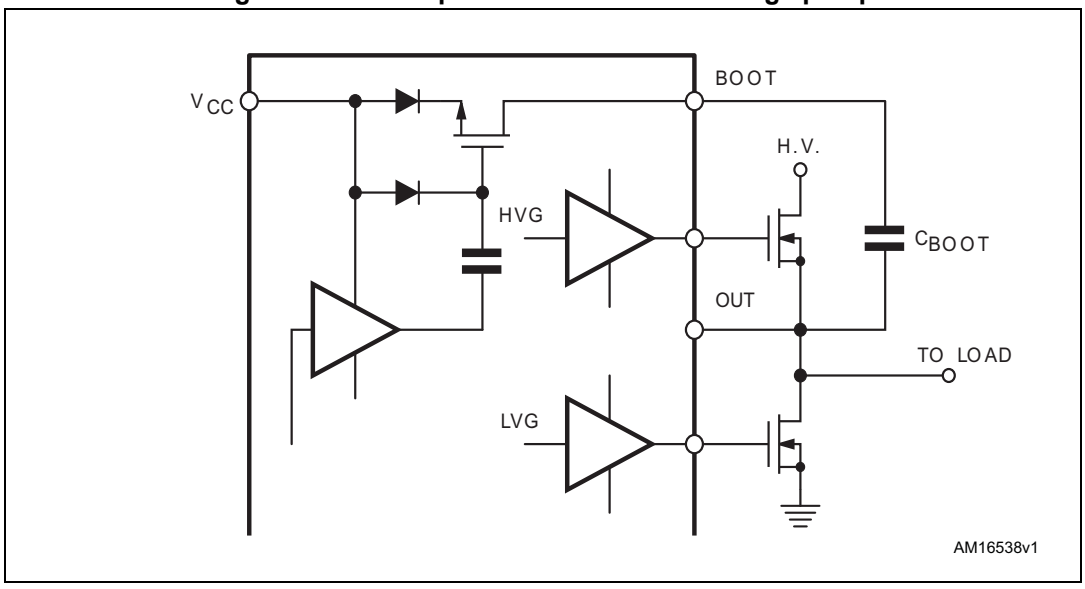


Figure 7. Bootstrap driver with internal charge pump



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

SO-8 package information

Figure 8. SO-8 package outline

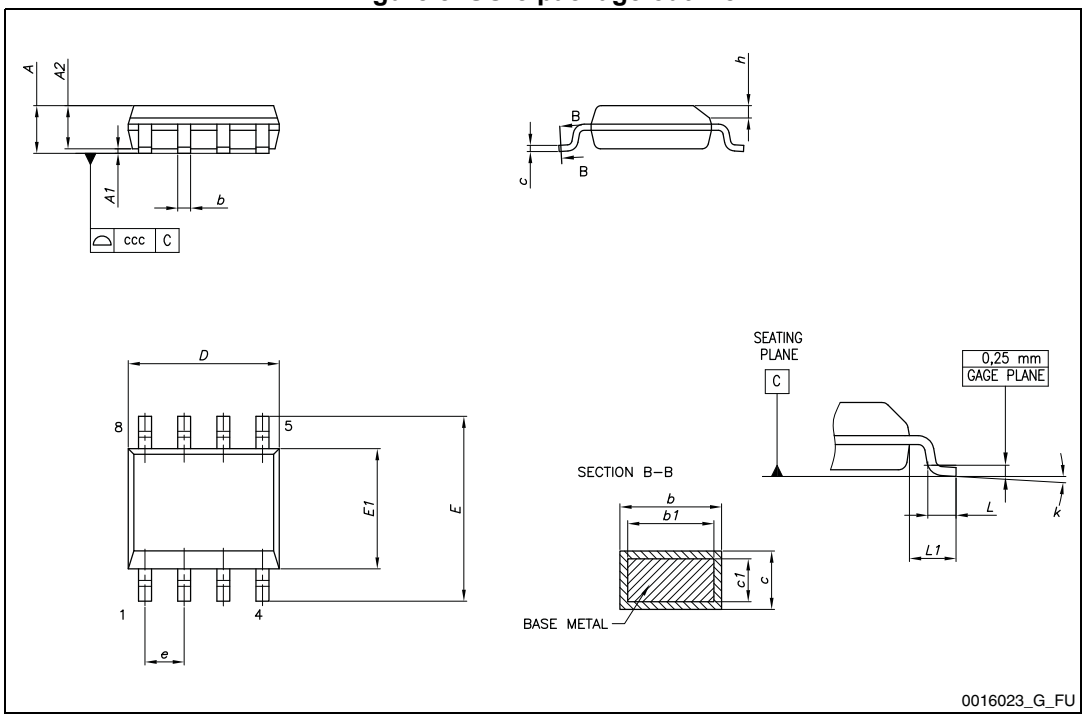
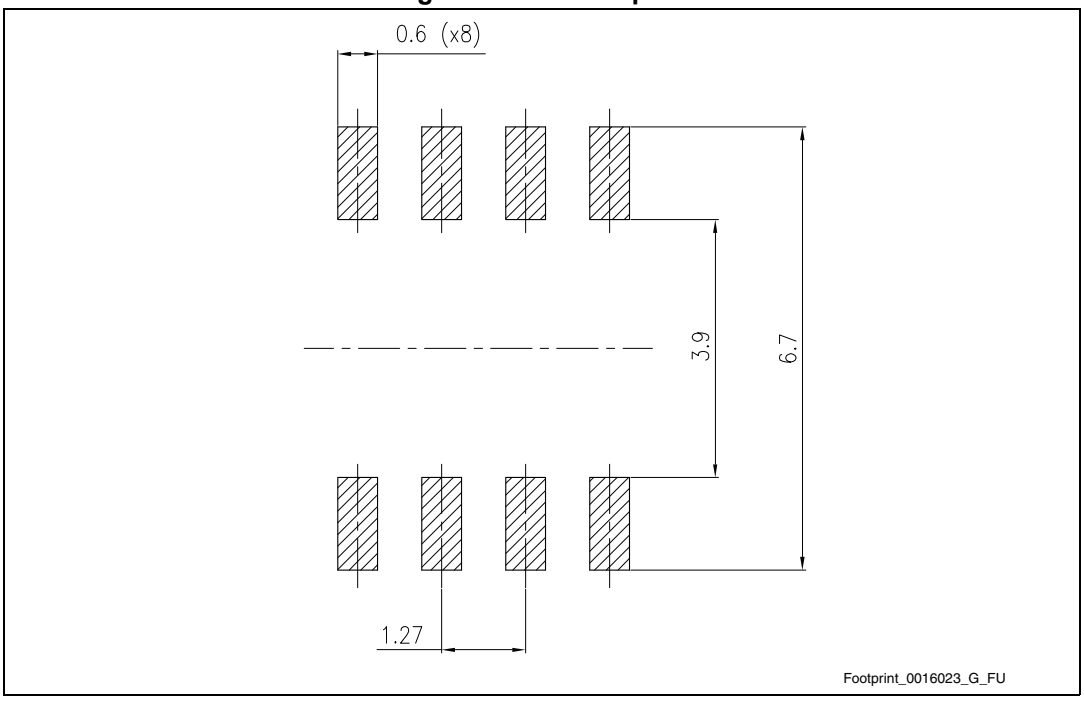


Table 8. SO-8 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 9. SO-8 footprint



9 Order codes

Table 9. Order codes

Order codes	Package	Packaging
L6395D	SO-8	Tube
L6395DTR	SO-8	Tape and reel

10 Revision history

Table 10. Document revision history

Date	Revision	Changes
20-Mar-2013	1	Initial release.
11-Sep-2015	2	Updated *Table 4 on page 6* (added ESD parameter and value). Updated note *2.* below *Table 7 on page 8* (replaced V_{CBOOTx} by V_{BOOTx}). Updated *Section 8 on page 13*. Moved *Table 9 on page 15* (moved from page 1 to page 15, updated/added titles). Minor modifications throughout document.