Errata

MCF5249E/D
Rev. 2, 11/2003

MCF5249 / MCF5249L
Device Errata

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This document identifies implementation differences between the MCF5249 processor and the description contained in the *MCF5249 User's Manual*. Please check the worldwide web at http://motorola.com/semiconductors for the latest updates.

Table 1 summarizes the MCF5249 errata.

Table 1 Summary of Errata

Errata ID	Module Affected	Date Errata Added	Applicable Mask Sets	Errata Title
1	PLL	3/20/03	0L99H – 5L99H	PLL Audio Clock (MCLK1, MCLK2) Generation Bug
2	QSPI	3/20/03	0L99H – 5L99H	QSPI Register Read Back Error
3	SDRAMC	3/20/03	0L99H, 2L99H, 4L99H	Address Signal A[24] Unavailable
4	EMAC	04/28/03	0L99H – 5L99H	Unexpected Pipeline Stall on EMAC Load / Store Accumulator Instruction

Errata 1 PLL Audio Clock (MCLK1, MCLK2) Generation Bug

1.1 Description

- When using the divide-by-four mode, there is a potential for the PLL to generate an incorrect clock (MCLK1 and/or MCLK2).
- When using the divide-by-three mode, a 50% duty cycle of the divided clock (MCLK1 and/or MCLK2) cannot be guaranteed.

1.2 Workaround

None. To avoid the issues stated above, use only the divide-by-two mode of the PLL. This can be achieved by keeping the CRSEL bit in the PLL control register (PLLCR)
set to 1.

Masks: 0L99H, 1L99H, 2L99H, 3L99H, 4L99H, 5L99H

Errata 2 QSPI Register Read Back Error

2.1 Description

When the 16-bit QSPI registers are read back as 32-bit longwords, the order in which the individual words are read is swapped. The longword, [31:16][15:0], is read as [15:0][31:16].

2.2 Workaround

Access the 16-bit QSPI registers only as 16-bit words.

Masks: 0L99H, 1L99H, 2L99H, 3L99H, 4L99H, 5L99H

Errata 3 Address Signal A[24] Unavailable

3.1 Description

For the 160 MAPBGA package of MCF5249, address line A[24] is not available. Instead address signal A[25] is available for use. Therefore, the accessible address lines for this package are A[23:1] and A[25].

This can cause non-contiguous memory space problems while interfacing to the following SDRAM sizes:

- 256Mbit (32Mbyte) SDRAM when the data bus is 8/16-bits wide, and
- 128Mbit (16Mbyte) SDRAM when the data bus is 8-bits wide.

3.2 Workaround

Allocate double the amount of space required for the SDRAM in the application's memory map (64Mbytes allocated for 32Mbyte SDRAM and 32Mbytes for 16Mbyte SDRAM). In the application's linker file, offset the start of the SDRAM by 16Mbytes in the 32Mbyte SDRAM case and by 8Mbytes in the 16Mbyte SDRAM case. This will make the entire accessible memory region contiguous.

Devices Affected: Only 160 MAPBGA package, MCF5249 [Not MCF5249L]
Masks: 0L99H, 2L99H, 4L99H

Errata 4 Unexpected Pipeline Stall on EMAC Load / Store Accumulator Instruction

4.1 Description

An unexpected pipeline stall occurs for accumulator load and accumulator store instructions that immediately follow a load accumulator or MAC instruction.

Specifically, the operand execution pipeline OEP is experiencing a 2T pipeline stall when a load/store accumulator instruction enters the pipeline immediately after any load accumulator or MAC instruction. The pipeline is supposed to stall only if there is a store accumulator instruction immediately following a load or MAC instruction which updated the specified accumulator.

A simple example can be created to expose this problem:

```
mac.l  ra,rb,acc0

mac.l  rc,rd,acc0

mov.l  acc1,rx
```

In the above example, the store of acc1 (mov.l acc1,rx) should not experience any stall since that accumulator is not being updated. In the current V2+EMAC implementation, it is being incorrectly stalled for 2 cycles.

NOTE

The operation of the instructions is correct. The only problem is that the expected timing is not.

4.2 Workarounds

No workaround.

Masks: 0L99H – 5L99H

Appendix A Revision History

Table 3 MCF5407 Processor Errata Change HIstory

Revision	Date	Change History
Rev 0	03/20/03	Initial Errata.
Rev 1	04/28/03	Unexpected Pipeline Stall on EMAC Load / Store Accumulator Instruction
Rev 2	10/30/03	Removal of Errata 4: DMA Writes to UART Cause Transmission Errors

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