

**450V P-CHANNEL ENHANCEMENT MODE MOSFET**
**Product Summary**

$BV_{DSS}$	$R_{DS(ON)}$	$I_D$ $T_A = +25^\circ C$
-450V	150Ω @ $V_{GS} = -10V$	-0.25A

**Description**

This 450V enhancement mode P-channel MOSFET provides users with a competitive specification offering efficient power handling capability, high impedance and is free from thermal runaway and thermally induced secondary breakdown. Applications benefiting from this device include a variety of Telecom and general high voltage switching circuits.

**Applications**

- Load Switching
- Uninterrupted Power Supply

**Features and Benefits**

- Low Gate Drive
- Low Input Capacitance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

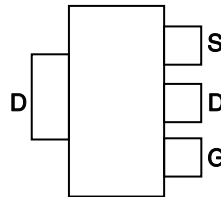
**Mechanical Data**

- Case: SOT223
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See Diagram Below
- Terminals: Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 <sup>(e3)</sup>
- Weight: 0.112 grams (Approximate)

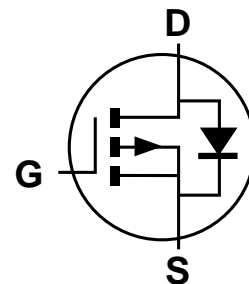
SOT223



Top View



Pin Out - Top View



Equivalent Circuit

**Ordering Information (Note 4)**

Part Number	Qualification	Case	Packaging
DMP45H150DHE-13	Standard	SOT223	2,500/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

**Marking Information**


**DII** = Manufacturer's Marking  
**P450H2** = Marking Code  
**YWW** = Date Code Marking  
 Y or Y = Year (ex: 7 = 2017)  
 WW = Week (01 to 53)

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	-450	V	
Gate-Source Voltage	V <sub>GSS</sub>	±30	V	
Continuous Drain Current (Note 5) V <sub>GS</sub> = -10V	I <sub>D</sub>	T <sub>C</sub> = +25°C T <sub>C</sub> = +70°C	-0.25 -0.20	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I <sub>DM</sub>	-0.45	A
Maximum Body Diode Continuous Current	I <sub>S</sub>	-0.45	A	
Avalanche Energy (Note 6) L=60mH	E <sub>AS</sub>	4	mJ	
Avalanche Current (Note 6) L=60mH	I <sub>AS</sub>	0.25	A	
Peak Diode Recovery dv/dt (I <sub>SD</sub> ≤ 1.0A, di/dt ≤ 100A/µs)	dv/dt	4.5	V/ns	

**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Total Power Dissipation (Note 6)	P <sub>D</sub>	T <sub>C</sub> = +25°C	13.9	W
		T <sub>C</sub> = +70°C	8.9	°C/W
Thermal Resistance, Junction to Ambient	R <sub>θJA</sub>	59.4	W	
Thermal Resistance, Junction to Case	R <sub>θJC</sub>	8.9	°C/W	
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C	

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS</b> (Note 5)						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-450	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250µA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	-1	µA	V <sub>DS</sub> = -450V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±30V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS</b> (Note 5)						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	-2.0	-3.0	-4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250µA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	40	150	Ω	V <sub>GS</sub> = -10V, I <sub>D</sub> = -50mA
Diode Forward Voltage	V <sub>SD</sub>	—	-0.8	-1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -50mA
<b>DYNAMIC CHARACTERISTICS</b> (Note 6)						
Input Capacitance	C <sub>ISS</sub>	—	59.2	—	pF	V <sub>DS</sub> = -25V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>OSS</sub>	—	11	—		
Reverse Transfer Capacitance	C <sub>RSS</sub>	—	1	—		
Forward Transconductance	g <sub>FS</sub>	40	—	—	ms	V <sub>DS</sub> = -25V, I <sub>D</sub> = -50mA
Gate Resistance	R <sub>G</sub>	—	50	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1.0MHz
Total Gate Charge	Q <sub>G</sub>	—	1.8	—	nC	V <sub>DS</sub> = -225V, I <sub>D</sub> = -100mA, V <sub>GS</sub> = -10V
Gate-Source Charge	Q <sub>GS</sub>	—	0.3	—		
Gate-Drain Charge	Q <sub>GD</sub>	—	0.9	—		
Turn-On Delay Time	t <sub>D(ON)</sub>	—	12	—	ns	V <sub>DD</sub> = -225V, R <sub>G</sub> = 3.0Ω, I <sub>D</sub> = -100mA
Turn-On Rise Time	t <sub>R</sub>	—	9	—		
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	19	—		
Turn-Off Fall Time	t <sub>F</sub>	—	87	—		
Body Diode Reverse Recovery Time	t <sub>RR</sub>	—	108	—	ns	V <sub>GS</sub> = 0V, I <sub>S</sub> = -100mA, V <sub>DD</sub> = -100V, di/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q <sub>RR</sub>	—	391	—	nC	V <sub>GS</sub> = 0V, I <sub>S</sub> = -100mA, V <sub>DD</sub> = -100V, di/dt = 100A/µs

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with 1 inch square copper pad layout.  
6. Guaranteed by design. Not subject to production testing.

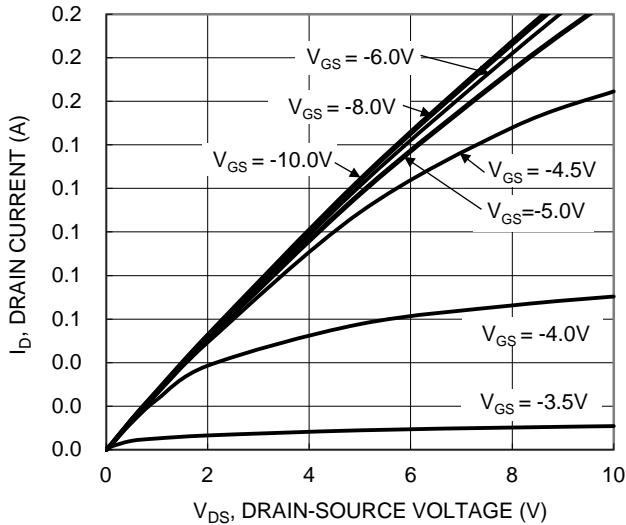


Figure 1. Typical Output Characteristic

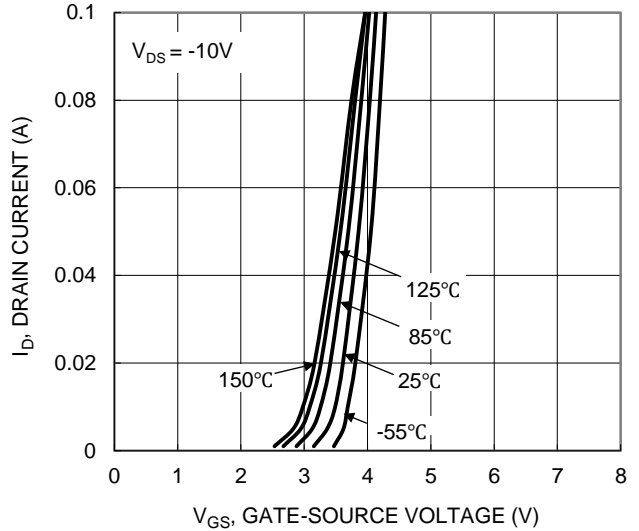


Figure 2. Typical Transfer Characteristic

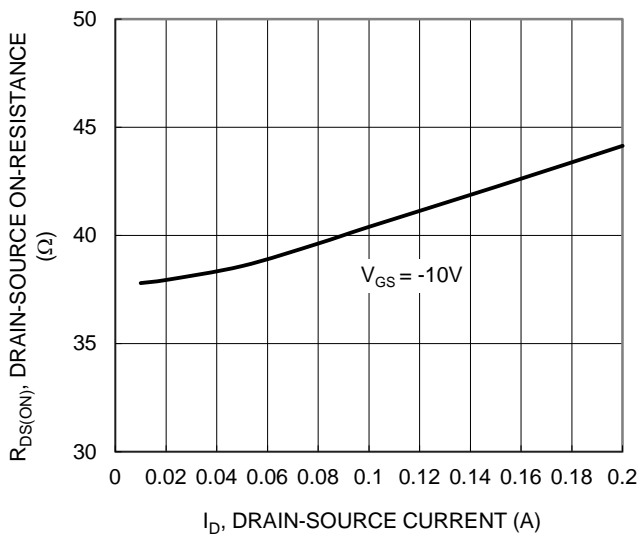


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

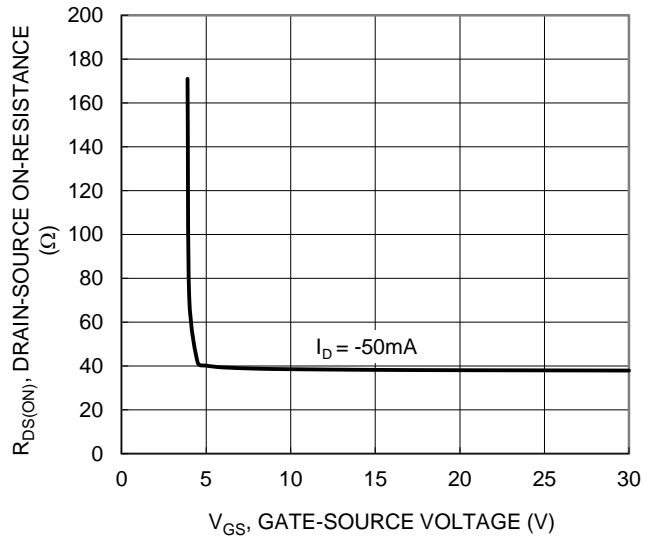


Figure 4. Typical Transfer Characteristic

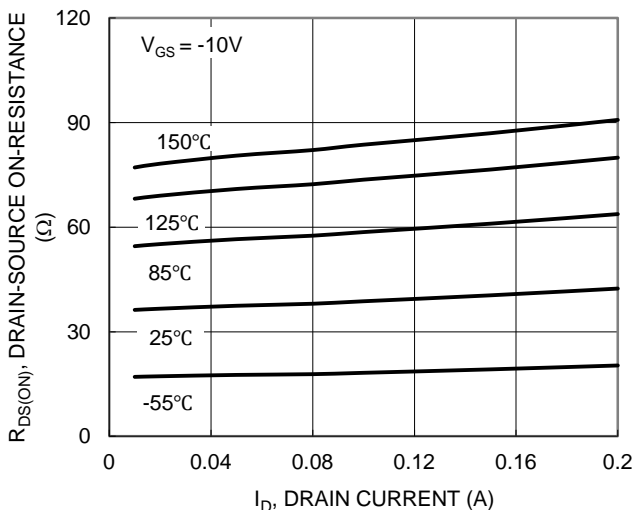


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

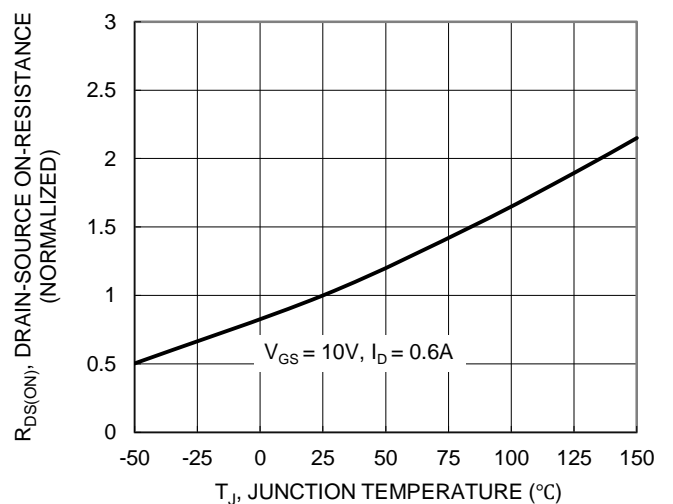


Figure 6. On-Resistance Variation with Temperature

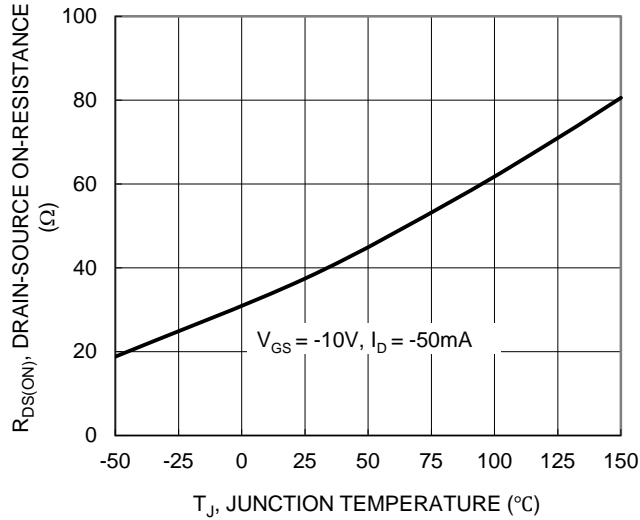


Figure 7. On-Resistance Variation with Temperature

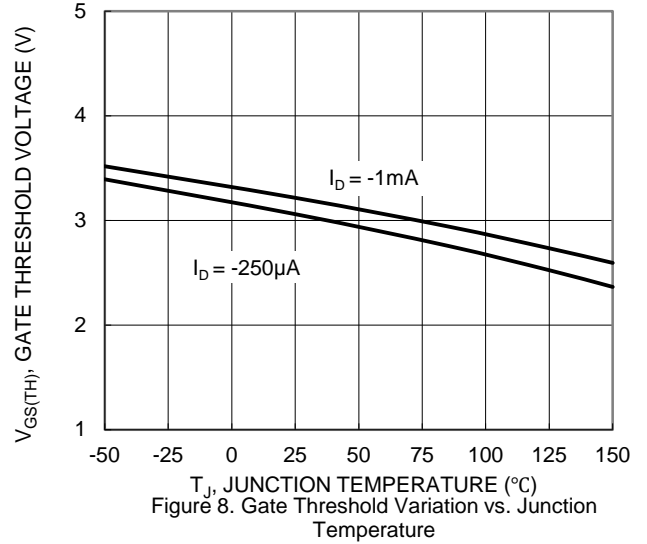


Figure 8. Gate Threshold Variation vs. Junction Temperature

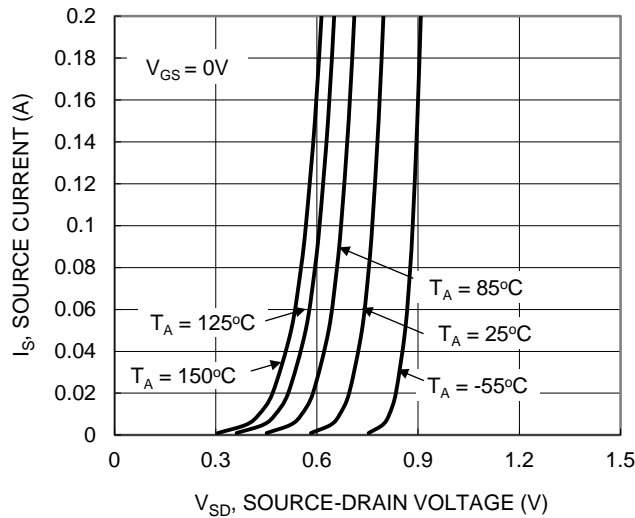


Figure 9. Diode Forward Voltage vs. Current

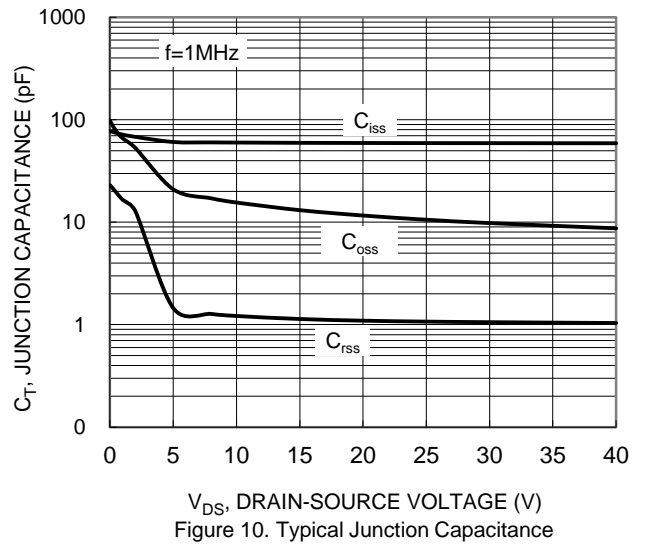


Figure 10. Typical Junction Capacitance

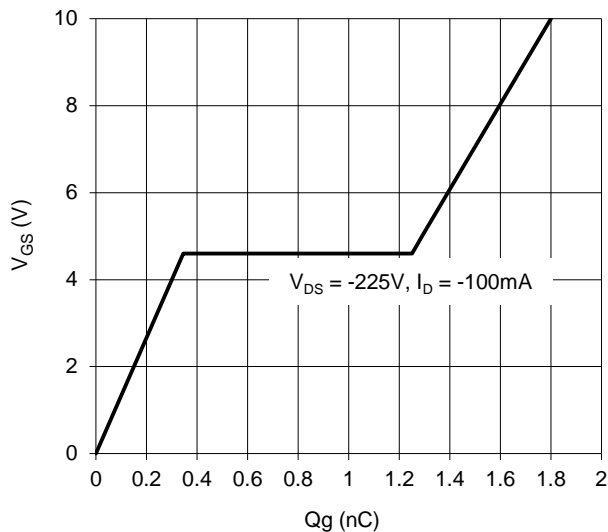


Figure 11. Gate Charge

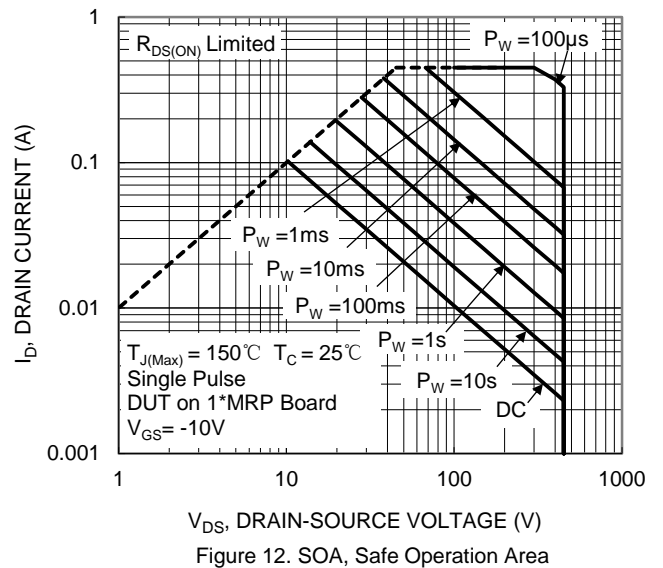
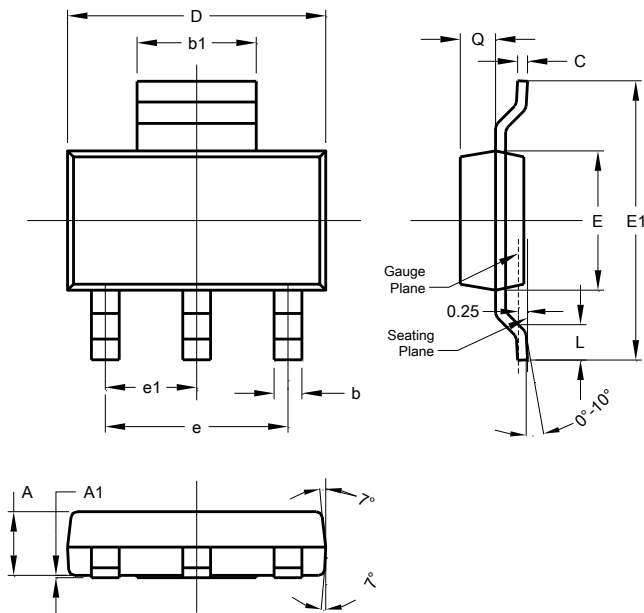


Figure 12. SOA, Safe Operation Area

**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**SOT223**

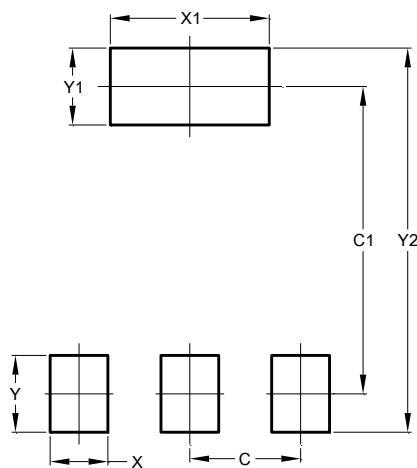


SOT223			
Dim	Min	Max	Typ
A	1.55	1.65	1.60
A1	0.010	0.15	0.05
b	0.60	0.80	0.70
b1	2.90	3.10	3.00
C	0.20	0.30	0.25
D	6.45	6.55	6.50
E	3.45	3.55	3.50
E1	6.90	7.10	7.00
e	-	-	4.60
e1	-	-	2.30
L	0.85	1.05	0.95
Q	0.84	0.94	0.89
All Dimensions in mm			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**SOT223**



Dimensions	Value (in mm)
C	2.30
C1	6.40
X	1.20
X1	3.30
Y	1.60
Y1	1.60
Y2	8.00

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