



**MICROCHIP**

# dsPIC33FJ12GP202

## dsPIC33FJ12GP202 PIM Information Sheet

The dsPIC33FJ12GP202 PIM is designed to demonstrate the capabilities of the dsPIC33FJ12GP202 family of general purpose devices using the Explorer 16 Development Board and the PICtail™ Plus daughter boards.

The dsPIC33FJ12GP202 is a high-performance 16-bit digital signal controller within a small 28-pin 6x6 mm QFN package.

The dsPIC33FJ12GP202 is equipped with Peripheral Pin Select (PPS), which allows many of the digital peripherals to be remapped to use any number of pins on the device.

The PIM takes advantage of PPS by using zero ohm resistors to connect the I/O to the 100-pin Explorer 16 Development Board. Simply removing the zero ohm resistors and using the test points associated with each I/O pin (i.e., RP0, RP1, etc.), allows the designer to reroute the pin to any of the available pins on the Explorer 16 Development Board. This capability enables easier and faster design times.

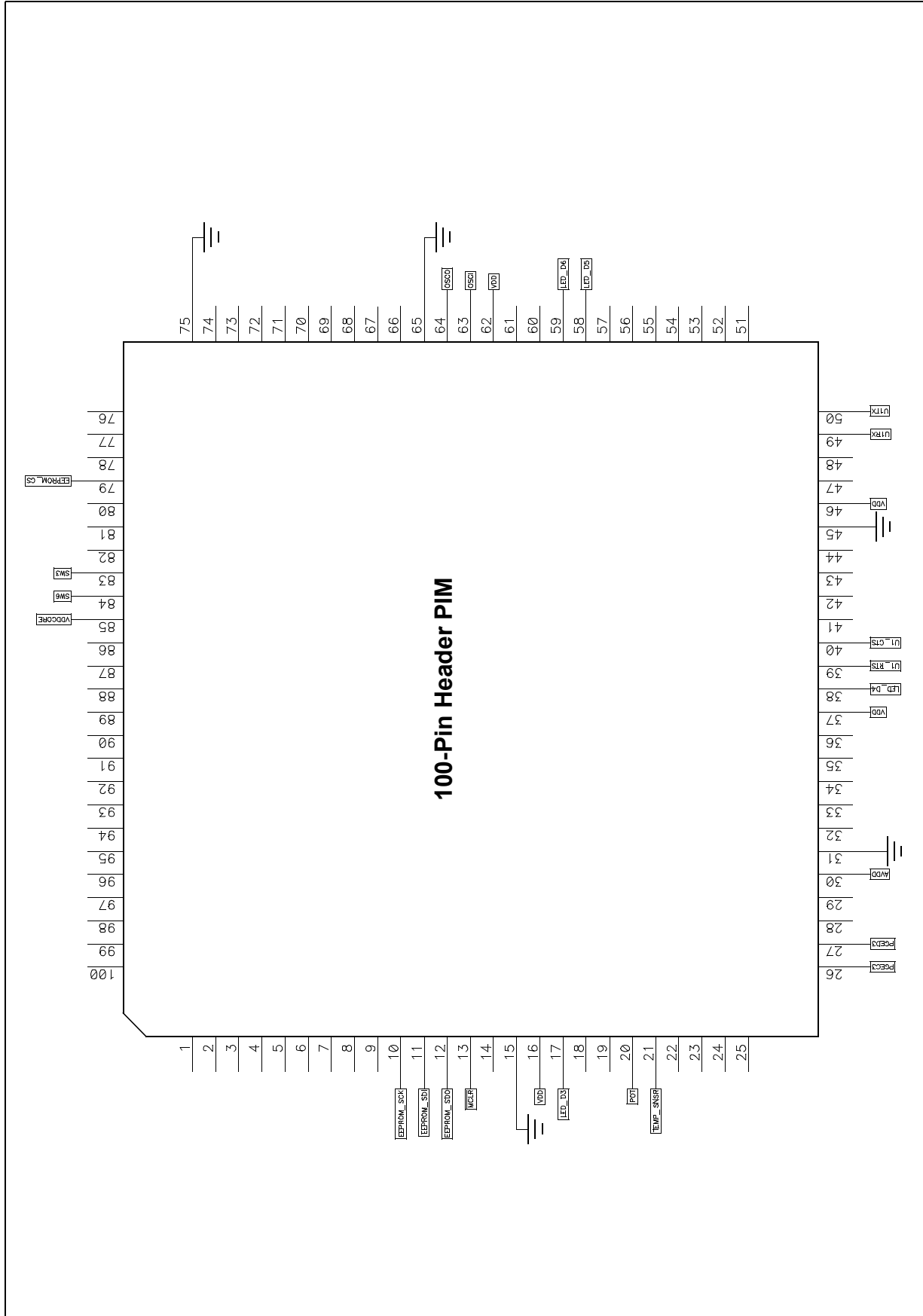
Table 1 shows the mapping between the Explorer 16 functions and the device pins.

**TABLE 1: 28-PIN TO 100-PIN PINOUT**

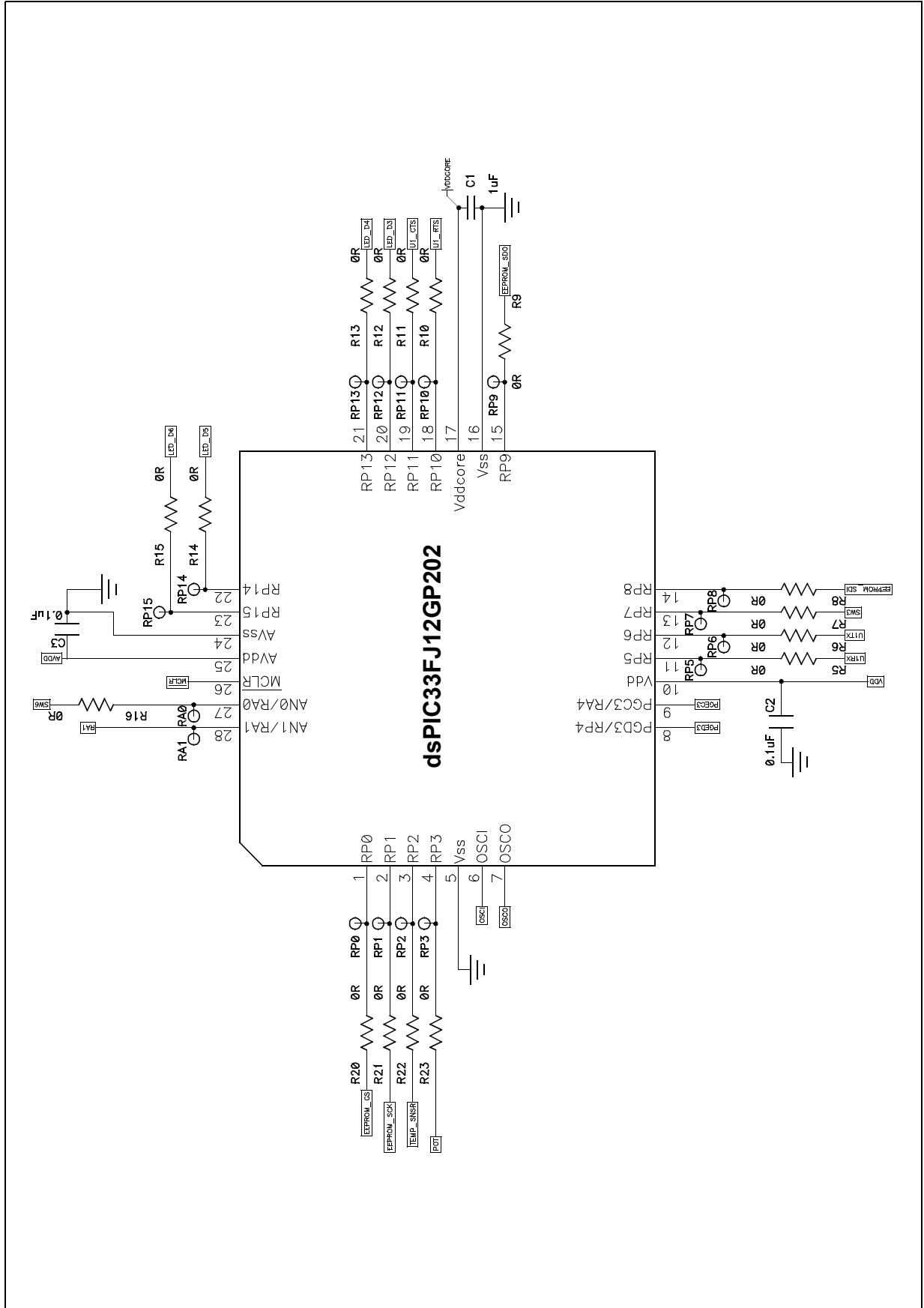
Device Pin Number	dsPIC33FJ12GP202	PIM Pin Number	Functional Description
1	PGED1/AN2/RP0/CN4 RB0	79	EEPROM CS
2	PGEC1/AN3/RP1/CN5/RB1	10	EEPROM SCK
3	AN4/RP2/CN6/RB2	21	Temp Sensor
4	AN5/RP3/CN7/RB3	20	POT
5	Vss	15	
6	OSCI/CLKI/CN30/RA2	63	OSCI
7	OSCO/CLKO/CN29/RA3	64	OSCO
8	PGED3/SOSCI/RP4/CN1/RB4	27	Debug
9	PGEC3/SOSCO/T1CK/CN0/RA4	26	Debug
10	VDD	16	
11	ASDA1/RP5/CN27/RB5	49	U1RX
12	ASCL1/RP6/CN24/RB6	50	U1TX
13	INT0/RP7/CN23/RB7	83	SW3
14	TCK/SCL1/RP8/CN22/RB8	11	EEPROM SDI
15	TDO/SDA1/RP9/CN21/RB9	12	EEPROM SDO
16	Vss	36	
17	VCAP/VDDCORE	85	
18	TDI/RP10/CN16/RB10	39	U1RTS
19	TMS/RP11/CN15/RB11	40	U1CTS
20	AN9/RP12/CN14/RB12	17	LED D3
21	AN8/RP13/CN13/RB13	38	LED D4
22	AN7/RP14/CN12/RB14	58	LED D5
23	AN6/RP15/CN11/RB15	59	LED D6
24	AVss	31	
25	AVDD	30	
26	MCLR	13	Master Clear
27	PGED2/AN0/VREF+/CN2/RA0	84	SW6
28	PGEC2/AN1/VREF-/CN3/RA1		

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FIGURE 1: 100-PIN HEADER SCHEMATIC



**FIGURE 2: 28-PIN DEVICE SCHEMATIC**



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NOTES:

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