MT90869

Flexible 16 K Digital Switch (F16kDX)

Data Sheet

Features

December 2010

- 16,384-channel x 16,384-channel non-blocking unidirectional switching.The Backplane and Local inputs and outputs can be combined to form a non-blocking switching matrix with 64 stream inputs and 64 stream outputs
- 8,192-channel x 8,192-channel non-blocking Backplane to Local stream switch
- 8,192-channel x 8,192-channel non-blocking Local to Backplane stream switch
- 8,192-channel x 8,192-channel non-blocking Backplane input to Backplane output switch
- 8,192-channel x 8,192-channel non-blocking Local input to Local output stream switch
- Rate conversion on all data paths, Backplane to Local, Local to Backplane, Backplane to Backplane and Local to Local streams
- Backplane port accepts 32 ST-BUS streams with data rates of 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s in any combination, or a fixed allocation of 16 streams at 32.768 Mb/s

Ordering Information

MT90869AG	272 Ball PBGA	Trays
MT90869AG2	272 Ball PBGA*	Trays

*Pb Free Tin/Silver/Copper

-40 to +85^{o}C

***Note**: the package thickness is different than the MT90869AG (see drawing at the end of the data sheet).

- Local port accepts 32 ST-BUS streams with data rates of 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s, in any combination
- Per-stream channel and bit delay for Local input streams
- Per-stream channel and bit delay for Backplane input streams
- Per-stream advancement for Local output streams
- Per-stream advancement for Backplane output streams
- Constant throughput delay for frame integrity

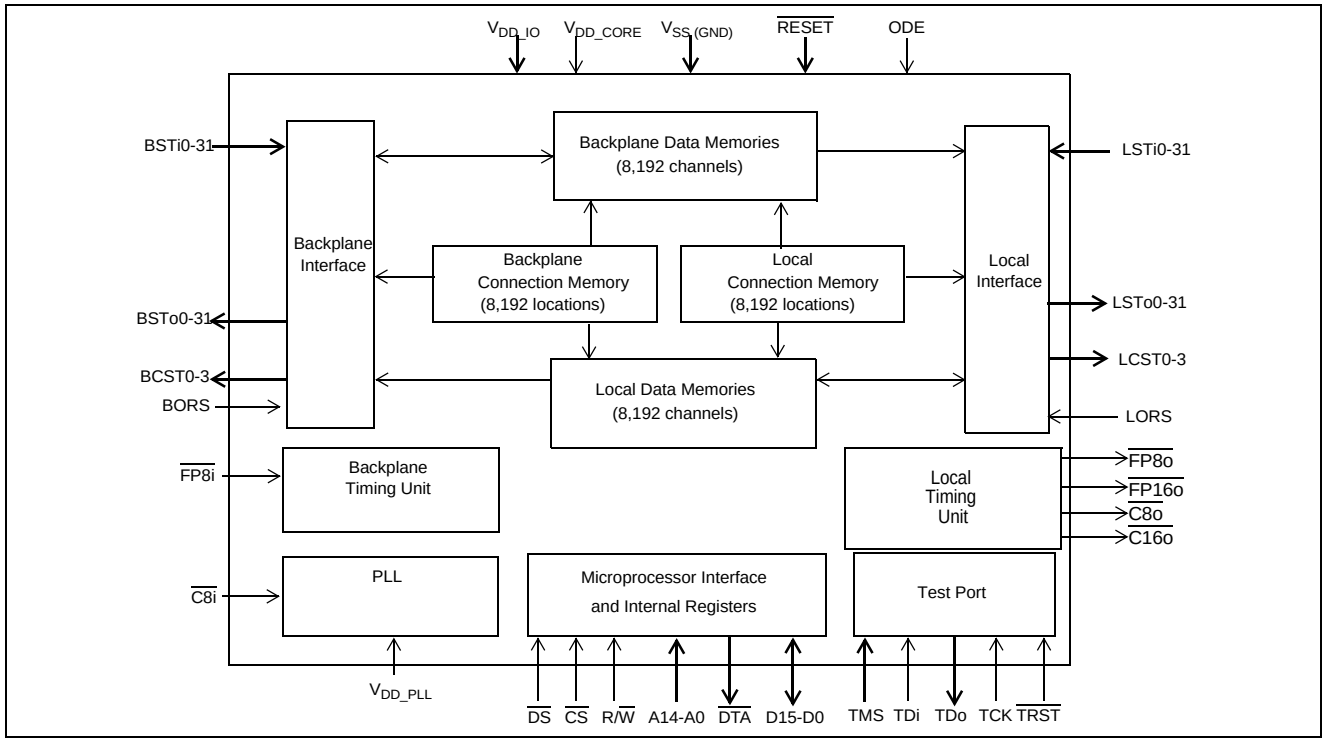

Figure 1 - MT90869 Functional Block Diagram

- Per-channel high impedance output control for Local and Backplane streams
- Per-channel driven-high output control for local and backplane streams
- High impedance-control outputs for external drivers on backplane and local port
- Per-channel message mode for local and backplane output streams
- Connection memory block programming for fast device initialization
- BER testing for local and backplane ports.
- Automatic selection between ST-BUS and GCI-BUS operation
- Non-multiplexed Motorola microprocessor interface
- Conforms to the mandatory requirements of the IEEE-1149.1 (JTAG) standard
- Memory Built-In-Self-Test (BIST), controlled via microprocessor registers
- 1.8 V core supply voltage
- 3.3 V I/O supply voltage
- 5 V tolerant inputs, outputs and I/Os
- Per stream subrate switching at 4 bit, 2 bit and 1 bit depending on stream data rate

Applications

- Central Office Switches (Class 5)
- Mediation Switches
- Class-independent switches
- Access Concentrators
- Scalable TDM-Based Architectures
- Digital Loop Carriers

Device Overview

The MT90869 has two data ports, the Backplane and the Local port. The Backplane port has two modes of operation, either 32 input and 32 output streams operated at 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s, in any combination, or 16 input and 16 output streams operated at 32.768 Mb/s. The Local port has 32 input and 32 output streams operated at 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s, in any combination.

The MT90869 contains two data memory blocks (Backplane and Local) to provide the following switching path configurations:

- Backplane-to-Local, supporting 8 K x 8 K data switching,
- Local-to-Backplane, supporting 8 K x 8 K data switching,
- Backplane-to-Backplane, supporting 8 K x 8 K data switching.
- Local-to-Local, supporting 8 K x 8 K data switching.

The device contains two connection memory blocks, one for the Backplane output and one for the Local output. Data to be output on the serial streams may come from either of the data memories (Connection Mode) or directly from the connection memory contents (Message Mode).

In Connection Mode the contents of the connection memory defines, for each output stream and channel, the source stream and channel (stored in data memory) to be switched.

In Message Mode, microprocessor data can be written to the connection memory for broadcast on the output streams on a per channel basis. This feature is useful for transferring control and status information to external circuits or other ST-BUS devices.

The device uses a master frame pulse ($\overline{\text{FP8i}}$) and master clock ($\overline{\text{C8i}}$) to define the frame boundary and timing for both the backplane port and the local port. The device will automatically detect whether an ST-BUS or a GCI-BUS style frame pulse is being used. There is a two frame delay from the time $\overline{\text{RESET}}$ is de-asserted to the establishment of full switch functionality. During this period the frame format is determined before switching begins.

The device provides $\overline{\text{FP8o}}$, $\overline{\text{FP16o}}$, $\overline{\text{C8o}}$ and $\overline{\text{C16o}}$ outputs to support external devices connected to the local port.

Subrate switching is accomplished by oversampling (i.e., 1 bit switching can be accomplished by sampling a 2 Mb/s stream at 16 Mbps). Refer to MSAN 175.

A non-multiplexed Motorola microprocessor port allows programming of the various device operation modes and switching configurations. The microprocessor port provides access for Register read/write, Connection Memory read/write and Data Memory read-only operations. The port has a 15-bit address bus, 16-bit data bus and 4 control signals. The microprocessor may monitor channel data in the backplane and local data memories.

The mandatory requirements of the IEEE-1149.1 (JTAG) standard are fully supported via a dedicated test port.

The MT90869 is manufactured in a 27 mm x 27 mm body, 1.27 mm ball-pitch, 272-PBGA to JEDEC standard MS-034 BAL-2 Iss. A.

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Changes Summary

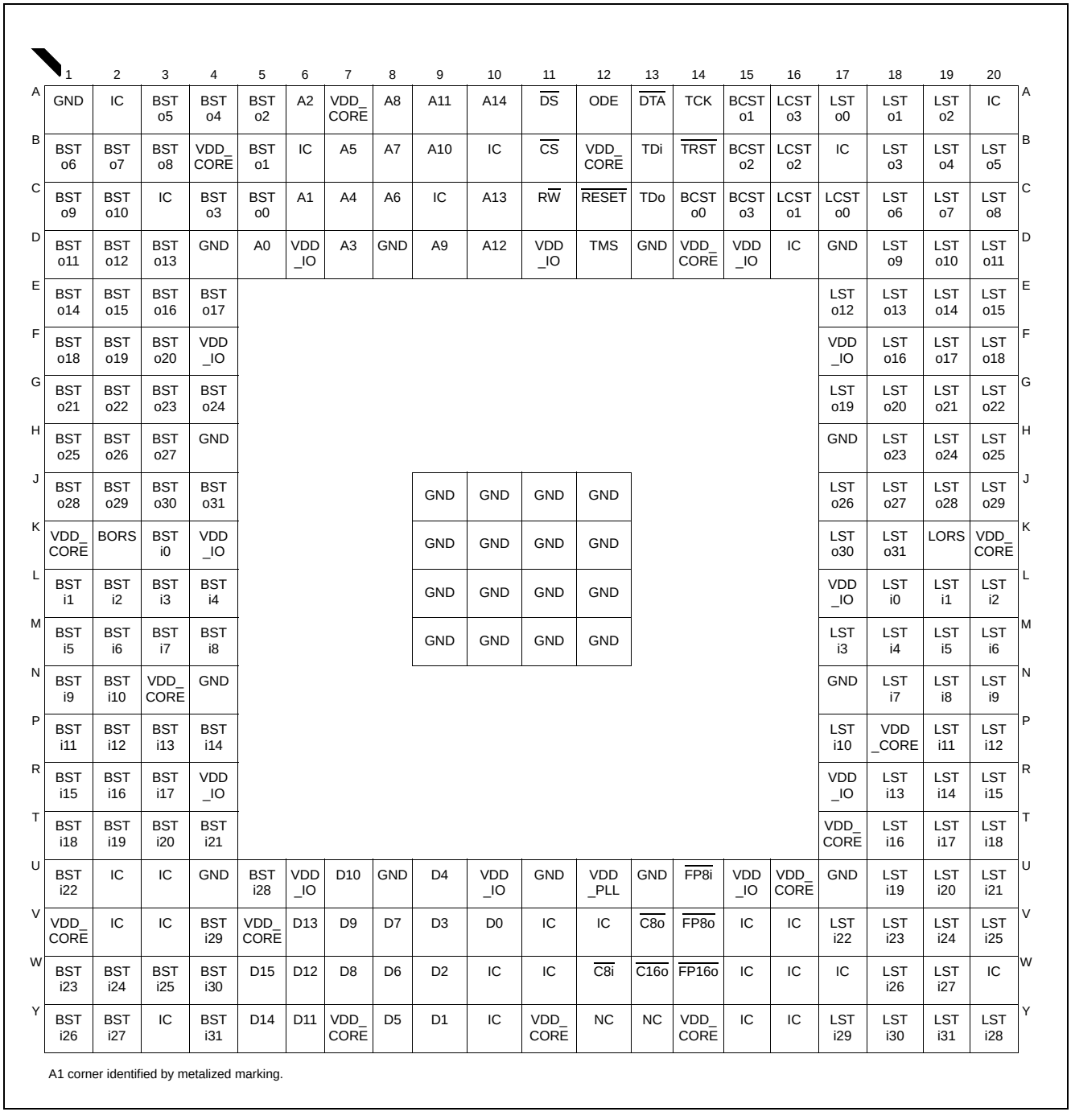
The following table captures the changes from the November 2005 issue.

Page	Item	Change
83	Package Drawing	Changed package Bill of Material with a thinner substrate thickness.

The following table captures the changes from the December 2002 issue.

Page	Item	Change
14	Pin Description, $\overline{C8i}$	The internal frame boundary alignment description is changed from the clock rising or falling edge to rising edge only. Also added description to specify setting the C8IPOL bit in the Control Register to one for clock rising edge alignment operation.
20	Figure 6, Local Port Timing Diagram for 2,4,8 and 16 Mb/s stream rates	Changed $\overline{C8i}$ frame boundary active edge from falling to rising edge.
22	Figure 7, Backplane Port Timing Diagram for 2, 4, 8, 16 and 32 Mb/s stream rates	Changed $\overline{C8i}$ frame boundary active edge from falling to rising edge.
22	Section 2.3. Backplane Frame Pulse Input and Master Input Clock Timing	Removed the falling clock edge frame boundary alignment option.
23	Figure 8, Backplane and Local Frame Pulse Alignment for Data Rates of 2 Mb/s, 4 Mb/s, 8 Mb/s and 16 Mb/s	Changed $\overline{C8i}$ frame boundary active edge from falling to rising edge.
24	Figure 9, Backplane and Local Input Channel Delay Timing Diagram	Changed $\overline{FPo}$ and $\overline{C8o}$ to $\overline{FPi}$ and $\overline{C8i}$ respectively and showing rising $\overline{C8i}$ frame boundary active edge.
25	Figure 10, Backplane and Local Input Bit Delay Timing Diagram for Data Rate of 16 Mb/s	Changed $\overline{FPo}$ and $\overline{C8o}$ to $\overline{FPi}$ and $\overline{C8i}$ respectively and showing rising C8i frame boundary active edge.
26	Figure 11, Backplane and Local Input Bit Delay Timing Diagram for Data Rate of 8 Mb/s	Changed $\overline{FPo}$ and $\overline{C8o}$ to $\overline{FPi}$ and $\overline{C8i}$ respectively.
51	Section 13.1. Control Register (CR) Bit 6, C8IPOL	Changed description to specify Bit 6, C8IPOL must be set high for rising clock edge frame boundary alignment operation.
52	Figure 18, Frame Boundary Conditions, ST- BUS Operation	Removed waveforms showing $\overline{C8i}$ falling edge frame boundary option.
53	Figure 19, Frame Boundary Conditions, GCI - BUS Operation	Removed waveforms showing $\overline{C8i}$ falling edge frame boundary option.

Page	Item	Change
72	Backplane and Local Clock Timing: Item 2, Backplane Frame Pulse Setup Time before C8i clock falling edge Item 3, Backplane Frame Pulse Hold Time from C8i clock falling edge	Item 2, Backplane Frame Pulse Setup Time before C8i clock falling edge changed to Backplane Frame Pulse Setup Time before C8i clock rising edge. Item 3, Backplane Frame Pulse Hold Time from C8i clock falling edge changed to Backplane Frame Pulse Hold Time from C8i clock rising edge.
73	Figure 20, Backplane and Local Clock Timing Diagram for ST-BUS	Changed C8i frame boundary active edge from falling to rising edge.
75	Figure 22, ST-BUS Backplane Data Timing Diagram (8 Mb/s, 4 Mb/s, 2 Mb/s)	Changed C8i frame boundary active edge from falling to rising edge.
76	Figure 23, ST-BUS Backplane Data Timing Diagram (32 Mb/s, 16 Mb/s)	Changed C8i frame boundary active edge from falling to rising edge.
79	Figure 26, ST-BUS Local Timing Diagram (16 Mb/s)	Changed C8i frame boundary active edge from falling to rising edge.
80	Figure 27, ST-BUS Local Data Timing Diagram (8 Mb/s, 4 Mb/s, 2 Mb/s)	Changed FPo and C8o to FPi and C8i respectively and showing rising C8i frame boundary active edge.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	IC	BST o5	BST o4	BST o2	A2	VDD_ CORE	A8	A11	A14	$\overline{DS}$	ODE	$\overline{DTA}$	TCK	BCST o1	LCST o3	LST o0	LST o1	LST o2	IC	A
B	BST o6	BST o7	BST o8	VDD_ CORE	BST o1	IC	A5	A7	A10	IC	$\overline{CS}$	VDD_ CORE	TDi	$\overline{TRST}$	BCST o2	LCST o2	IC	LST o3	LST o4	LST o5	B
C	BST o9	BST o10	IC	BST o3	BST o0	A1	A4	A6	IC	A13	R$\overline{W}$	$\overline{RESET}$	TDo	BCST o0	BCST o3	LCST o1	LCST o0	LST o6	LST o7	LST o8	C
D	BST o11	BST o12	BST o13	GND	A0	VDD _IO	A3	GND	A9	A12	VDD _IO	TMS	GND	VDD_ CORE	VDD _IO	IC	GND	LST o9	LST o10	LST o11	D
E	BST o14	BST o15	BST o16	BST o17													LST o12	LST o13	LST o14	LST o15	E
F	BST o18	BST o19	BST o20	VDD _IO													VDD _IO	LST o16	LST o17	LST o18	F
G	BST o21	BST o22	BST o23	BST o24													LST o19	LST o20	LST o21	LST o22	G
H	BST o25	BST o26	BST o27	GND													GND	LST o23	LST o24	LST o25	H
J	BST o28	BST o29	BST o30	BST o31					GND	GND	GND	GND					LST o26	LST o27	LST o28	LST o29	J
K	VDD_ CORE	BORS	BST i0	VDD _IO					GND	GND	GND	GND					LST o30	LST o31	LORS	VDD_ CORE	K
L	BST i1	BST i2	BST i3	BST i4					GND	GND	GND	GND					VDD _IO	LST i0	LST i1	LST i2	L
M	BST i5	BST i6	BST i7	BST i8					GND	GND	GND	GND					LST i3	LST i4	LST i5	LST i6	M
N	BST i9	BST i10	VDD_ CORE	GND													GND	LST i7	LST i8	LST i9	N
P	BST i11	BST i12	BST i13	BST i14													LST i10	VDD _CORE	LST i11	LST i12	P
R	BST i15	BST i16	BST i17	VDD _IO													VDD _IO	LST i13	LST i14	LST i15	R
T	BST i18	BST i19	BST i20	BST i21													VDD_ CORE	LST i16	LST i17	LST i18	T
U	BST i22	IC	IC	GND	BST i28	VDD _IO	D10	GND	D4	VDD _IO	GND	VDD _PLL	GND	$\overline{FP8i}$	VDD _IO	VDD_ CORE	GND	LST i19	LST i20	LST i21	U
V	VDD_ CORE	IC	IC	BST i29	VDD_ CORE	D13	D9	D7	D3	D0	IC	IC	$\overline{C8o}$	$\overline{FP8o}$	IC	IC	LST i22	LST i23	LST i24	LST i25	V
W	BST i23	BST i24	BST i25	BST i30	D15	D12	D8	D6	D2	IC	IC	$\overline{C8i}$	$\overline{C16o}$	$\overline{FP16o}$	IC	IC	IC	LST i26	LST i27	IC	W
Y	BST i26	BST i27	IC	BST i31	D14	D11	VDD_ CORE	D5	D1	IC	VDD_ CORE	NC	NC	VDD_ CORE	IC	IC	LST i29	LST i30	LST i31	LST i28	Y

A1 corner identified by metalized marking.

Figure 2 - MT90869 PBGA Connections (272 PBGA) Pin Diagram
(as viewed through top of package)

Pin Description

Name	Package Coordinates	Description
V_{DD_IO}	D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15	**Power Supply for Periphery Circuits:** +3.3 V
V_{DD_CORE}	A7, B4, B12, D14, K1, K20, N3, P18, T17, U16, V1, V5, Y7, Y11, Y14	**Power Supply for Core Logic Circuits: +1.8 V**
V_{DD_PLL}	U12	**Power Supply for Analog PLL: +1.8 V**
$V_{SS\ (GND)}$	A1, D4, D8, D13, D17, H4, H17, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, N4, N17, U4, U8, U11, U13, U17	**Ground**
BSTi0 - 15	K3, L1, L2, L3, L4, M1, M2, M3, M4, N1, N2, P1, P2, P3, P4, R1	**Backplane Serial Input Streams 0 to 15 (5 V Tolerant, Internal pull-down).** In Non-32 Mb/s Mode, these pins accept serial TDM data streams at a data-rate of:- 16.384 Mb/s (with 256 channels per stream), 8.192 Mb/s (with 128 channels per stream), 4.096 Mb/s (with 64 channels per stream), or 2.048 Mb/s (with 32 channels per stream). The data-rate is independently programmable for each input stream. In 32 Mb/s Mode, these pins accept serial TDM data streams at a fixed data-rate of 32.768 Mb/s (with 512 channels per stream).
BSTi16 - 31	R2, R3, T1, T2, T3, T4, U1,W1, W2, W3, Y1, Y2, U5, V4, W4, Y4	**Backplane Serial Input Streams 16 to 31 (5 V Tolerant, Internal pull-down).** In Non-32 Mb/s Mode, these pins accept serial TDM data streams at a data-rate of:- 16.384 Mb/s (with 256 channels per stream), 8.192 Mb/s (with 128 channels per stream), 4.096 Mb/s (with 64 channels per stream), or 2.048 Mb/s (with 32 channels per stream). The data-rate is independently programmable for each input stream. In 32 Mb/s Mode, these pins are unused and should be externally connected to a defined logic level.

Pin Description

Name	Package Coordinates	Description
BSTo0 - 15	C5, B5, A5 C4, A4, A3, B1, B2, B3, C1, C2, D1, D2, D3, E1, E2	**Backplane Serial Output Streams 0 to 15 (5 V Tolerant, Three-state Outputs).** In Non-32 Mb/s Mode, these pins output serial TDM data streams at a data-rate of:- 16.384 Mb/s (with 256 channels per stream), 8.192 Mb/s (with 128 channels per stream), 4.096 Mb/s (with 64 channels per stream), or 2.048 Mb/s (with 32 channels per stream). The data-rate is independently programmable for each output stream. In 32 Mb/s Mode, these pins output serial TDM data streams at a fixed data-rate of 32.768 Mb/s (with 512 channels per stream). Refer to descriptions of the **BORS** and **ODE** pins for control of the output High or High-Impedance state.
BSTo16 - 31	E3, E4, F1, F2, F3, G1, G2, G3, G4, H1, H2, H3, J1, J2, J3, J4	**Backplane Serial Output Streams 16 to 31 (5 V Tolerant Three-state Outputs).** In Non-32 Mb/s Mode, these pins output serial TDM data streams at a data-rate of:- 16.384 Mb/s (with 256 channels per stream), 8.192 Mb/s (with 128 channels per stream), 4.096 Mb/s (with 64 channels per stream), or 2.048 Mb/s (with 32 channels per stream). The data-rate is independently programmable for each output stream. These pins are unused when the 32 Mb/s Mode is selected. Refer to descriptions of the **BORS** and **ODE** pins for control of the output High or High-Impedance state.
BCSTo0-3	C14, A15, B15, C15	**Backplane Output Channel High Impedance Control (5 V Tolerant Three-state Outputs).** Active high output enable which may be used to control external buffering individually for a set of backplane output streams on a per channel basis. In non-32 Mb/s mode (stream rates 2 Mb/s to 16 Mb/s): BCSTo0 is the output enable for BSTo[0,4,8,12,16,20,24,28], BCSTo1 is the output enable for BSTo[1,5,9,13,17,21,25,29], BCSTo2 is the output enable for BSTo[2,6,10,14,18,22,26,30], BCSTo3 is the output enable for BSTo[3,7,11,15,19,23,27,31]. In 32 Mb/s mode (stream rate 32 Mb/s): BCSTo0 is the output enable for BSTo[0,4,8,12], BCSTo1 is the output enable for BSTo[1,5,9,13], BCSTo2 is the output enable for BSTo[2,6,10,14], BCSTo3 is the output enable for BSTo[3,7,11,15]. Refer to descriptions of the **BORS** and **ODE** pins for control of the output High or High-Impedance state.

Pin Description

Name	Package Coordinates	Description
$\overline{FP8i}$	U14	**Frame Pulse Input (5 V Tolerant).** This pin accepts the Frame Pulse signal. The pulse width may be active for 122 ns or 244 ns at the frame boundary and the Frame Pulse Width bit (FPW) of the Control Register must be set Low (default) for a 122 ns and set High for a the 244 ns pulse condition.The device will automatically detect whether an **ST-BUS** or **GCI-BUS** style frame pulse is applied.
$\overline{C8i}$	W12	**Master Clock Input (5 V Tolerant).** This pin accepts a 8.192 MHz clock. The internal Frame Boundary is aligned with the rising edge of this clock. This rising edge frame boundary alignment is controlled by the C8IPOL bit in the Control Register as shown in Table 16 on page 51. The C8IPOL bit MUST be set to ONE for the rising edge frame boundary to be detected correctly. Falling C8i edge frame boundary alignment is not supported and should not be used.
$\overline{CS}$	B11	**Chip Select (5 V Tolerant).** Active low input used by the microprocessor to enable the microprocessor port access. This input is internally set low during a device $\overline{RESET}$.
$\overline{DS}$	A11	**Data Strobe (5 V Tolerant).** This active low input works in conjunction with $\overline{CS}$ to enable the microprocessor port read and write operations.
R/$\overline{W}$	C11	**Read/Write (5 V Tolerant).** This input controls the direction of the data bus lines (D0-D15) during a microprocessor access.
A0 - A14	D5, C6, A6, D7, C7, B7, C8, B8, A8, D9, B9, A9, D10, C10, A10	**Address 0 - 14 (5 V Tolerant).** These pins form the 15-bit address bus to the internal memories and registers. A0 = LSB
D0 - D15	V10, Y9, W9, V9,U9, Y8, W8, V8, W7, V7, U7, Y6, W6, V6, Y5, W5	**Data Bus 0 - 15 (5 V Tolerant).** These pins form the 16-bit data bus of the microprocessor port. D0 = LSB
$\overline{DTA}$	A13	**Data Transfer Acknowledgment (5 V Tolerant).** This active low output indicates that a data bus transfer is complete. A pull-up resistor is required to hold a HIGH level. (Max. I_{OL} = 10 mA).
TMS	D12	**Test Mode Select (5 V Tolerant with internal pull-up).** JTAG signal that controls the state transitions of the TAP controller.
TCK	A14	**Test Clock (5 V Tolerant).** Provides the clock to the JTAG test logic.
TDi	B13	**Test Serial Data In (5 V Tolerant with internal pull-up).** JTAG serial test instructions and data are shifted in on this pin.
TDo	C13	**Test Serial Data Out (5 V Tolerant Three-state Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG is not enabled.
$\overline{TRST}$	B14	**Test Reset (5 V Tolerant with internal pull-up)** Asynchronously initializes the JTAG TAP controller to the Test-Logic-Reset state. To be pulsed low during power-up for JTAG testing. This pin must be held LOW for normal functional operation of the device.
$\overline{RESET}$	C12	**Device Reset (5 V Tolerant with internal pull-up).** This input (active LOW) asynchronously applies reset and synchronously releases reset to the device. In the reset state, the outputs LSTo0 - 31 and BSTo0 - 31 are set to a high or high impedance depending on the state of the LORS and BORS external control pins, respectively. It clears the device registers and internal counters. This pin must stay low for more than 2 cycles of input clock C8i for the reset to be invoked.

Pin Description

Name	Package Coordinates	Description
LSTi0-31	L18, L19, L20, M17, M18, M19, M20, N18, N19, N20, P17, P19, P20, R18, R19, R20, T18, T19, T20, U18, U19, U20, V17, V18, V19, V20, W18, W19, Y20, Y17, Y18, Y19	**Local Serial Input Streams 0 to 31 (5 V Tolerant with internal pull-down).** These pins accept serial TDM data streams at a data-rate of:- 16.384 Mb/s (with 256 channels per stream), 8.192 Mb/s (with 128 channels per stream), 4.096 Mb/s (with 64 channels per stream), or 2.048 Mb/s (with 32 channels per stream). The data-rate is independently programmable for each input stream.
$\overline{\text{C16o}}$	W13	**$\overline{\text{C16o}}$ Output Clock (Three-state Output).** A 16.384 MHz clock output. The clock falling edge or rising edge is aligned with the local frame boundary, this is controlled by the COPOL bit of the Control Register.
$\overline{\text{C8o}}$	V13	**$\overline{\text{C8o}}$ Output Clock (Three-state Output).** A 8.192 MHz clock output. The clock falling edge or rising edge is aligned with the local frame boundary, this is controlled by the COPOL bit of the Control Register.
$\overline{\text{FP16o}}$	W14	**Frame Pulse Output (Three-state Output).** Frame pulse output is active for 61ns at the frame boundary. The frame pulse, running at a 8 KHz rate, will be the same format (ST-BUS or GCI-BUS) as the input frame pulse (FP8i).
$\overline{\text{FP8o}}$	V14	**Frame Pulse Output (Three-state Output).** Frame pulse output is active for 122 ns at the frame boundary. The frame pulse, running at 8 KHz rate, will be the same style (ST-BUS or GCI-BUS) as the input frame pulse (FP8i).
LSTo0 - 31	A17, A18, A19, B18, B19, B20, C18, C19, C20, D18, D19, D20, E17, E18, E19, E20, F18, F19, F20, G17, G18, G19, G20, H18, H19, H20, J17, J18, J19, J20, K17, K18	**Local Serial Output Streams 0 to 31 (5 V Tolerant Three-state Outputs).** These pins output serial TDM data streams at a data-rate of:- 16.384 Mb/s (with 256 channels per stream), 8.192 Mb/s (with 128 channels per stream), 4.096 Mb/s (with 64 channels per stream), or 2.048 Mb/s (with 32 channels per stream). The data-rate is independently programmable for each output stream. Refer to descriptions of the **LORS** and **ODE** pins for control of the output High or High-Impedance state.
LCSTo0-3	C17, C16, B16, A16	**Local Output Channel High Impedance Control (5 V Tolerant Three-state Outputs).** Active high output enable which may be used to control external buffering individually for a set of local output streams on a per channel basis. LCSTo0 is the output enable for LSTo[0,4,8,12,16,20,24,28], LCSTo1 is the output enable for LSTo[1,5,9,13,17,21,25,29], LCSTo2 is the output enable for LSTo[2,6,10,14,18,22,26,30], LCSTo3 is the output enable for LSTo[3,7,11,15,19,23,27,31]. Refer to descriptions of the **LORS** and **ODE** pins for control of the output High or High-Impedance state.

Pin Description

Name	Package Coordinates	Description
ODE	A12	**Output Drive Enable (5 V Tolerant, Internal pull-up).** An asynchronous input providing Output Enable control to the BSTo0- 31, LSTo0-31, BCSTo0-3 and LCSTo0-3 outputs. When LOW, the BSTo0-31 and LSTo0- 31 outputs are driven high or high impedance (dependent on the **BORS** and **LORS** pin settings respectively) and the outputs BCSTo0-3 and LCSTo0-3 are driven low. When HIGH, the outputs BSTo0- 31, LSTo0-31, BCSTo0-3 and LCSTo0-3 are enabled.
BORS	K2	**Backplane Output Reset State (5 V Tolerant, Internal pull-down).** When this input is LOW the device will initialize with the BSTo0-31 outputs driven high, and the BCSTo0-3 outputs driven low. Following initialization, the Backplane stream outputs are always active and a high impedance state, if required on a per-channel basis, may be implemented with external buffers controlled by outputs BCSTo0-3. When this input is HIGH, the device will initialize with the BSTo0-31 outputs at high impedance and the BCSTo0-3 outputs driven low. Following initialization, the Backplane stream outputs may be set active or high impedance using the **ODE** pin or on a per-channel basis with the **BE** bit in Backplane Connection Memory.
LORS	K19	**Local Output Reset State (5 V Tolerant, Internal pull-down).** When this input is LOW, the device will initialize with the LSTo0-31 outputs driven high and the LCSTo0-3 outputs driven low. Following initialization, the Local stream outputs are always active and a high impedance state, if required on a per-channel basis, may be implemented with external buffers controlled by the LCSTo0-3. When this input is HIGH, the device will initialize with the LSTo0-31 outputs at high impedance and the LCSTo0-3 driven low. Following initialization, the Local stream outputs may be set active or high impedance using the **ODE** pin or on a per-channel basis with the **LE** bit in Local Connection Memory.
NC	Y12, Y13	No Connect No connection to be made.
IC0	A2, A20, B6, B10, B17, C3, C9, D16, U2, U3, V2, V3, V11, V12, V15, V16, W10, W11, W15, W16, W17, W20, Y3, Y10, Y15, Y16	Internal Connects These inputs MUST be held LOW.

1.0 Bidirectional and Unidirectional Switching Applications

The MT90869 has a maximum capacity of 16,384 input channels and 16,384 output channels. This is calculated from the maximum number of streams and channels: 64 input streams (32 backplane, 32 local) at 16.384 Mb/s and 64 output streams (32 backplane, 32 local) at 16.384 Mb/s.

One typical mode of operation is to separate the Backplane and Local sides, as shown in Figure 3 below.

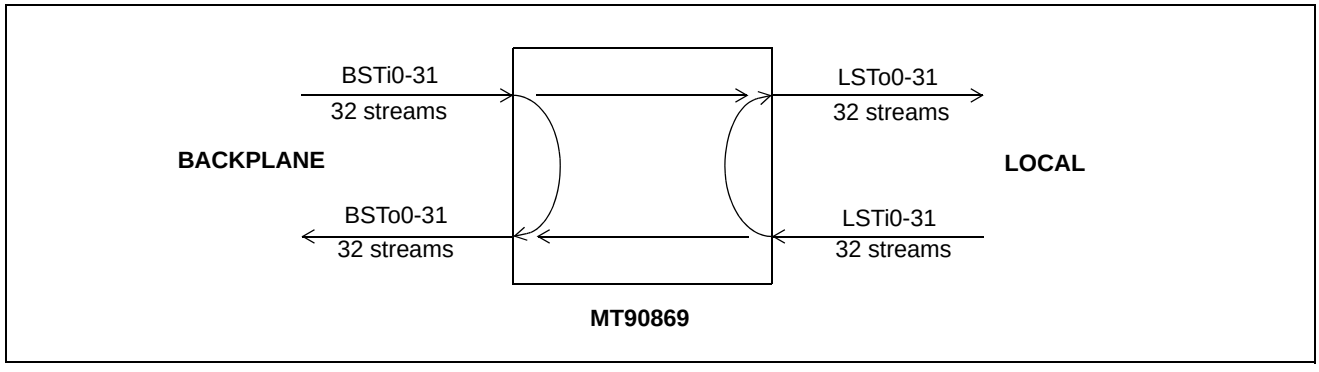


Figure 3 - 8,192 x 8,192 Channels (16 Mb/s), Bidirectional Switching

In this system setup, the chip has a capacity of 8,192 input channels and 8,192 output channels on the Backplane side as well as 8,192 input channels and 8,192 output channels on the Local side. Note that some or all of the output channels on one side can come from the other side, i.e., Backplane input to Local output switching.

Often a system design does not need to differentiate between a Backplane and Local side, and merely needs maximum switching capacity. In this case, the MT90869 can be used as shown in Figure 4 to give the full 16,384 x 16,384 channel capacity.

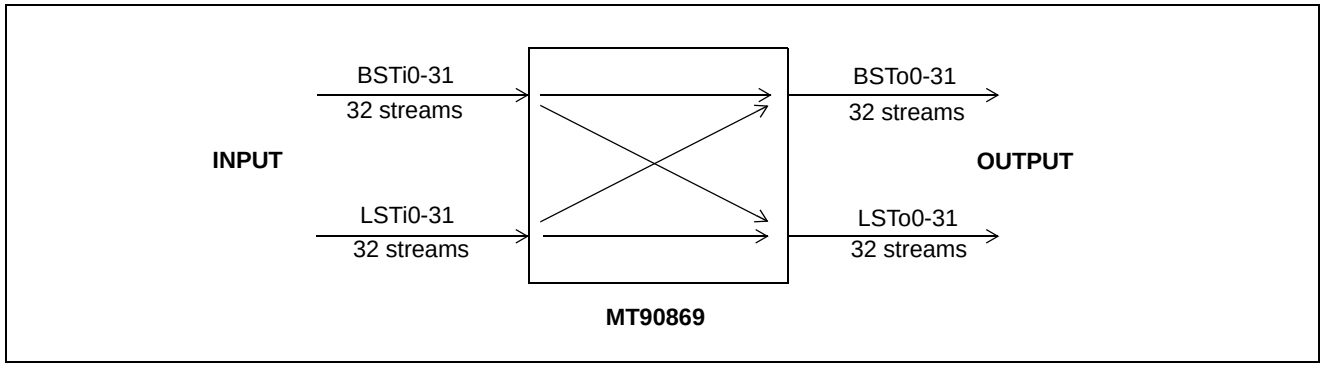


Figure 4 - 16,384 x 16,384 Channels (16 Mb/s), Unidirectional Switching

In this system, the Backplane and Local inputs and outputs are combined so that the switch appears as a 64 stream input by 64 stream output switch. This style of operation is similar to older switch designs, such as the MT90826.

Note, in either configuration the Backplane may be operated in the 32 Mb/s Mode, providing 512 channels on each of the 16 available input and output streams (BSTi0-15 and BSTo0-15) operating at a data-rate of 32.768 Mb/s, in conjunction with the Local streams (LSTi0-31 and LSTo0-31) operated at 16.384 Mb/s. This allows data-rate conversion between 32.768 Mb/s and 16.384 Mb/s without loss to the switching capacity.

1.1 Flexible Configuration

The F16KDX can be configured as an 8 K by 8 K non-blocking bi-directional digital switch, a 16 K by 16 K unidirectional non-blocking digital switch, and as a blocking switch with various switching capacities.

A. Non-Blocking Bi-directional Configuration (Typical System Configuration)

- 8,192-channel x 8,192-channel non-blocking switching from backplane to local streams
- 8,192-channel x 8,192-channel non-blocking switching from local to backplane streams
- 8,192-channel x 8,192-channel non-blocking switching from backplane input to backplane output streams
- 8,192-channel x 8,192-channel non-blocking switching from local input to local output streams

B. Unidirectional Configuration

Because the input and output drivers are synchronous, the user can combine input backplane streams and input local streams or output backplane streams and output local streams to increase the total number of input and output streams of the switch in a unidirectional configuration.

- 16,384-channel x 16,384-channel non-blocking switching from input to output streams

C. Blocking Configuration

The F16KDX can be configured as a blocking bi-directional switch if it is an application requirement. For example, it can be configured as a 12 k by 4 K blocking switch:

- 12,288-channel x 4,096-channel blocking switching from "backplane" to "local" streams
- 4,096-channel x 12,288-channel blocking switching from "local" to "backplane" streams
- 12,288-channel x 12,288-channel non-blocking switching from "backplane" input to "backplane" output streams
- 4,096-channel x 4,096-channel non-blocking switching from "local" input to "local" output streams

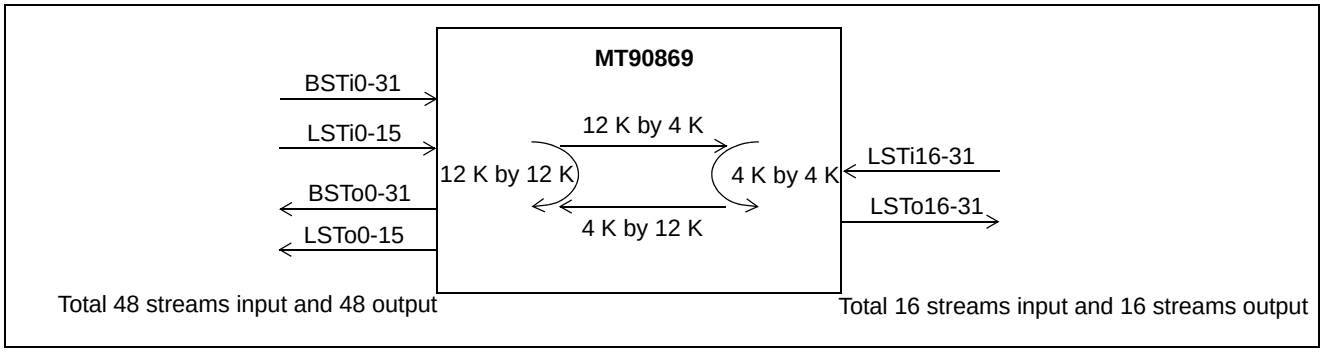


Figure 5 - 12 K by 4 K Blocking Configuration

2.0 Functional Description

2.1 Switching Configuration

The device supports five switching configurations. (1) Backplane-to-Local, (2) Local-to-Backplane, (3) Backplane-to-Backplane, (4) Local-to-Local, and (5) Uni-directional switch. The following sections describe the switching paths in detail. Configurations (1) - (4) enable a non-blocking switch with 8192 input channels and 8192 output channels at Backplane stream data-rates of 16.384 Mb/s or 32.768 Mb/s, and Local stream data-rates of 16.384 Mb/s. The switch paths of Configurations (1) to (4) may be operated simultaneously.

2.1.1 Backplane-to-Local Path

The device can provide data switching between the Backplane input port and the Local output port. The Local Connection Memory determines the switching configurations.

2.1.2 Local-to-Backplane Path

The device can provide data switching between the Local input port and the Backplane output port. The Backplane Connection Memory determines the switching configurations.

2.1.3 Backplane-to-Backplane Path

The device can provide data switching between the Backplane input and output ports. The Backplane Connection Memory determines the switching configurations.

2.1.4 Local-to-Local Path

The device can provide data switching between the Local input and output ports. The Local Connection Memory determines the switching configurations.

2.1.5 Uni-directional Switch

The device may be optionally configured to provide a 16,384 x 16,384 uni-directional switch by grouping together all input and all output streams. All streams may be operated at a data-rate of 16.384 Mb/s, or a combination of 16.384 Mb/s and 32.768 Mb/s. Lower data-rates may be employed with a corresponding reduction in switch capacity.

2.2 Port Data Rate Modes and Selection

The selection of individual stream data-rates is summarized in Table 1.

2.2.1 Local Port Rate Selection

The local port has 32 input (LSTi0-31) and 32 output (LSTo0-31) data streams. All input and output streams may be individually selected for operation at a data rate of either 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s. The timing of the input and output clocks and frame pulses are shown in Figure 6, Local Port Timing Diagram for 2,4,8 and 16 Mb/s stream rates.

2.2.1.1 Local Input Port

The bit rate for each input stream is selected by writing to a dedicated Local Input Bit Rate Register (LIBRR0-31). Refer to Local Input Bit Rate Register (LIBRRn) Bits.

Stream Number	Rate Selection Capability (for each individual stream)
Input stream - Backplane 0-15 (BSTi0-15)	2.048, 4.096, 8.192 or 16.384 Mb/s - Non-32 Mb/s Mode 32.768 Mb/s - 32 Mb/s Mode
Input stream - Backplane 16-31 (BSTi16-31)	2.048, 4.096, 8.192 or 16.384 Mb/s - Non-32 Mb/s Mode Unused - 32 Mb/s Mode
Output stream - Backplane 0-15 (BSTo0-15)	2.048, 4.096, 8.192 or 16.384 Mb/s - Non-32 Mb/s Mode 32.76 8Mb/s - 32 Mb/s Mode
Output stream - Backplane 16-31 (BSTo16-31)	2.048, 4.096, 8.192 or 16.384 Mb/s - Non-32 Mb/s Mode Unused - 32 Mb/s Mode
Input stream - Local 0-31 (LSTi0-31)	2.048, 4.096, 8.192 or 16.384 Mb/s
Output stream - Local 0-31 (LSTo0-31)	2.048, 4.096, 8.192 or 16.384 Mb/s

Table 1 - Per-stream Data-Rate Selection: Backplane and Local, Non-32 Mb/s Mode and 32 Mb/s Mode

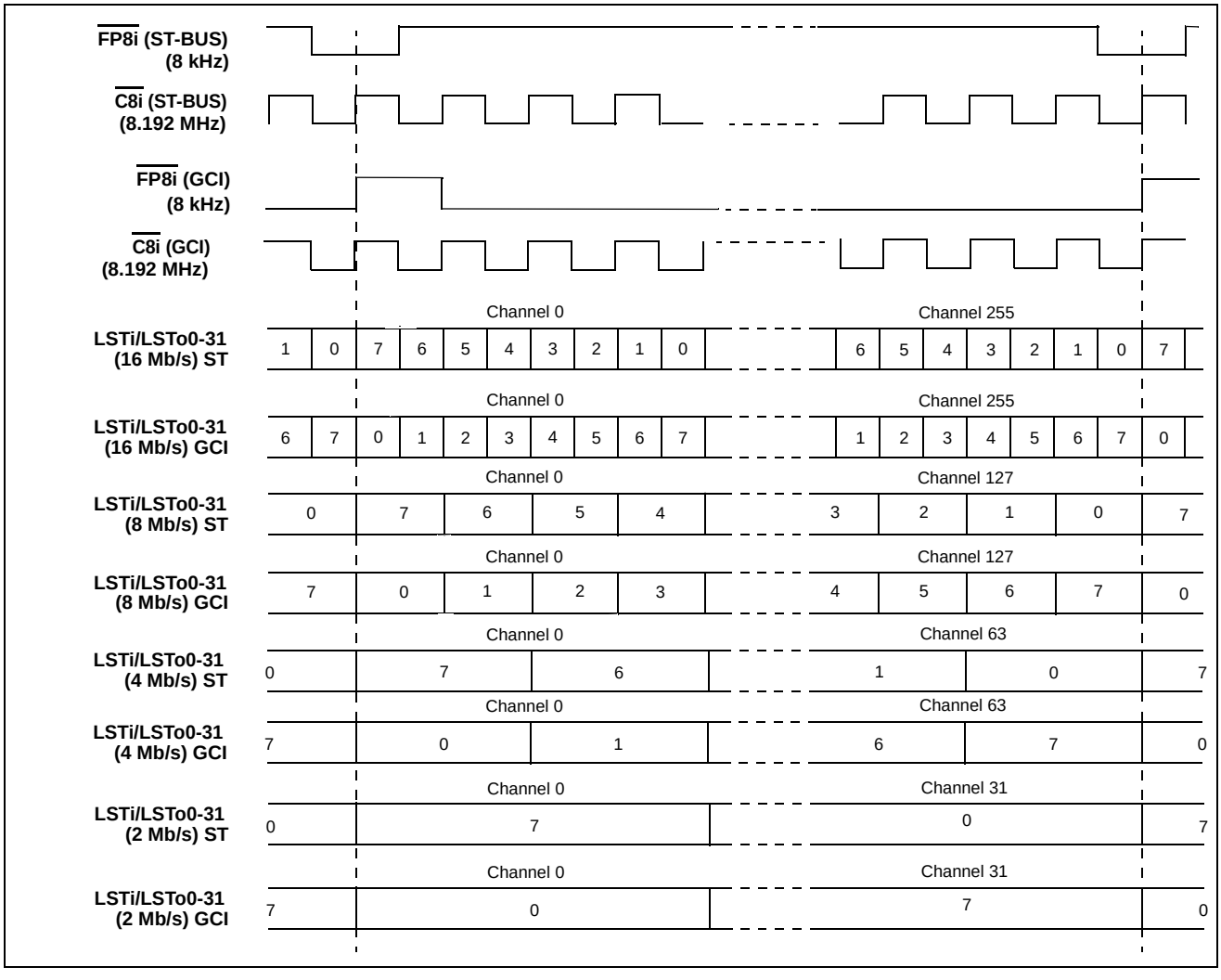


Figure 6 - Local Port Timing Diagram for 2,4,8 and 16 Mb/s stream rates

2.2.1.2 Local Output Port

The bit rate for each output stream is selected by writing to a dedicated Local Output Bit Rate Register (LOBRR0-31). Refer to Local Output Bit Rate Register (LOBRRn) Bits.

Operation of stream data in the Connection Mode or the Message Mode is determined by the state of the LMM bit, and the channel High-impedance state controlled by the LE bit of the Local Connection Memory. The data source (i.e. from the Local or Backplane Data Memory) is determined by the LSRC bit of the Local Connection Memory. Refer to Section 6.1, Local Connection Memory, and Section 12.3, Local Connection Memory Bit Definition.

2.2.2 Backplane Port Rate Selection

The Backplane streams may be operated in one of two modes, namely Non-32 Mb/s Mode and 32 Mb/s Mode. The Local stream data-rates are not affected by the operating mode of the Backplane. The operating mode of the Backplane is determined by setting the Control Register bit, MODE32. Setting the bit HIGH will invoke the 32 Mb/s Mode. Setting the bit LOW will invoke the Non-32 Mb/s mode. The default bit value on device Reset is LOW. The timing of the input and output clocks and frame pulses are shown in Figure 7, Backplane Port Timing Diagram for 2, 4, 8, 16 and 32 Mb/s stream rates.

Non-32 Mb/s Mode: Each of the 32 Backplane streams (BSTi0-31 and BSTo0-31) and Local streams (LSTi0-31 and LSTo0-31) can be independently programmed for a data-rate of 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s.

32 Mb/s Mode: 16 of the Backplane input streams (BSTi0-15) and 16 Backplane output (BSTo0-15) streams operate at a fixed rate of 32.768 Mb/s. In this mode, the upper 16 input (BSTi16-31) and 16 output (BSTi16-31) streams are unused. All 32 Local streams can be independently programmed for a data-rate of 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s.

2.2.2.1 Backplane Input Port

The bit rate for each input stream is selected by writing to a dedicated Backplane Input Bit Rate Register (BOBRR0-31). Refer to Backplane Input Bit Rate Register (BIBRRn) Bits. If the 32 Mb/s mode is selected by writing to the Control Register bit (MODE32), the settings in BIBRRn are ignored.

2.2.2.2 Backplane Output Port

The bit rate for each output stream is selected by writing to a dedicated Backplane Output Bit Rate Register (BOBRR0-31). Refer to Backplane Output Bit Rate Register (BOBRRn) Bits. If the 32 Mb/s mode is selected by writing to the Control Register bit (MODE32), the settings in BOBRRn are ignored.

Operation of stream data in the Connection Mode or the Message Mode is determined by the state of the BMM bit, and the channel High-impedance state controlled by the BE bit of the Backplane Connection Memory. The data source (i.e., from the Local or Backplane Data Memory) is determined by the BSRC bit of the Backplane Connection Memory. Refer to Section 6.2, Backplane Connection Memory and Section 12.4, Backplane Connection Memory Bit Definition.

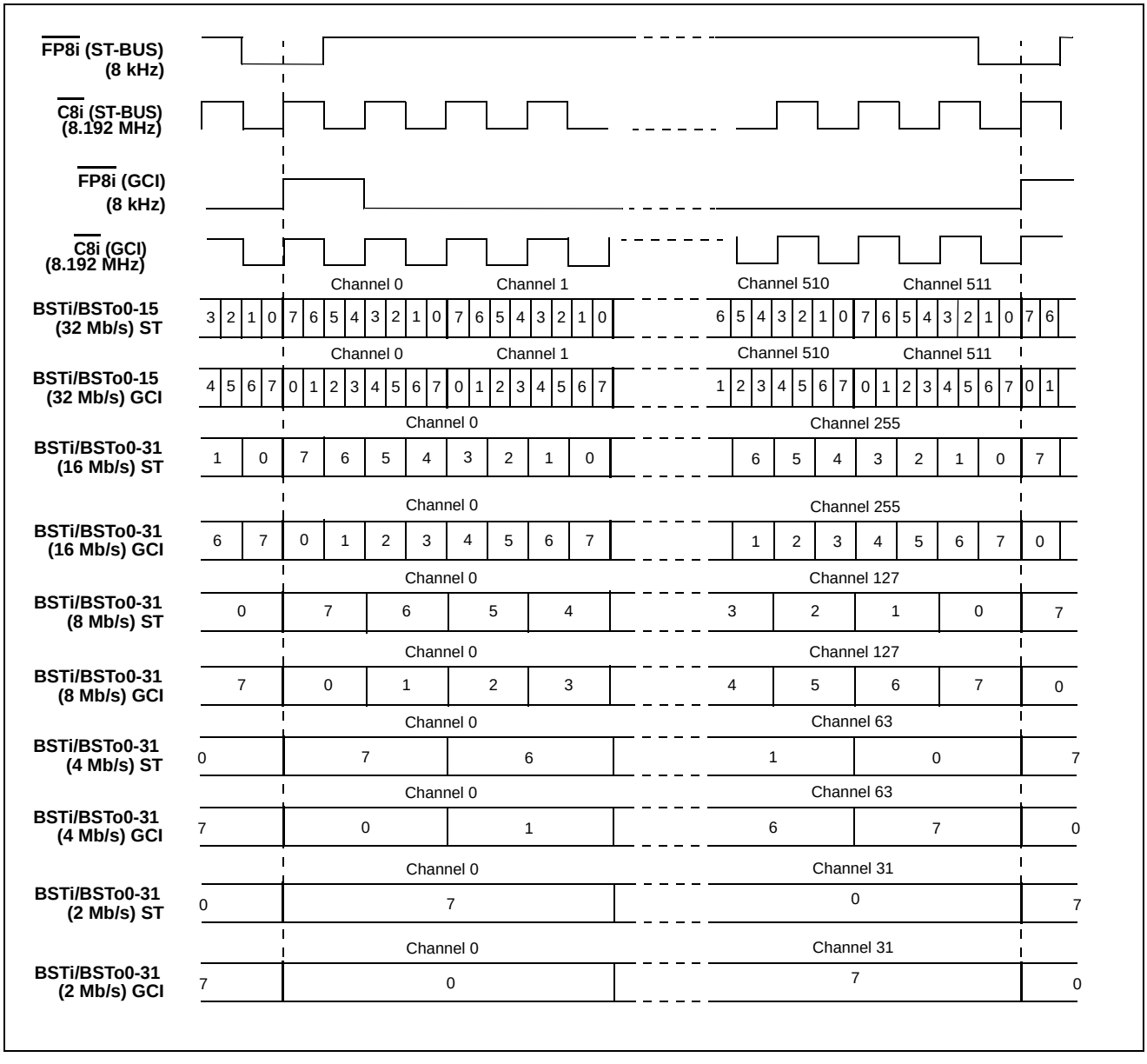


Figure 7 - Backplane Port Timing Diagram for 2, 4, 8, 16 and 32 Mb/s stream rates

2.3 Backplane Frame Pulse Input and Master Input Clock Timing

The Backplane frame pulse ($\overline{\text{FP8i}}$) is an 8 kHz input signal active for 122 ns or 244 ns at the frame boundary. The FPW bit in the Control Register must be set according to the applied pulse width. See Pin Description and Control Register Bits, for details.

The active state and timing of $\overline{\text{FP8i}}$ may conform either to the ST-BUS or to the GCI-BUS as shown in Figure 6, Local Port Timing Diagram for 2,4,8 and 16 Mb/s stream rates, and Figure 7, Backplane Port Timing Diagram for 2, 4, 8, 16 and 32 Mb/s stream rates. The MT90869 will automatically detect whether an ST-BUS or a GCI-BUS style frame pulse is being used for the master frame pulse ($\overline{\text{FP8i}}$). The device will detect the frame boundary alignment using the rising edge of the input clock ($\overline{\text{C8i}}$), provided the C8IPOL bit in Table 16, “Control Register Bits,” on page 51 is set to one. Before the C8IPOL bit is set to one, the frame boundary will not be detected correctly. For the

purposes of describing the device operation, the remaining part of this document assumes the ST-BUS style frame pulse with a single width frame pulse of 122 ns and the C8IPOL bit is set to one unless explicitly stated otherwise.

In addition, the device provides FP8o, FP16o, C8o and C16o outputs to support external devices which connect to the local port. The local frame pulses (FP8o, FP16o) will be provided in the same style as the master frame pulse (FP8i). The polarity of C8o and C16o, at the Frame Boundary, can be controlled by the Control Register bit, COPOL. An analog phase lock loop (APLL) is used to multiply the external clock frequency to generate an internal clock signal operated at 131.072 MHz.

2.4 Backplane Frame Pulse Input and Local Frame Pulse Output Alignment

The MT90869 accepts a Backplane Frame Pulse (FP8i) and generates the Local Frame Pulse outputs, FP8o and FP16o, which are aligned to the master frame pulse. There is a constant three frame delay for data being switched. Figure 8, Backplane and Local Frame Pulse Alignment for Data Rates of 2 Mb/s, 4 Mb/s, 8 Mb/s and 16 Mb/s, shows the backplane and local frame pulse alignment for different data rates.

For further details of Frame Pulse conditions and options see Section 13.1, Control Register (CR), Figure 18, Frame Boundary Conditions, ST- BUS Operation, and Figure 19, Frame Boundary Conditions, GCI - BUS Operation.

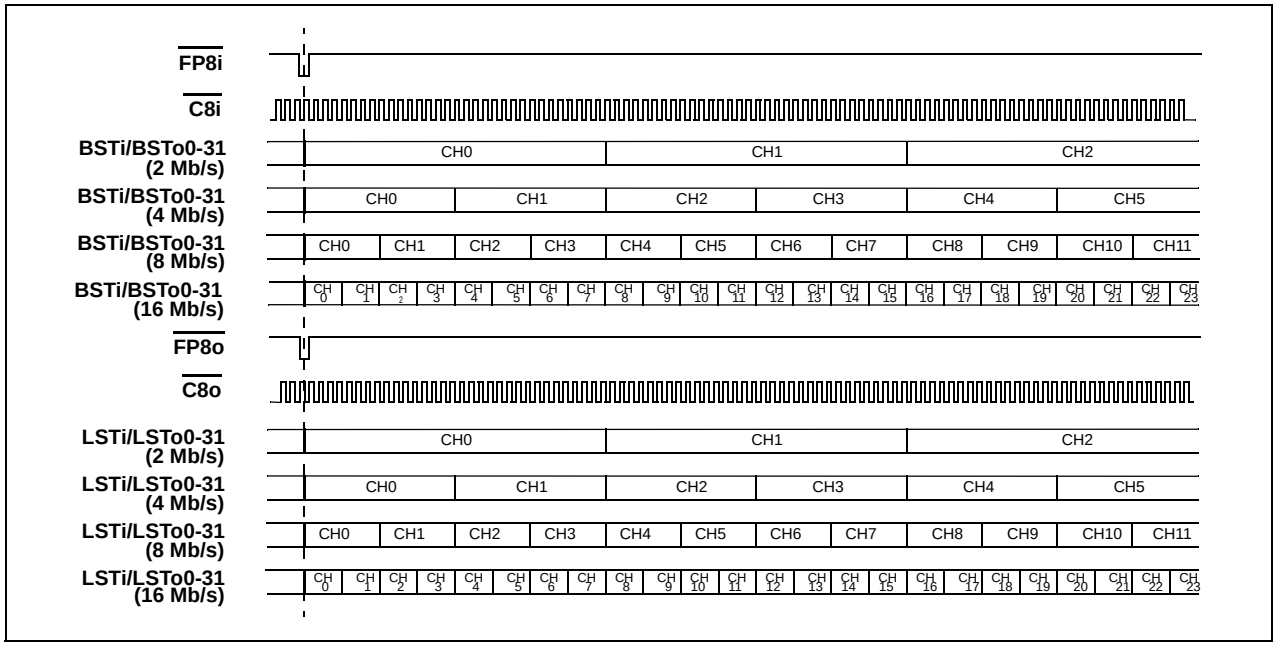


Figure 8 - Backplane and Local Frame Pulse Alignment for Data Rates of 2 Mb/s, 4 Mb/s, 8 Mb/s and 16 Mb/s

3.0 Input and Output Offset Programming

3.1 Input Channel Delay Programming (Backplane and Local Input Streams)

Various registers are used to control the input sampling point (delay) and the output advancement for the Local and Backplane streams. The following sections explain the details of these offset programming features.

The control of the Input Channel Delay and the Input Bit Delay allows each input stream to have a different frame boundary with respect to the master frame pulse, FP8i. By default, all input streams have channel delay of zero such that Ch0 is the first channel that appears after the frame boundary.

By programming the Backplane or Local input channel delay registers, BCDR0-31 and LCDR0-31, users can assign the Ch0 position to be located at any one of the channel boundaries in a frame. For delays within channel boundaries, the input bit delay programming can be used.

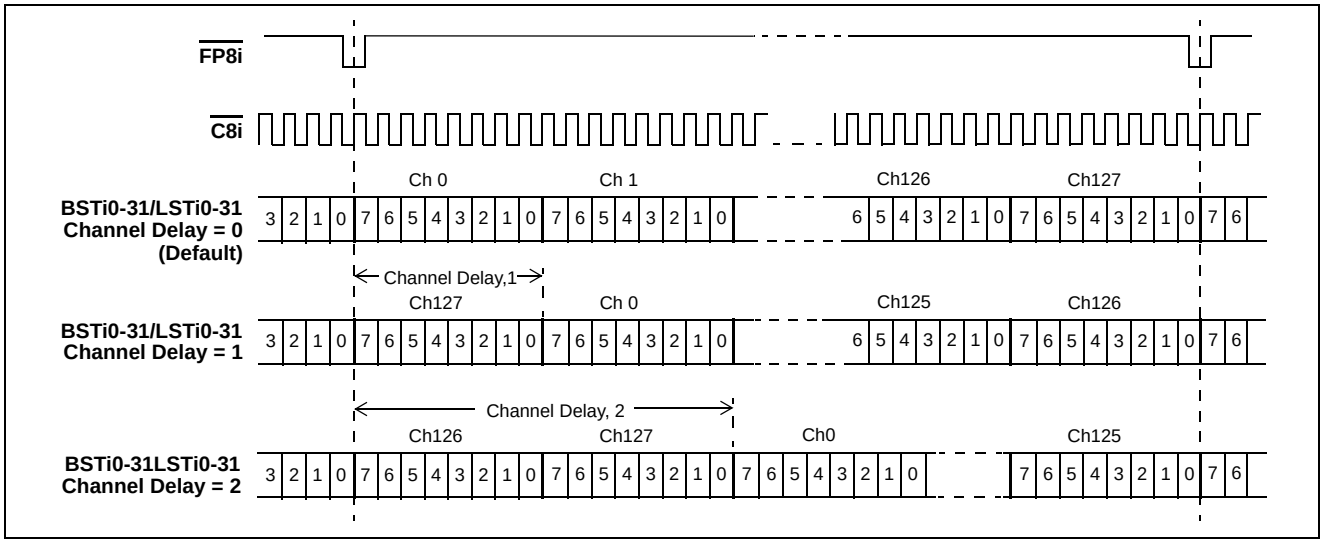


Figure 9 - Backplane and Local Input Channel Delay Timing Diagram

The use of Input Channel Delay in combination with Input Bit Delay enables the Ch0 position to be placed anywhere within a frame to a resolution of 1/4 of the bit period.

3.2 Input Bit Delay Programming (Backplane and Local Input Streams)

In addition to the Input Channel Delay programming, the Input Bit Delay programming feature provides users with greater flexibility when designing switch matrices for high speed operation. The input bit delay may be programmed on a per-stream basis to accommodate delays created on PCM highways. For all streams the delay is up to 7 3/4 bits with a resolution of 1/4 bit, for the selected data-rate.

See Figure 10 and Figure 11 for Input Bit Delay Timing at 16 Mb/s and 8 Mb/s data rates, respectively.

The local input delay is defined by the Local Input Delay registers, LIDR0 to LIDR31, corresponding to the local data streams, LSTi0 to LSTi31, and the backplane input delay is defined by the Backplane Input Delay registers, BIDR0 to BIDR31, which correspond to the backplane data streams, BSTi0 to BSTi31.

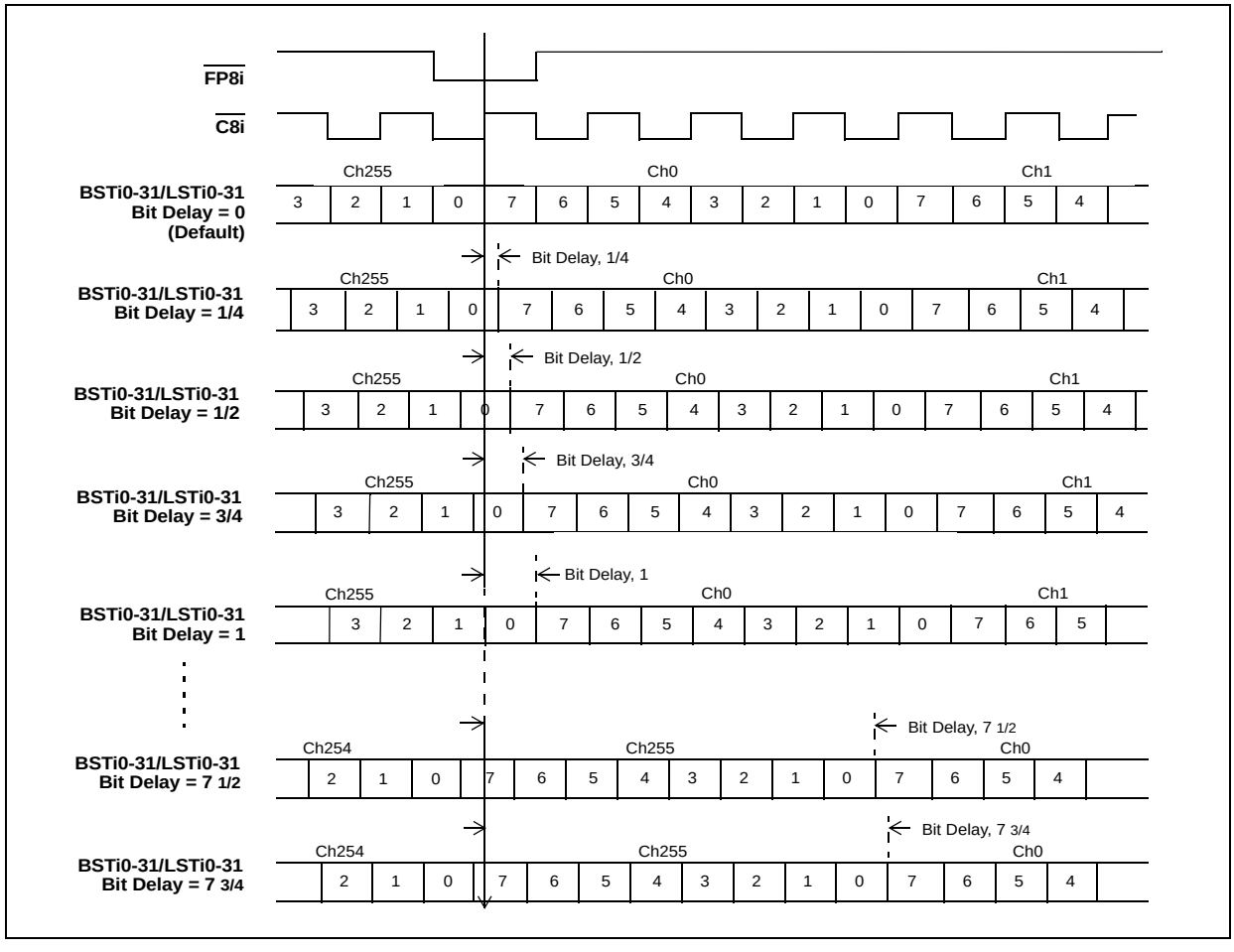


Figure 10 - Backplane and Local Input Bit Delay Timing Diagram for Data Rate of 16 Mb/s

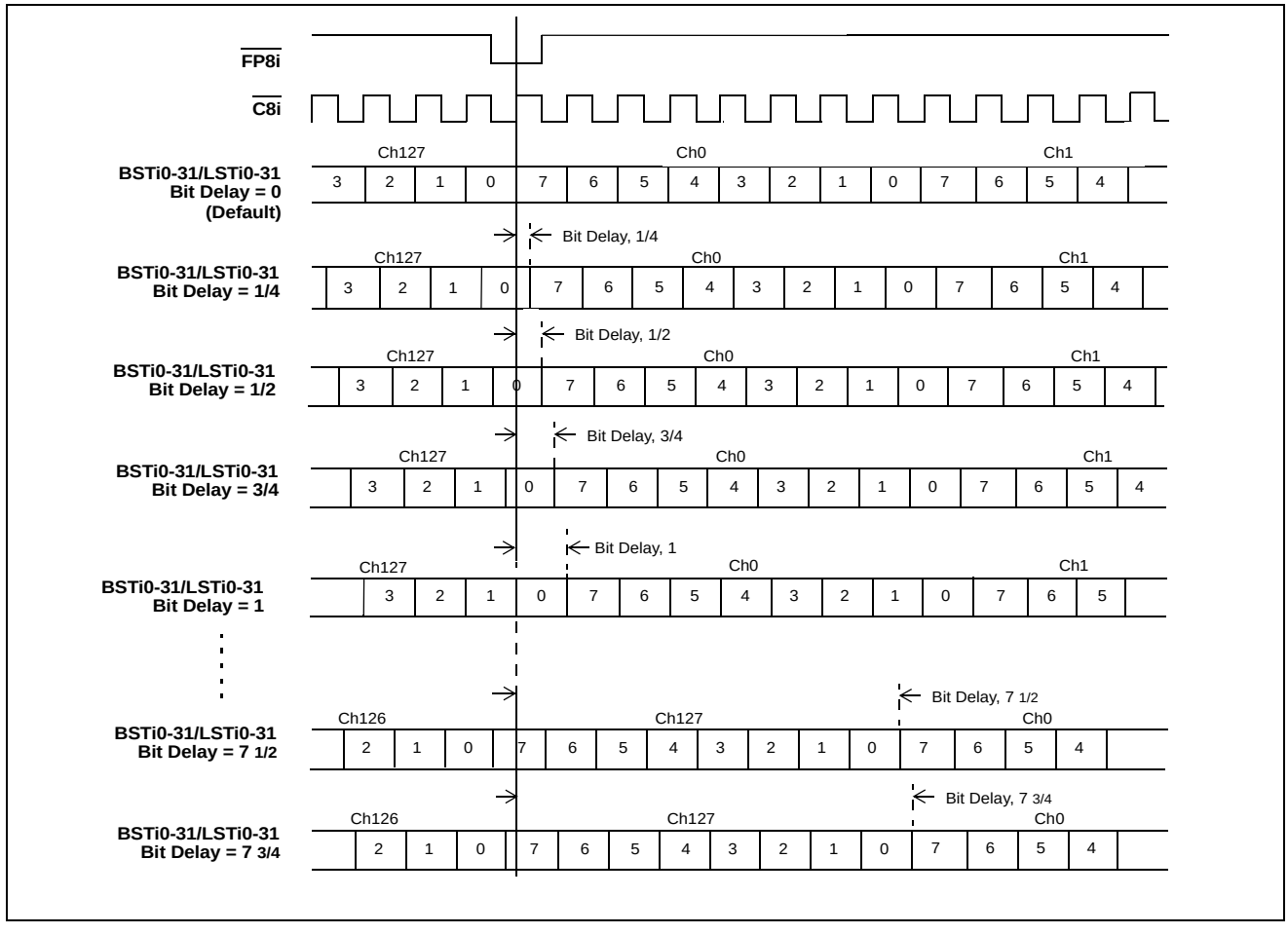


Figure 11 - Backplane and Local Input Bit Delay Timing Diagram for Data Rate of 8 Mb/s

3.3 Output Advancement Programming (Backplane and Local Output Streams)

This feature is used to advance the output channel alignment of individual local or backplane output streams with respect to the frame boundary. Each output stream has its own advancement value which can be programmed by the output advancement registers. The output advancement selection is useful in compensating for various parasitic loading on the serial data output pins.

3.3.1 Local Output Advancement Programming

The local output advancement registers, **LOAR0-31**, are used to control the local output advancement. The advancement is determined with reference to the internal system clock rate (131.072 MHz). For 2 Mb/s, 4 Mb/s, 8 Mb/s or 16 Mb/s streams the advancement may be 0, -2 cycles, -4 cycles or -6 cycles, which converts to approximately 0ns, -15 ns, -30 ns or -45 ns as shown in Figure 12.

3.3.2 Backplane Output Advancement Programming

The backplane output advancement registers, **BOAR0-31** are used to control the backplane output advancement. The advancement is determined with reference to the internal system clock rate (131.072 MHz). For 2 Mb/s, 4 Mb/s, 8 Mb/s or 16 Mb/s streams the advancement may be 0, -2 cycles, -4 cycles or -6 cycles, which converts to

approximately 0ns, -15 ns, -30 ns or -45 ns as shown in Figure 12. For 32 Mb/s streams, the advancement may be 0, -1 cycle, -2 cycles or -3 cycles, which converts to approximately 0ns, -7 ns, -15 ns or -22 ns.

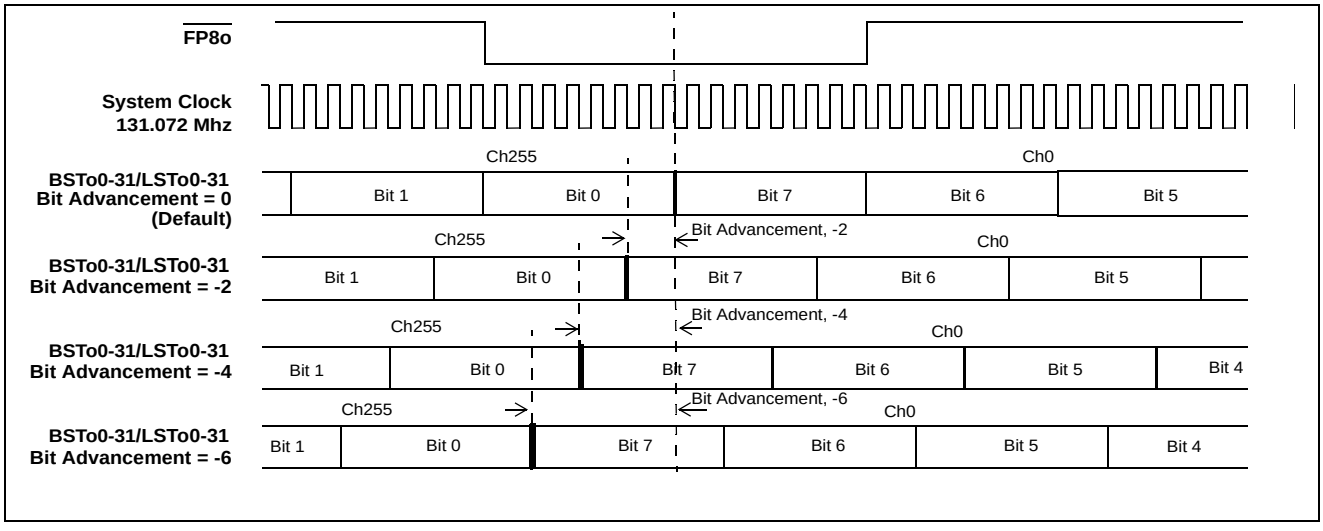


Figure 12 - Backplane and Local Output Advancement Timing diagram for Data Rate of 16 Mb/s

4.0 Port High Impedance Control

4.1 Local Port High Impedance Control

The input pin, **LORS**, selects whether the Local output streams, **LSTo0-31** are set to high impedance at the output of the MT90869 itself, or are always driven (active HIGH or active LOW) and a high impedance state, if required on a per-channel basis, is invoked through an external interface circuit controlled by the **LCSTo0-3** signals. Setting **LORS** to a LOW state will configure the output streams, **LSTo0-31,** to transmit bi-state channel data with per-channel high-impedance determined by external circuits under the control of the **LCSTo0-3** outputs. Setting **LORS** to a HIGH state will configure the output streams, **LSTo0-31,** of the MT90869 to invoke a high-impedance output on a per-channel basis.

The state of the **LORS** pin is detected and the MT90869 configured accordingly during a **$\overline{\text{RESET}}$** operation, e.g. following power-up. The LORS pin is asynchronous input and is expected to be hard-wired for a particular system application, although it may be driven under logic control if preferred.

4.1.1 LORS Set LOW

The data (channel control bit) transmitted by **LCSTo0-3** replicates the Local Output Enable Bit (**LE**) of the Local Connection Memory, with a LOW state indicating the channel to be set to High Impedance. See **Section 12.3, Local Connection Memory Bit Definition** for setting the Local Output Enable Bit (**LE**).

The **LCSTo0-3** outputs transmit serial data (channel control bits) at 16.384 Mb/s, with each bit representing the per-channel high impedance state for specific streams. Eight output streams are allocated to each control line as follows:

(See also **Pin Description**)

- LCSTo0 outputs the channel control bits for streams LSTo0, 4, 8, 12, 16, 20, 24 and 28.
- LCSTo1 outputs the channel control bits for streams LSTo1, 5, 9, 13, 17, 21, 25 and 29.

- LCSTo2 outputs the channel control bits for streams LSTo2, 6, 10, 14, 18, 22, 26 and 30.
- LCSTo3 outputs the channel control bits for streams LSTo3, 7, 11, 15, 19, 23, 27 and 31.

The Channel Control Bit location, within a frame period, for each channel of the Local output streams is presented in LCSTo Allocation of Channel Control Bits to the Output Streams**.**

As an aid to the description, the channel control bit for a single channel on specific streams is presented, with reference to Table 2:

(1) The Channel Control Bit corresponding to Stream 0, Channel 0, **LSTo0_Ch0,** is transmitted on **LCSTo0** and is advanced, relative to the Frame Boundary, by 10 periods of **C16o**.

(2) The Channel Control Bit corresponding to Stream 28, Channel 0, **LSTo28_Ch0,** is transmitted on **LCSTo0** in advance of the Frame Boundary by three periods of output clock, **C16o**. Similarly, the Channel Control Bits for **LSTo29_Ch0**, **LSTo30_Ch0** and **LSTo31_Ch0** are advanced relative to the Frame Boundary by three periods of **C16o**, on **LCSTo1**, **LCSTo2** and **LCSTo3**, respectively.

The **LCSTo0-3** outputs data at a constant data-rate of 16.384 Mb/s, independent of the data-rate selected for the individual output streams, **LSTo0-31**. Streams at data-rates lower than 16.384 Mb/s will have the value of the respective channel control bit repeated for the duration of the channel. The bit will be repeated twice for 8.192 Mb/s streams, four times for 4.096 Mb/s streams and eight times for 2.048 Mb/s streams. The channel control bit is not repeated for 16.384 Mb/s streams.

Examples are presented, with reference to Table 2:

(3) With stream **LSTo4** selected to operate at a data-rate of 2.048 Mb/s, the value of the Channel Control Bit for **Channel 0** will be transmitted during the **C16o** clock period nos. 2040, 2048, 8, 16, 24, 32, 40 and 48.

(4) With stream **LSTo8** operated at a data-rate of 8.192Mb/s, the value of the Channel Control Bit for **Channel 1** will be transmitted during the **C16o** clock period nos. 9 and 17.

Figure 13, Local Port External High Impedance Control Bit Timing (ST-Bus Mode) shows the channel control bits for **LCSTo0**, **LCSTo1**, **LCSTo2** and **LCSTo3** in one possible scenario which includes stream **LSTo0** at a data-rate of 16.384 Mb/s, **LSTo1** at 8.192 Mb/s, **LSTo6** at 4.096 Mb/s and **LSTo7** at 2.048 Mb/s. All remaining streams are operated at a data-rate of 16.384 Mb/s.

4.1.2 LORS Set HIGH

The Local Output Enable Bit (**LE**) of the Local Connection Memory has direct per-channel control on the high-impedance state of the Local Output streams, **LSTo0-31**. Programming a LOW state will set the stream output of the MT90869 to High Impedance for the duration of the channel period. See **Section 12.3, Local Connection Memory Bit Definition**, for programming details.

The **LCSTo0-3** outputs remain active.

	Allocated Stream No.				Channel No. [2]			
$\overline{\text{C16o}}$ Period[1]	LCSTo0	LCSTo1	LCSTo2	LCSTo3	16 Mb/s	8 Mb/s	4 Mb/s	2 Mb/s
2039	0 [3-1]	1	2	3	Ch 0	Ch 0	Ch 0	Ch 0
2040	4 [3-3]	5	6	7	Ch 0	Ch 0	Ch 0	Ch 0
2041	8	9	10	11	Ch 0	Ch 0	Ch 0	Ch 0
2042	12	13	14	15	Ch 0	Ch 0	Ch 0	Ch 0

Table 2 - LCSTo Allocation of Channel Control Bits to the Output Streams

	Allocated Stream No.				Channel No. [2]				
$\overline{C16o}$ Period[1]	LCSTo0	LCSTo1	LCSTo2	LCSTo3	16 Mb/s	8 Mb/s	4 Mb/s	2 Mb/s	
2043	16	17	18	19	Ch 0	Ch 0	Ch 0	Ch 0	
2044	20	21	22	23	Ch 0	Ch 0	Ch 0	Ch 0	
2045	24	25	26	27	Ch 0	Ch 0	Ch 0	Ch 0	
2046	28 [3-2]	29 [3-2]	30 [3-2]	31 [3-2]	Ch 0	Ch 0	Ch 0	Ch 0	
2047	0	1	2	3	Ch 1	Ch 0	Ch 0	Ch 0	
2048	4 [3-3]	5	6	7	Ch 1	Ch 0	Ch 0	Ch 0	Frame
1	8	9	10	11	Ch 1	Ch 0	Ch 0	Ch 0	Boundary
2	12	13	14	15	Ch 1	Ch 0	Ch 0	Ch 0	
3	16	17	18	19	Ch 1	Ch 0	Ch 0	Ch 0	
4	20	21	22	23	Ch 1	Ch 0	Ch 0	Ch 0	
5	24	25	26	27	Ch 1	Ch 0	Ch 0	Ch 0	
6	28	29	30	31	Ch 1	Ch 0	Ch 0	Ch 0	
7	0	1	2	3	Ch 2	Ch 1	Ch 0	Ch 0	
8	4 [3-3]	5	6	7	Ch 2	Ch 1	Ch 0	Ch 0	
9	8 [3-4]	9	10	11	Ch 2	Ch 1	Ch 0	Ch 0	
10	12	13	14	15	Ch 2	Ch 1	Ch 0	Ch 0	
11	16	17	18	19	Ch 2	Ch 1	Ch 0	Ch 0	
12	20	21	22	23	Ch 2	Ch 1	Ch 0	Ch 0	
13	24	25	26	27	Ch 2	Ch 1	Ch 0	Ch 0	
14	28	29	30	31	Ch 2	Ch 1	Ch 0	Ch 0	
15	0	1	2	3	Ch 3	Ch 1	Ch 0	Ch 0	
16	4 [3-3]	5	6	7	Ch 3	Ch 1	Ch 0	Ch 0	
17	8 [3-4]	9	10	11	Ch 3	Ch 1	Ch 0	Ch 0	
etc	etc	etc	etc	etc	etc	etc	etc	etc	
etc	etc	etc	etc	etc	etc	etc	etc	etc	
2029	etc	etc	etc	etc	Ch 254	Ch 127	Ch 63	Ch 31	
2030	28	29	30	31	Ch 254	Ch 127	Ch 63	Ch 31	
2031	0	1	2	3	Ch 255	Ch 127	Ch 63	Ch 31	
2032	4	5	6	7	Ch 255	Ch 127	Ch 63	Ch 31	
2033	8	9	10	11	Ch 255	Ch 127	Ch 63	Ch 31	
2034	12	13	14	15	Ch 255	Ch 127	Ch 63	Ch 31	
2035	16	17	18	19	Ch 255	Ch 127	Ch 63	Ch 31	

Table 2 - LCSTo Allocation of Channel Control Bits to the Output Streams

	Allocated Stream No.				Channel No. [2]				
$\overline{\text{C16o}}$ Period[1]	LCSTo0	LCSTo1	LCSTo2	LCSTo3	16 Mb/s	8 Mb/s	4 Mb/s	2 Mb/s	
2036	20	21	22	23	Ch 255	Ch 127	Ch 63	Ch 31	
2037	24	25	26	27	Ch 255	Ch 127	Ch 63	Ch 31	
2038	28	29	30	31	Ch 255	Ch 127	Ch 63	Ch 31	
2039	0	1	2	3	Ch 0	Ch 0	Ch 0	Ch 0	
2040	4	5	6	7	Ch 0	Ch 0	Ch 0	Ch 0	
2041	8	9	10	11	Ch 0	Ch 0	Ch 0	Ch 0	
2042	12	13	14	15	Ch 0	Ch 0	Ch 0	Ch 0	
2043	16	17	18	19	Ch 0	Ch 0	Ch 0	Ch 0	
2044	20	21	22	23	Ch 0	Ch 0	Ch 0	Ch 0	
2045	24	25	26	27	Ch 0	Ch 0	Ch 0	Ch 0	
2046	28	29	30	31	Ch 0	Ch 0	Ch 0	Ch 0	
2047	0	1	2	3	Ch 1	Ch 0	Ch 0	Ch 0	
2048	4	5	6	7	Ch 1	Ch 0	Ch 0	Ch 0	Frame
1	8	9	10	11	Ch 1	Ch 0	Ch 0	Ch 0	Boundary
2	12	13	14	15	Ch 1	Ch 0	Ch 0	Ch 0	
3	16	17	18	19	Ch 1	Ch 0	Ch 0	Ch 0	
etc	etc	etc	etc	etc	etc	etc	etc	etc	

Table 2 - LCSTo Allocation of Channel Control Bits to the Output Streams

Note 1: Clock Period count is referenced to Frame Boundary.
Note 2: The Channel Numbers presented relate to the data-rate selected for a specific stream.
Note 3-1 to 3-4: See Section 4.1.1 for examples of Channel Control Bit for streams of different data-rates.

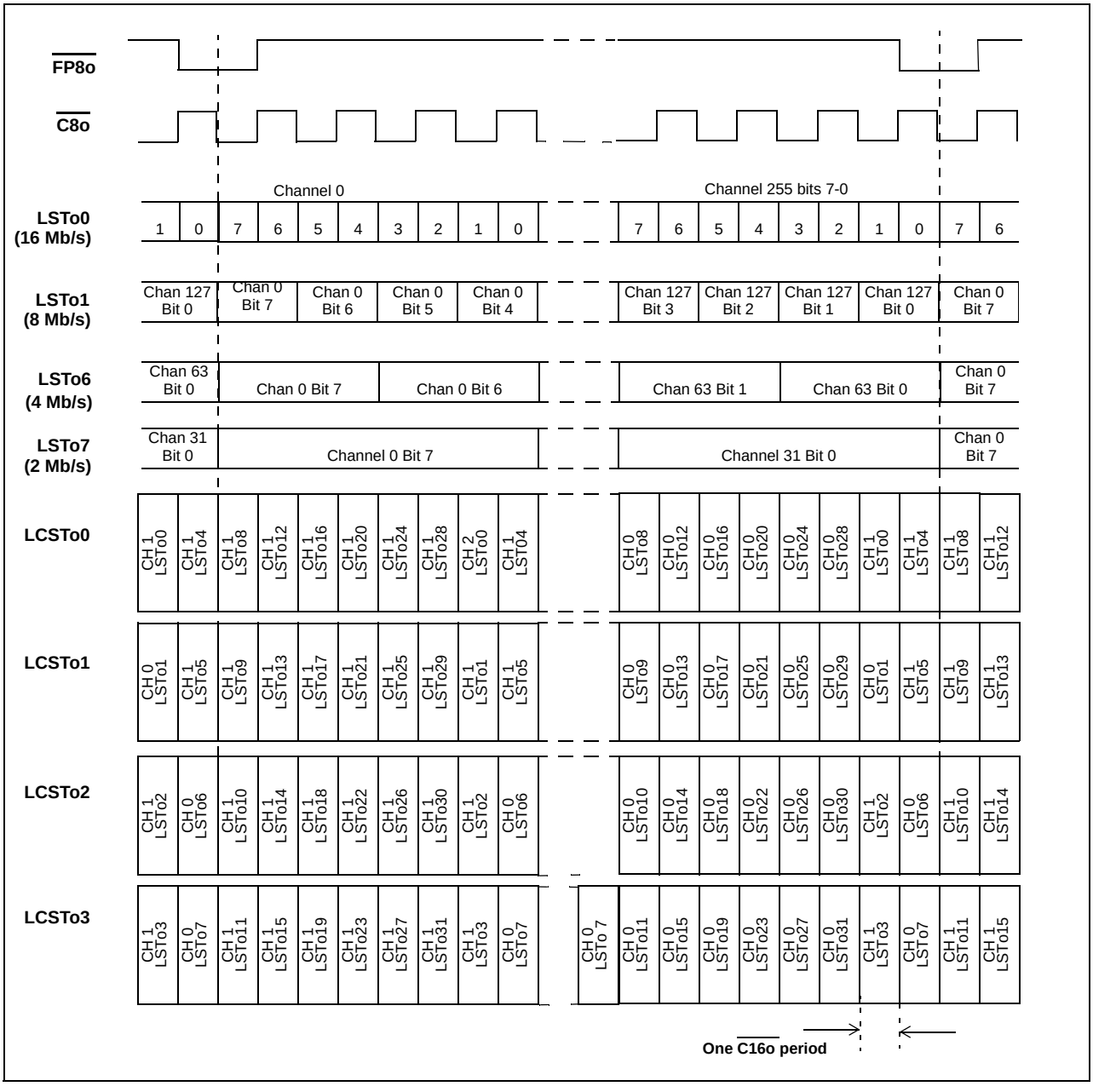


Figure 13 - Local Port External High Impedance Control Bit Timing (ST-Bus Mode)

4.2 Backplane High Impedance Control

The input pin, **BORS**, selects whether the Backplane output streams, **BSTo0-31** are set to high impedance at the output of the MT90869 itself, or are always driven (active HIGH or active LOW) and a high impedance state, if required on a per-channel basis, is invoked through an external interface circuit controlled by the **BCSTo0-3** signals. Setting **BORS** to a LOW state will configure the output streams, **BSTo0-31,** to transmit bi-state channel data with per-channel high-impedance determined by external circuits under the control of the **BCSTo0-3** outputs. Setting **BORS** to a HIGH state will configure the output streams, **BSTo0-31,** of the MT90869 to invoke a high-impedance output on a per-channel basis.

The state of the **BORS** pin is detected and the MT90869 configured accordingly during a **$\overline{\text{RESET}}$** operation, e.g. following power-up. The BORS pin is an asynchronous input and is expected to be hard-wired for a particular system application, although it may be driven under logic control if preferred.

4.2.1 BORS Set LOW, Non-32 Mb/s Mode

The data (channel control bit) transmitted by **BCSTo0-3** replicates the Backplane Output Enable Bit (**BE**) of the Backplane Connection Memory, with a LOW state indicating the channel to be set to High Impedance. See **Section 12.4, Backplane Connection Memory Bit Definition** for setting the Backplane Output Enable Bit (**BE**).

The **BCSTo0-3** outputs transmit serial data (channel control bits) at 16.384 Mb/s, with each bit representing the per-channel high impedance state for specific streams. Eight output streams are allocated to each control line as follows:

(See also **Pin Description**)

- BCSTo0 outputs the channel control bits for streams BSTo0, 4, 8, 12, 16, 20, 24 and 28.
- BCSTo1 outputs the channel control bits for streams BSTo1, 5, 9, 13, 17, 21, 25 and 29.
- BCSTo2 outputs the channel control bits for streams BSTo2, 6, 10, 14, 18, 22, 26 and 30.
- BCSTo3 outputs the channel control bits for streams BSTo3, 7, 11, 15, 19, 23, 27 and 31.

The Channel Control Bit location, within a frame period, for each channel of the Backplane output streams is presented in **BCSTo Allocation of Channel Control Bits to the Output Streams (Non-32 Mb/s Mode)**.

As an aid to the description, the channel control bit for a single channel on specific streams is presented, with reference to Table 3:

(1) The Channel Control Bit corresponding to Stream 0, Channel 0, **BSTo0_Ch0,** is transmitted on **BCSTo0** and is advanced, relative to the Frame Boundary, by 10 periods of **C16o**.

(2) The Channel Control Bit corresponding to Stream 28, Channel 0, **BSTo28_Ch0,** is transmitted on **BCSTo0** in advance of the Frame Boundary by three periods of output clock, **C16o**. Similarly, the Channel Control Bits for **BSTo29_Ch0**, **BSTo30_Ch0** and **BSTo31_Ch0** are advanced relative to the Frame Boundary by three periods of **C16o**, on **BCSTo1**, **BCSTo2** and **BCSTo3**, respectively.

The **BCSTo0-3** outputs data at a constant data-rate of 16.384 Mb/s, independent of the data-rate selected for the individual output streams, **BSTo0-31**. Streams at data-rates lower than 16.384 Mb/s will have the value of the respective channel control bit repeated for the duration of the channel. The bit will be repeated twice for 8.192 Mb/s streams, four times for 4.096 Mb/s streams and eight times for 2.048 Mb/s streams. The channel control bit is not repeated for 16.384 Mb/s streams.

Examples are presented, with reference to Table 3:

(3) With stream **BSTo4** selected to operate at a data-rate of 2.048 Mb/s, the value of the Channel Control Bit for **Channel 0** will be transmitted during the **C16o** clock period nos. 2040, 2048, 8, 16, 24, 32, 40 and 48.

(4) With stream **BSTo8** operated at a data-rate of 8.192 Mb/s, the value of the Channel Control Bit for **Channel 1** will be transmitted during the **C16o** clock period nos. 9 and 17.

	Allocated Stream No.				**Channel No. [2]**			
$\overline{\text{C16o}}$ Period[1]	**BCSTo0**	**BCSTo1**	**BCSTo2**	**BCSTo3**	**16 Mb/s**	**8 Mb/s**	**4 Mb/s**	**2 Mb/s**
2039	0 [3-1]	1	2	3	Ch 0	Ch 0	Ch 0	Ch 0
2040	4 [3-3]	5	6	7	Ch 0	Ch 0	Ch 0	Ch 0

Table 3 - BCSTo Allocation of Channel Control Bits to the Output Streams (Non-32 Mb/s Mode)

	Allocated Stream No.				Channel No. [2]				
$\overline{C16o}$ Period[1]	BCSTo0	BCSTo1	BCSTo2	BCSTo3	16 Mb/s	8 Mb/s	4 Mb/s	2 Mb/s	
2041	8	9	10	11	Ch 0	Ch 0	Ch 0	Ch 0	
2042	12	13	14	15	Ch 0	Ch 0	Ch 0	Ch 0	
2043	16	17	18	19	Ch 0	Ch 0	Ch 0	Ch 0	
2044	20	21	22	23	Ch 0	Ch 0	Ch 0	Ch 0	
2045	24	25	26	27	Ch 0	Ch 0	Ch 0	Ch 0	
2046	28 [3-2]	29 [3-2]	30 [3-2]	31 [3-2]	Ch 0	Ch 0	Ch 0	Ch 0	
2047	0	1	2	3	Ch 1	Ch 0	Ch 0	Ch 0	
2048	4 [3-3]	5	6	7	Ch 1	Ch 0	Ch 0	Ch 0	Frame
1	8	9	10	11	Ch 1	Ch 0	Ch 0	Ch 0	Boundary
2	12	13	14	15	Ch 1	Ch 0	Ch 0	Ch 0	
3	16	17	18	19	Ch 1	Ch 0	Ch 0	Ch 0	
4	20	21	22	23	Ch 1	Ch 0	Ch 0	Ch 0	
5	24	25	26	27	Ch 1	Ch 0	Ch 0	Ch 0	
6	28	29	30	31	Ch 1	Ch 0	Ch 0	Ch 0	
7	0	1	2	3	Ch 2	Ch 1	Ch 0	Ch 0	
8	4 [3-3]	5	6	7	Ch 2	Ch 1	Ch 0	Ch 0	
9	8 [3-4]	9	10	11	Ch 2	Ch 1	Ch 0	Ch 0	
10	12	13	14	15	Ch 2	Ch 1	Ch 0	Ch 0	
11	16	17	18	19	Ch 2	Ch 1	Ch 0	Ch 0	
12	20	21	22	23	Ch 2	Ch 1	Ch 0	Ch 0	
13	24	25	26	27	Ch 2	Ch 1	Ch 0	Ch 0	
14	28	29	30	31	Ch 2	Ch 1	Ch 0	Ch 0	
15	0	1	2	3	Ch 3	Ch 1	Ch 0	Ch 0	
16	4 [3-3]	5	6	7	Ch 3	Ch 1	Ch 0	Ch 0	
17	8 [3-4]	9	10	11	Ch 3	Ch 1	Ch 0	Ch 0	
etc	etc	etc	etc	etc	etc	etc	etc	etc	
etc	etc	etc	etc	etc	etc	etc	etc	etc	
2029	etc	etc	etc	etc	Ch 254	Ch 127	Ch 63	Ch 31	
2030	28	29	30	31	Ch 254	Ch 127	Ch 63	Ch 31	
2031	0	1	2	3	Ch 255	Ch 127	Ch 63	Ch 31	
2032	4	5	6	7	Ch 255	Ch 127	Ch 63	Ch 31	
2033	8	9	10	11	Ch 255	Ch 127	Ch 63	Ch 31	

Table 3 - BCSTo Allocation of Channel Control Bits to the Output Streams (Non-32 Mb/s Mode)

	Allocated Stream No.				Channel No. [2]				
$\overline{C16o}$ Period[1]	BCSTo0	BCSTo1	BCSTo2	BCSTo3	16 Mb/s	8 Mb/s	4 Mb/s	2 Mb/s	
2034	12	13	14	15	Ch 255	Ch 127	Ch 63	Ch 31	
2035	16	17	18	19	Ch 255	Ch 127	Ch 63	Ch 31	
2036	20	21	22	23	Ch 255	Ch 127	Ch 63	Ch 31	
2037	24	25	26	27	Ch 255	Ch 127	Ch 63	Ch 31	
2038	28	29	30	31	Ch 255	Ch 127	Ch 63	Ch 31	
2039	0	1	2	3	Ch 0	Ch 0	Ch 0	Ch 0	
2040	4	5	6	7	Ch 0	Ch 0	Ch 0	Ch 0	
2041	8	9	10	11	Ch 0	Ch 0	Ch 0	Ch 0	
2042	12	13	14	15	Ch 0	Ch 0	Ch 0	Ch 0	
2043	16	17	18	19	Ch 0	Ch 0	Ch 0	Ch 0	
2044	20	21	22	23	Ch 0	Ch 0	Ch 0	Ch 0	
2045	24	25	26	27	Ch 0	Ch 0	Ch 0	Ch 0	
2046	28	29	30	31	Ch 0	Ch 0	Ch 0	Ch 0	
2047	0	1	2	3	Ch 1	Ch 0	Ch 0	Ch 0	
2048	4	5	6	7	Ch 1	Ch 0	Ch 0	Ch 0	Frame
1	8	9	10	11	Ch 1	Ch 0	Ch 0	Ch 0	Boundary
2	12	13	14	15	Ch 1	Ch 0	Ch 0	Ch 0	
3	16	17	18	19	Ch 1	Ch 0	Ch 0	Ch 0	
etc	etc	etc	etc	etc	etc	etc	etc	etc	

Table 3 - BCSTo Allocation of Channel Control Bits to the Output Streams (Non-32 Mb/s Mode)

Note 1: Clock Period count is referenced to Frame Boundary.
Note 2: The Channel Numbers presented relate to the data-rate selected for a specific stream.
Note 3-1 to 3-4: See Section 4.2.1 for examples of Channel Control Bit for streams of different data-rates.

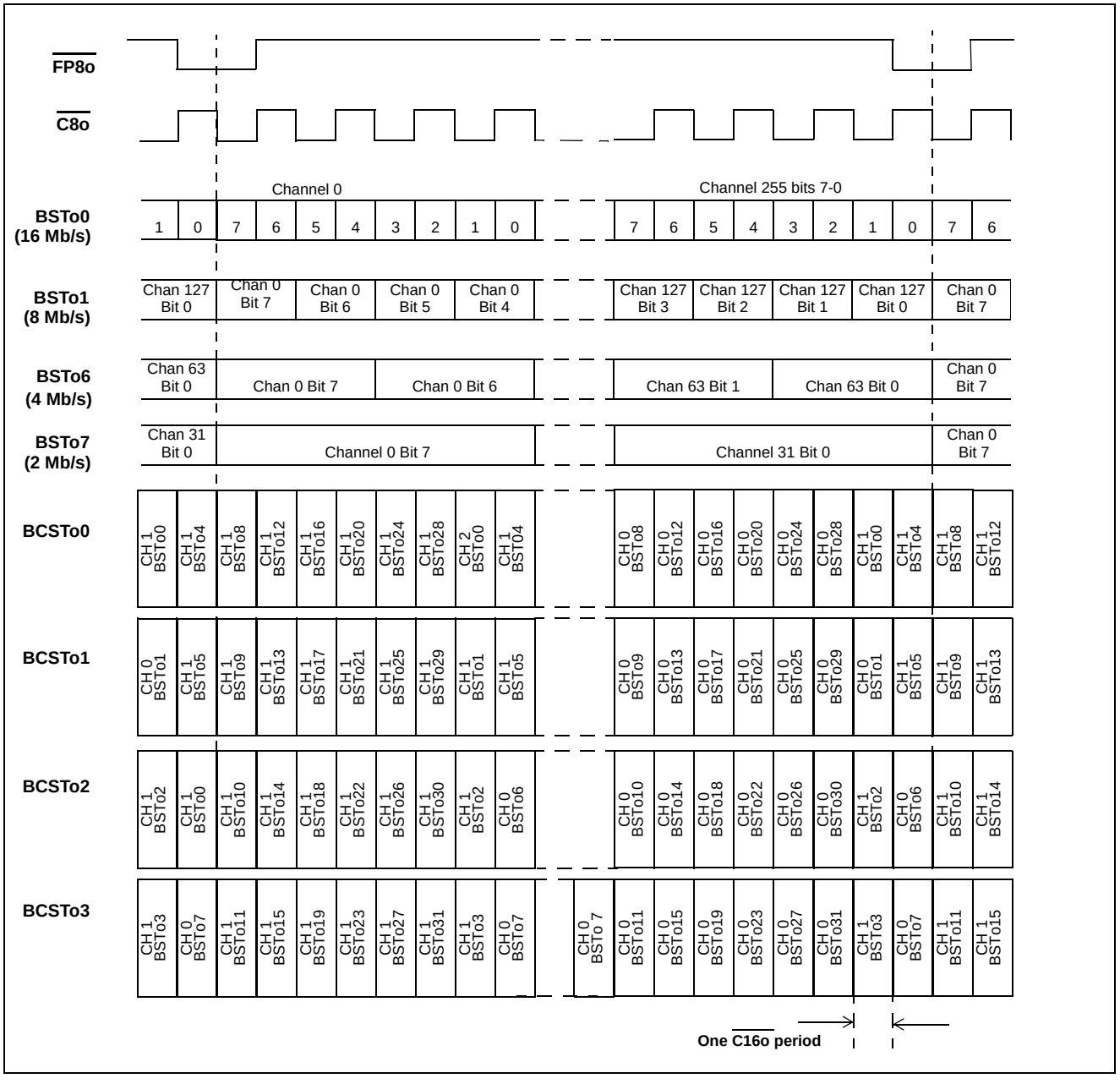


Figure 14 - Backplane Port External High Impedance Control Bit Timing (Non-32 Mb/s mode)

Figure 14, Backplane Port External High Impedance Control Bit Timing (Non-32 Mb/s mode) shows the channel control bits for **BCSTo0**, **BCSTo1**, **BCSTo2** and **BCSTo3** in one possible scenario which includes stream **BSTo0** at a data-rate of 16.384 Mb/s, **BSTo1** at 8.192 Mb/s, **BSTo6** at 4.096 Mb/s and **BSTo7** at 2.048 Mb/s. All remaining streams are operated at a data-rate of 16.384 Mb/s.

4.2.2 BORS Set LOW, 32 Mb/s Mode

The data (channel control bit) transmitted by **BCSTo0-3** replicates the Backplane Output Enable Bit (**BE**) of the Backplane Connection Memory, with a LOW state indicating the channel be set to High Impedance. See **Section 12.4, Backplane Connection Memory Bit Definition** for setting the Backplane Output Enable Bit (**BE**).

The **BCSTo0-3** outputs transmit serial data (channel control bits) at 16.384 Mb/s, with each bit representing the per-channel high impedance state for specific streams. Four output streams are allocated to each control line as follows:-

(See also **Pin Description**)

- BCSTo0 outputs the channel control bits for streams BSTo0, 4, 8, and 12.
- BCSTo1 outputs the channel control bits for streams BSTo1, 5, 9, and 13.
- BCSTo2 outputs the channel control bits for streams BSTo2, 6, 10, and 14.
- BCSTo3 outputs the channel control bits for streams BSTo3, 7, 11, and 15.

The Channel Control Bit location, within a frame period, for each channel of the Backplane output streams is presented in **BCSTo Allocation of Channel Control Bits to the Output Streams (32 Mb/s Mode)**

The **BCSTo0-3** outputs data at a constant data-rate of 16.384Mb/s and all output streams, **BSTo0-15**, operate at a data-rate of 32.768 Mb/s.

As an aid to the description, the channel control bit for a single channel on specific streams is presented, with reference to Table 4:

(1) The Channel Control Bit corresponding to Stream 0, Channel 0, **BSTo0_Ch0,** is transmitted on **BCSTo0** and is advanced, relative to the Frame Boundary, by six periods (clock period no. 2043) of **C16o**.

(2) The Channel Control Bit corresponding to Stream 12, Channel 0, **BSTo12_Ch0,** is transmitted on **BCSTo0** in advance of the Frame Boundary by three periods (clock period no. 2046) of output clock, **C16o**. Similarly, the Channel Control Bits for **BSTo13_Ch0**, **BSTo14_Ch0** and **BSTo15_Ch0** are advanced relative to the Frame Boundary by three periods of **C16o**, on **BCSTo1**, **BCSTo2** and **BCSTo3**, respectively.

(3) For stream **BSTo4** the value of the Channel Control Bit for **Channel 510** will be transmitted during the **$\overline{\text{C16o}}$** clock period no. 2036 on **BCSTo0**.

(4) For stream **BSTo5** the value of the Channel Control Bit for **Channel 4** will be transmitted during the **$\overline{\text{C16o}}$** clock period no. 12 on **BCSTo1**.

Figure 15, Backplane Port External High Impedance Control Timing (32 Mb/s Mode) shows the channel control bits for **BCSTo0**, **BCSTo1**, **BCSTo2** and **BCSTo3**.

	Allocated Stream No.				**Channel No. [2]**
$\overline{\text{C16o}}$ Period[1]	**BCSTo0**	**BCSTo1**	**BCSTo2**	**BCSTo3**	**32 Mb/s**
2039	0	1	2	3	Ch 511
2040	4	5	6	7	Ch 511
2041	8	9	10	11	Ch 511
2042	12	13	14	15	Ch 511
2043	0 [3-1]	1	2	3	Ch 0
2044	4	5	6	7	Ch 0
2045	8	9	10	11	Ch 0
2046	12 [3-2]	13 [3-2]	14 [3-2]	15 [3-2]	Ch 0
2047	0	1	2	3	Ch 1

Table 4 - BCSTo Allocation of Channel Control Bits to the Output Streams (32 Mb/s Mode)

	Allocated Stream No.				Channel No. [2]	
$\overline{\text{C16o}}$ Period[1]	BCSTo0	BCSTo1	BCSTo2	BCSTo3	32 Mb/s	
2048	4	5	6	7	Ch 1	Frame
1	8	9	10	11	Ch 1	Boundary
2	12	13	14	15	Ch 1	
3	0	1	2	3	Ch 2	
4	4	5	6	7	Ch 2	
5	8	9	10	11	Ch 2	
6	12	13	14	15	Ch 2	
7	0	1	2	3	Ch 3	
8	4	5	6	7	Ch 3	
9	8	9	10	11	Ch 3	
10	12	13	14	15	Ch 3	
11	0	1	2	3	Ch 4	
12	4	5^{3-4}	6	7	Ch 4	
13	8	9	10	11	Ch 4	
14	12	13	14	15	Ch 4	
15	0	1	2	3	Ch 5	
16	4	5	6	7	Ch 5	
17	8	9	10	11	Ch 5	
etc	etc	etc	etc	etc	etc	
etc	etc	etc	etc	etc	etc	
2029	etc	etc	etc	etc	Ch 508	
2030	12	13	14	15	Ch 508	
2031	0	1	2	3	Ch 509	
2032	4	5	6	7	Ch 509	
2033	8	9	10	11	Ch 509	
2034	12	13	14	15	Ch 509	
2035	0	1	2	3	Ch 510	
2036	4^{3-3}	5	6	7	Ch 510	
2037	8	9	10	11	Ch 510	
2038	12	13	14	15	Ch 510	
2039	0	1	2	3	Ch 511	
2040	4	5	6	7	Ch 511	

Table 4 - BCSTo Allocation of Channel Control Bits to the Output Streams (32 Mb/s Mode)

	Allocated Stream No.				Channel No. [2]	
$\overline{C16o}$ Period[1]	BCSTo0	BCSTo1	BCSTo2	BCSTo3	32 Mb/s	
2041	8	9	10	11	Ch 511	
2042	12	13	14	15	Ch 511	
2043	0	1	2	3	Ch 0	
2044	4	5	6	7	Ch 0	
2045	8	9	10	11	Ch 0	
2046	12	13	14	15	Ch 0	
2047	0	1	2	3	Ch 1	
2048	4	5	6	7	Ch 1	Frame
1	8	9	10	11	Ch 1	Boundary
2	12	13	14	15	Ch 1	
3	0	1	2	3	Ch 2	
etc	etc	etc	etc	etc	etc	

Table 4 - BCSTo Allocation of Channel Control Bits to the Output Streams (32 Mb/s Mode)

Note 1: Clock Period count is referenced to Frame Boundary.
Note 2: The Channel Numbers presented relate to the specific stream operating at a data-rate of 32.768Mb/s.
Note 3-1 to 3-4: See Section 4.2.2 for examples of Channel Control Bits.

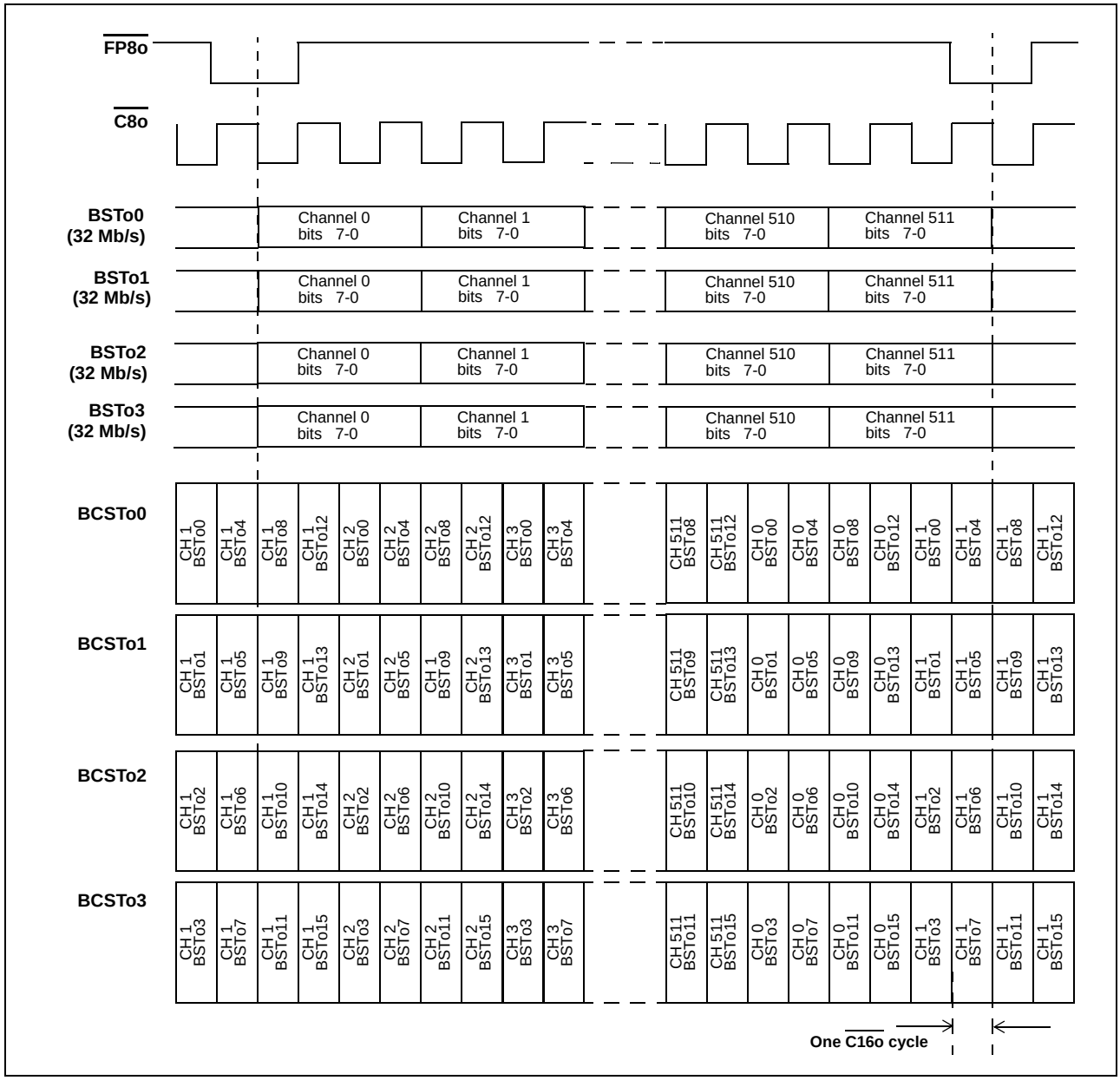


Figure 15 - Backplane Port External High Impedance Control Timing (32 Mb/s Mode)

4.2.3 BORS Set HIGH

The Backplane Output Enable Bit (**BE**) of the Backplane Connection Memory has direct per-channel control on the high-impedance state of the Backplane Output streams, **BSTo0-31** (for Non-32 Mb/s Mode) and BSTo0-15 (for 32 Mb/s Mode). Programming a LOW state will set the stream output of the MT90869 to High Impedance for the duration of the channel period. See **Section 12.4, Backplane Connection Memory Bit Definition**, for programming details.

The **BCSTo0-3** outputs remain active.

5.0 Data Delay Through the Switching Paths

For all data rates, the received serial data is converted to parallel format and stored sequentially in the data memory. Each data memory location corresponds to an input stream and channel number. To provide constant delay and maintain frame integrity, the MT90869 utilizes four pages of data memory. Consecutive frames are written in turn to each page of memory. Reading is controlled to allow a channel data written in frame N to be read during frame N+3.

A constant delay of three frames is applied to all switching paths irrespective of data-rate or channel number. See Figure 16, Constant Switch Delay: Examples of different stream rates and routing.

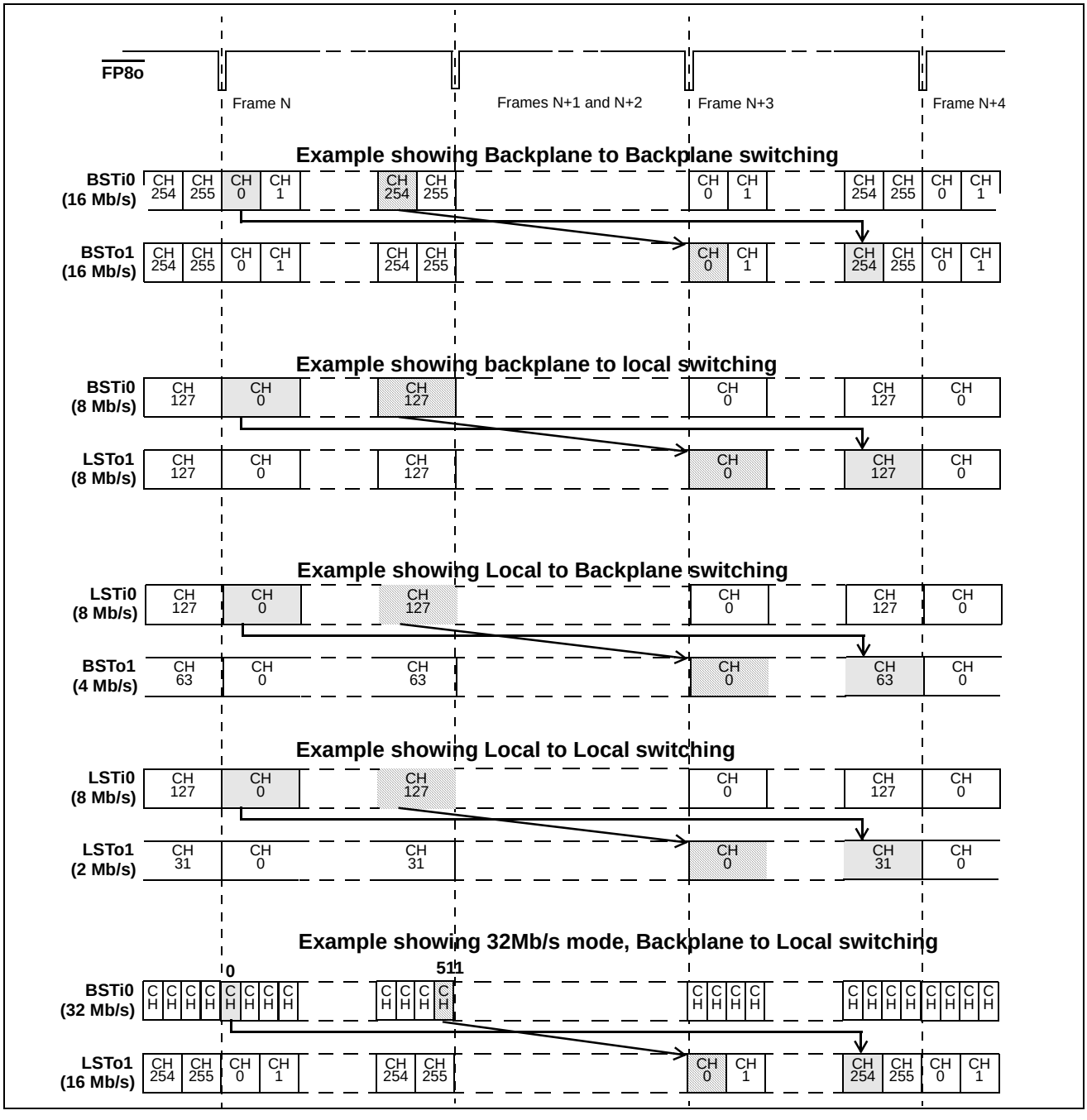


Figure 16 - Constant Switch Delay: Examples of different stream rates and routing

6.0 Connection Memory Description

The MT90869 incorporates two connection memories, Local Connection Memory and Backplane Connection Memory.

6.1 Local Connection Memory

The Local Connection Memory (LCM) is 16-bit wide with 8,192 memory locations to support the Local output port. The most significant bit of each word, bit [15], selects the source stream from either the Backplane or the Local port and determines the Backplane-to-Local or Local-to-Local data routing. Bits [14:13] select the control modes of the Local output streams, namely the per-channel message and the per-channel high impedance output control modes. In Connection Mode (Bit14 = LOW), Bits [12:0] select the source stream and channel number as detailed in Table 5. In Message Mode (Bit14 = HIGH), Bits [12:8] are unused and Bits [7:0] contain the message byte to be transmitted.

The Control Register bits MS2, MS1, and MS0 must be set to 000, respectively, to select the Local Connection Memory for the Write and Read operations via the microprocessor port. See **Section 7.0, Microprocessor Port**, and Section 13.1, Control Register (CR) for details on microprocessor port access.

Source Stream Bit Rate	Source Stream No.	Source Channel No.
2 Mb/s	[12:8] legal values 0:31	[7:0] legal values 0:31
4 Mb/s	[12:8] legal values 0:31	[7:0] legal values 0:63
8 Mb/s	[12:8] legal values 0:31	[7:0] legal values 0:127
16 Mb/s	[12:8] legal values 0:31	[7:0] legal values 0:255
32 Mb/s (Backplane streams only)	[12:9] legal values 0:15	[8:0] legal values 0:511

Table 5 - Local and Backplane Connection Memory Configuration

6.2 Backplane Connection Memory

The Backplane Connection Memory (BCM) is 16-bit wide with 8,192 memory locations to support the Backplane output port. The most significant bit of each word, bit [15], selects the source stream from either the Backplane or the Local port and determines the Local-to-Backplane or Backplane-to-Backplane data routing. Bits [14:13] select the control modes of the Backplane output streams, namely the per-channel Message Mode and the per-channel high impedance output control mode. In Connection Mode (Bit14 = LOW), Bits [12:0] select the source stream and channel number as detailed in Table 5. In Message Mode (Bit14 = HIGH), Bits [12:8] are unused and Bits [7:0] contain the message byte to be transmitted.

The Control Register bits MS2, MS1, and MS0 must be set to 001, respectively, to select the Backplane Connection Memory for the Write and Read operations via the microprocessor port. See **Section 7.0, Microprocessor Port**, and Section 13.1, Control Register (CR) for details on microprocessor port access.

6.3 Connection Memory Block Programming

This feature allows fast, simultaneous, initialization of the Local and Backplane Connection Memories after power up. When the Memory Block Programming mode is enabled, the contents of the Block Programming Register (BPR) will be loaded into the connection memories. See Table 16 and Table 17 for details of the Control Register and Block Programming Register values, respectively.

6.3.1 Memory Block Programming Procedure

- Set the **MBP** bit in the Control Register from LOW to HIGH.
- Set the **BPE** bit to HIGH in the Block Programming Register (BPR). The Local Block Programming data bits, **LBPD2-0**, of the Block Programming Register, will be loaded into Bit 15, Bit 14 and Bit 13, respectively. of the Local Connection Memory. The remaining bit positions are loaded with zeros as shown in Table 6.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LBPD2	LBPD1	LBPD0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6 - Local Connection Memory in Block Programming Mode

The Backplane Block Programming data bits, **BBPD2-0**, of the Block Programming Register, will be loaded into Bit 15, Bit 14 and Bit 13, respectively, of the Backplane Connection Memory. The remaining bit positions are loaded with zeros as shown in Table 7.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BBPD2	BBPD1	BBPD0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7 - Backplane Connection Memory in Block Programming Mode

The Block Programming Register bit, BPE will be automatically reset LOW within 125us, to indicate completion of memory programming.

The Block Programming Mode can be terminated at any time prior to completion by setting the **BPE** bit of the Block Programming Register or the MBP bit of the Control Register to LOW.

Note the default values (LOW) of **LBPD2-0** and **BBPD2-0** of the Block Programming Register, following a device reset, may be used. These settings shall set all output channels to High, or High-Impedance, in accordance with the **LORS** and **BORS** pin conditions, see Pin Description for further details. The Local Connection Memory shall be configured to select data from Channel 0 of Backplane input Stream 0 (**BSTi0**), and the Backplane Connection Memory shall be configured to select data from Channel 0 of Local input Stream 0 (**LSTi0**). Alternative conditions may be established by programming bits **LBPD2-0** and **BBPD2-0** of the Block Programming Register at the time of setting Bit **BPE** to HIGH. See Section 12.3, Local Connection Memory Bit Definition, Section 12.4, Backplane Connection Memory Bit Definition, and Section 13.2, Block Programming Register (BPR).

7.0 Microprocessor Port

The MT90869 supports non-multiplexed Motorola microprocessors. The microprocessor port consists of 16-bit parallel data bus (**D0-15**), 15-bit address bus (**A0-14**) and four control signals (**CS, DS, R/W** and **DTA**). The data bus provides access to the internal registers, the Backplane Connection and Data memories, and the Local Connection and Data memories. Each memory has 8,192 locations. See Address Map for Data and Connection Memory Locations (A14=1), for the address mapping.

Each Connection Memory can be read or written via the 16-bit microprocessor port. The Data Memories can only be read (but not written) from the microprocessor port.

To prevent the bus 'hanging', in the event of the MT90869 not receiving a master clock, the microprocessor port shall complete the DTA handshake when accessed but any data read from the bus will be invalid.

There must be a minimum of 30 ns between CPU accesses, to allow the MT90869 device to recognize the accesses as separate (i.e., a minimum of 30 ns must separate the de-assertion of DTA (to high) and the assertion of CS and/or DS to initiate the next access).

8.0 Device Power-up, Initialization and Reset

8.1 Power-Up Sequence

The recommended power-up sequence is for the VDD_IO supply (nominally +3.3 V) to be established before the power-up of the VDD_PLL and VDD_CORE supplies (nominally +1.8 V). The VDD_PLL and VDD_CORE supplies may be powered up simultaneously, but neither should 'lead' the VDD_IO supply by more than 0.3 V.

All supplies may be powered-down simultaneously.

8.2 Initialization

Upon power up, the MT90869 should be initialized by applying the following sequence:

1 Ensure the **$\overline{\text{TRST}}$** pin is permanently LOW to disable the JTAG TAP controller.

2 Set **$\overline{\text{ODE}}$** pin to LOW. This configures the **LCSTo0-3** output signals to LOW (i.e. to set optional external output buffers to high impedance), and sets the **LSTo0-31** outputs to high or high impedance, dependent on the **LORS** input value, and sets the **BCSTo0-3** output signals to LOW (i.e., to set optional external output buffers to high impedance), and sets the **BSTo0-31** outputs to high or high impedance, dependent on **BORS** input value. Refer to Pin Description for details of the **LORS** and **BORS** pins.

3 Reset the device by pulsing the **$\overline{\text{RESET}}$** pin to zero for at least two cycles of the input clock, **$\overline{\text{C8i}}$**.

4 Use the Block Programming Mode to initialize the Local and the Backplane Connection Memories. Refer to Section 6.3, Connection Memory Block Programming.

5 Set **$\overline{\text{ODE}}$** pin to HIGH after the connection memories are programmed to ensure that bus contention will not occur at the serial stream outputs.

8.3 Reset

The **$\overline{\text{RESET}}$** pin is used to reset the device. When set LOW, an asynchronous reset is applied to the MT90869. It is synchronized to the internal clock and remains active for 50 us following release (set HIGH) of the external **$\overline{\text{RESET}}$** to allow time for the PLL to fully settle. During the reset period, depending on the state of input pins **LORS** and **BORS**, the output streams **LSTo0- 31** and **BSTo0-31** are set to high or high impedance, and all internal registers and counters are reset to the default state.

The **$\overline{\text{RESET}}$** pin must remain low for two input clock cycles (**$\overline{\text{C8i}}$**) to guarantee a synchronized reset release.

When a $\overline{\text{RESET}}$ is applied to the MT90869, the CS line is inhibited and the DTA line may become active through simultaneous microport activity. External gating of the $\overline{\text{DTA}}$ line with $\overline{\text{CS}}$ is recommended to avoid bus conflict in applications incorporating multiple devices with individual reset conditions.

9.0 Bit Error Rate Test

Independent Bit Error Rate (BER) test mechanisms are provided for the Local and Backplane ports. In both ports there is a BER transmitter and a BER receiver. The transmitter and receiver are each independently controlled to allow either looped back, or uni-directional testing. The transmitter generates a 2^{15}-1 or 2^{23}-1 Pseudo Random Binary Sequence (PRBS), which may be allocated to a specific stream and a number of channels. This is defined by a stream number, a start channel number, and the number of consecutive channels following the start channel. The stream, channel number and the number of consecutive channels following the start channel are similarly allocated for the receiver and detection of the PRBS. Examples of a channel sequence are presented in Figure 17.

When enabled, the receiver attempts to lock to the PRBS on the incoming bit stream. Once lock is achieved, by detection of a seed value, a bit by bit comparison takes place and each error shall increment a 16-bit counter. A counter 'roll-over' shall occur in the event of an error count in excess of 65535.

The BER operations are controlled by registers as follows (refer to **Section 13.3, Bit Error Rate Test Control Register (BERCR)** for overall control, **Section 13.10, Local Bit Error Rate (BER) Registers** and Section 13.11, Backplane Bit Error Rate (BER) Registers for register programming details):

- BER Control Register (**BERCR**) - Independently enables BER transmission and receive testing for backplane and local ports.
- Local and Backplane BER Start Send Registers (**LBSSR** and **BBSSR**) - Defines the output stream and start channel for BER transmission.
- Local and Backplane Transmit BER Length Registers (**LTXBLR** and **BTXBLR**) - Defines, for transmit stream, how many consecutive channels to follow the start channel.
- Local and Backplane BER Start Receive Registers (**LBSR** and **BBSR**) - Define the input stream and channel from where the BER sequence will start to be compared.
- Local and Backplane Receive BER Length Registers (**LRXBLR** and **BRXBLR**) - Defines, for the receive stream, how many consecutive channels follow the start channel.
- Local and Backplane BER Count Registers (**LBCR** and **BBCR**) - Contain the number of counted errors.

The registers listed completely define the transmit stream and channels. When BER transmission is enabled for these channels, the source bits and the message mode bits, **LSRC** and **LMM** in the Local Connection Memory, and **BSRC** and **BMM** in the Backplane Connection Memory, are ignored. The enable bits (**LE** and **BE**) of the respective connection memories should be set to HIGH to enable the outputs for the selected channels.

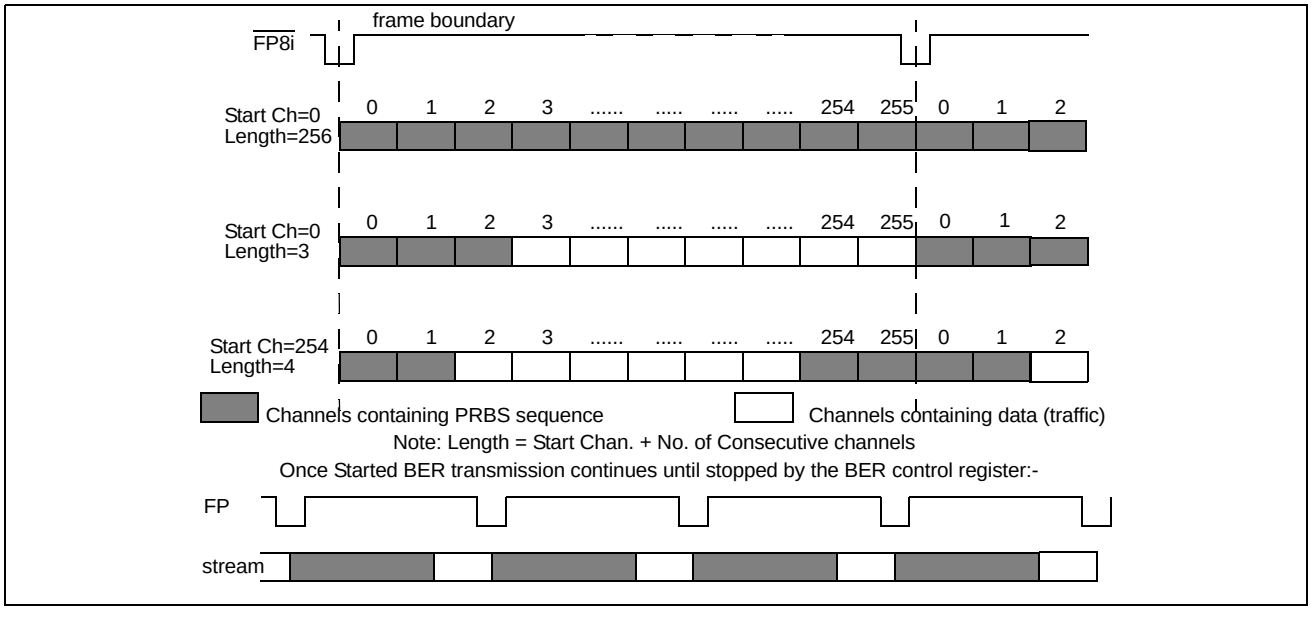


Figure 17 - Examples of BER transmission channels

10.0 Memory Built-In-Self-Test (BIST) Mode

As operation of the memory BIST will corrupt existing data, this test must only be instigated when the device is placed “out-of-service” or isolated from live traffic.

The memory BIST mode is enabled through the microprocessor port (**Section 13.14, Memory BIST Register**). Internal BIST memory controllers generate the memory test pattern (S-march) and control the memory test. The memory test result is monitored through the Memory BIST Register when controlled via the microprocessor interface.

11.0 JTAG Port

The MT90869 JTAG interface conforms to the Boundary-Scan IEEE 1149.1 standard. The operation of the boundary-scan circuit shall be controlled by an external Test Access Port (TAP) Controller. JTAG is intended to be used during the development cycle. The JTAG interface is operational when the MT90869 core (V_{DD}-core) is powered at typical voltage levels.

11.1 Test Access Port (TAP)

The Test Access Port (TAP) consists of four input pins and one output pin described as follows:

- **Test Clock Input (TCK)**
  TCK provides the clock for the TAP Controller and is independent of any on-chip clock. **TCK** permits the shifting of test data into or out of the Boundary-Scan register cells under the control of the TAP Controller in Boundary-Scan Mode.
- **Test Mode Select Input (TMS)**
  The TAP controller uses the logic signals applied to the TMS input to control test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin in internally pulled to V_{DD_IO} when not driven from an external source.
- **Test Data Input (TDi)**
  Depending on the previously applied data to the **TMS** input, the serial input data applied to the **TDi** port is connected either to the Instruction Register or to a Test Data Register. Both registers are described in a Section 11.2, TAP Registers. The applied input data is sampled at the rising edge of TCK pulses. This pin is internally pulled to V_{DD_IO} when not driven from an external source.
- **Test Data Output (TDo)**
  Depending on the previously applied sequence to the **TMS** input, the contents of either the instruction register or data register are serially shifted out towards the **TDo**. The data out of the **TDo** is clocked on the falling edge of the **TCK** pulses. When no data is shifted through the boundary scan cells, the **TDo** output is set to a high impedance state.
- **Test Reset ($\overline{\text{TRST}}$)**
  $\overline{\text{TRST}}$ provides an asynchronous Reset to the JTAG scan structure. This pin is internally pulled to V_{DD_IO} when not driven from an external source.

11.2 TAP Registers

The MT90869 uses the public instructions defined in the IEEE 1149.1 standard with the provision of an Instruction Register and three Test Data Registers.

11.2.1 Test Instruction Register

The JTAG interface contains a four-bit instruction register. Instructions are serially loaded into the Instruction Register from the **TDi** pin when the TAP Controller is in the shift-IR state. Instructions are subsequently decoded to achieve two basic functions: to select the Test Data Register to operate while the instruction is current, and to define the serial Test Data Register path to shift data between **TDi** and **TDo** during data register scanning.

11.2.2 Test Data Registers

11.2.2.1 The Boundary-Scan Register

The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the MT90869 core logic.

11.2.2.2 The Bypass Register

The Bypass register is a single stage shift register to provide a one-bit path from **TDi** to **TDo**.

11.2.2.3 The Device Identification Register

The JTAG device ID for the MT90869 is $0086914B_H$.

Version, Bits <31:28>:0000

Part No., Bits <27:12>:0000 1000 0110 1001

Manufacturer ID, Bits <11:1>:0001 0100 101

Header, Bit <0> (LSB):1

11.3 Boundary Scan Description Language (BSDL) File

A Boundary Scan Description Language (BSDL) file is available from Zarlink Semiconductor to aid in the use of the IEEE 1149.1 test interface.

12.0 Memory Address Mappings

Address Bit	Description
A14	Selects memory or register access
A13-A9	Stream address (0-31)
A8-A0	Channel address (0-511)
	Notes: 1. Bit A14 must be high for accessing to data and connection memory positions. Bit A14 must be low for accessing registers. 2. Streams 0 to 15 are used when the backplane serial streams are at 32.768 Mb/s. 3. Channels 0 to 31 are used when serial stream is at 2.048 Mb/s. 4. Channels 0 to 63 are used when serial stream is at 4.096 Mb/s. 5. Channels 0 to 127 are used when serial stream is at 8.192 Mb/s. 6. Channels 0 to 255 are used when serial stream is at 16.384 Mb/s. 7. Channels 0 to 511 are used when serial stream is at 32.768 Mb/s.

Table 8 - Address Map for Data and Connection Memory Locations (A14=1)

The device contains two data memory blocks, one for received backplane data and one for received local data. For all data rates the received data is converted to parallel format by internal serial to parallel converters and stored sequentially in the relevant data memory.

12.1 Backplane Data Memory Bit Definition

The 8-bit Backplane Data Memory (BDM) has 8,192 positions. The locations are associated with the backplane input streams and channels. The address bits (A13:0) of the microprocessor define the addresses of the streams and the channels. The BDM is configured as follows:

Bit	Name	Description
15-8	Reserved	Set to a default value of 0
7-0	BDM	Backplane Data Memory Backplane Input Channel Data

Table 9 - Backplane Data Memory (BDM) Bits

12.2 Local Data Memory Bit Definition

The 8-bit Local Data Memory (LDM) has 8,192 positions. The locations are associated with the local input streams and channels. The address bits of the microprocessor define the addresses of the streams and the channels. The LDM is configured as follows:

Bit	Name	Description
15-8	Reserved	Set to a default value of 0
7-0	LDM	Local Data Memory Local Input Channel Data

Table 10 - Local Data Memory (LDM) Bits

12.3 Local Connection Memory Bit Definition

The Local Connection Memory (LCM) has 8,192 addresses of 16-bit words. Each address, accessed through bits A13-A0 of the microprocessor port, is allocated to an individual Local output stream and channel. The bit definition for each 16-bit word is presented in Table 11 for Local-to-Local and Backplane (Non-32 Mb/s Mode)-to-Local connections, and in Table 12, for Local-to-Local and Backplane(32 Mb/s Mode)-to-Local connections. Bit LSRC selects the switch configuration for Backplane-to-Local or Local-to-Local. When the per-channel Message Mode is selected (LMM = HIGH), the lower byte of the LCM word (LCAB7-0) will be transmitted as data on the output stream (LSTo0-31) in place of data defined by the Source Control, Stream and Channel Address bits.

Bit	Name	Description
15	LSRC	**Source Control Bit** When LOW, the source is from the Backplane input port (Backplane Data Memory). When HIGH, the source is from the Local input port (Local Data Memory). Ignored when LMM is set HIGH.
14	LMM	**Local Message Mode Bit** When LOW, the channel is in Connection Mode. When HIGH, the channel is in Message Mode.
13	LE	**Local Output Enable Bit** When LOW the channel may be high impedance, either at the device output, or set by an external buffer dependent upon the LORS pin. When HIGH the channel is active.

Bit	Name	Description
12-8	LSAB4-0	**Source Stream Address Bits** The binary value of these 5 bits represents the input stream number. Ignored when LMM is set HIGH.
7-0	LCAB7-0	**Source Channel Address Bits** The binary value of these 8 bits represents the input channel number when LMM is set LOW. Transmitted as data when LMM is set HIGH.

Table 11 - LCM Bits for Local-to-Local and Backplane (Non-32 Mb/s Mode)-to-Local Switching

Bit	Name	Description
15	LSRC	**Source Control Bit.** When LOW, the source is from the Backplane input port (Backplane Data Memory). When HIGH, the source is from the Local input port (Local Data Memory). Ignored when LMM is set HIGH.
14	LMM	**Local Message Mode Bit** When LOW, the channel is in Connection Mode. When HIGH, the channel is in Message Mode.
13	LE	**Local Output Enable Bit** When LOW, the channel may be high impedance, either at the device output or set by an external buffer, dependent upon the LORS pin. When HIGH, the channel is active.
12-9	LSAB3-0	**Source Stream Address Bits.** The binary value of these 4 bits represents the input stream number. Ignored when LMM is set HIGH.
8-0	LCAB8-0	**Channel Address Bits.** The binary value of these 9 bits represents the input channel number, when LMM is LOW. Bits LCAB7-0 transmitted as data when LMM is set HIGH.

Table 12 - LCM Bits for Backplane(32 Mb/s Mode)-to-Local Switching

12.4 Backplane Connection Memory Bit Definition

The Backplane Connection Memory (BCM) has 8,192 addresses of 16-bit words. Each address, accessed through bits A13-A0 of the microprocessor port, is allocated to an individual Backplane output stream and channel. The bit definition for each 16-bit word is presented in Table 13 for Local-to- Backplane (Non-32Mb/s Mode) and Backplane-to-Backplane (Non-32 Mb/s Mode) connections, and in Table 14, for Local-to-Backplane (32Mb/s Mode) and Backplane-to-Backplane (32 Mb/s Mode) connections.

Bit BSRC selects the switch configuration for Local-to-Backplane or Backplane-to-Backplane. When the per-channel Message Mode is selected (BMM = HIGH), the lower byte of the BCM word (BCAB7-0) will be transmitted as data on the output stream (BSTo0-31) in place of data defined by the Source Control, Stream Address and Channel Address bits.

Bit	Name	Description
15	BSRC	**Backplane Source Control Bit.** When LOW, the source is from the local input port (Local Data Memory). When HIGH, the source is from the backplane input port (Backplane Data Memory). BSRC is ignored when BMM is set HIGH in Message Mode.
14	BMM	**Backplane Message Mode Bit.** When LOW, the channel is in Connection Mode. When HIGH, the channel is in Message Mode.
13	BE	**Backplane Output Enable Bit.** When LOW the channel may be high impedance, either at the device output or set by an external buffer, dependent upon the BORS pin. When HIGH the channel is active.
12-8	BSAB4-0	**Backplane Source Stream Address Bits.** The binary value of these 5 bits represents the input stream number. BSAB4-0 are ignored when BMM is set HIGH in Message Mode.
7-0	BCAB7-0	**Source Channel Address Bits.** The binary value of these 8 bits represents the input channel number when BMM is set LOW. BCAB7-0 are transmitted as data when BMM is set HIGH in Message Mode.

Table 13 - BCM Bits for Local-to-Backplane and Backplane-to-Backplane Switching (Non-32 Mb/s Mode)

Bit	Name	Description
15	BSRC	**Backplane Source Control Bit.** When LOW, the source is from the local input port (Local Data Memory). When HIGH, the source is from the backplane input port (Backplane Data Memory). BSRC is ignored when BMM is set HIGH in Message Mode.
14	BMM	**Backplane Message Mode Bit.** When LOW, the channel is in Connection Mode. When HIGH, the channel is in Message Mode.
13	BE	**Backplane Output Enable Bit.** When this bit is low the channel may be high impedance, either at the device output or set by an external buffer, dependent upon the BORS pin. When the bit is high the channel is active.
12-9	BSAB3-0	**Backplane Source Stream Address Bits.** The binary value of these 4 bits represents the input stream number. BSAB3-0 are ignored when BMM is set HIGH in Message Mode.
8-0	BCAB8-0	**Source Channel Address Bits**. The binary value of these 9 bits represents the input channel number when BMM is LOW. BCAB7-0 are transmitted as data when BMM is set HIGH in Message Mode.

Table 14 - BCM Bits for Backplane-to-Backplane Switching (32Mb/s mode)

12.5 Internal Register Mappings

A14 - A0	Register
0000_H	Control Register, CR
0001_H	Block Programming Register, BPR
0002_H	BER Control Register, BERCR
0003_H - 0022_H	Local Input Channel Delay Register 0, LCDR0 - Register 31, LCDR31
0023_H - 0042_H	Local Input Bit Delay Register 0, LIDR0 - Register 31, LIDR31
0043_H - 0062_H	Backplane Input Channel Delay Register 0, BCDR0 - Register 31, BCDR31
0063_H - 0082_H	Backplane Input Bit Delay Register 0, BIDR0 - Register 31, BIDR31
0083_H - $00A2_H$	Local Output Advancement Register 0, LOAR0 - Register 31, LOAR31
$00A3_H$ - $00C2_H$	Backplane Output Advancement Register 0, BOAR0 - Register 31, BOAR31
$00C3_H$	Local BER Start Send Register, LBSSR
$00C4_H$	Local Transmit BER Length Register, LTXBLR
$00C5_H$	Local Receive BER Length Register, LRXBLR
$00C6_H$	Local BER Start Receive Register, LBSRR
$00C7_H$	Local BER Count Register, LBCR
$00C8_H$	Backplane BER Start Send Register, BBSSR
$00C9_H$	Backplane Transmit BER Length Register, BTXBLR
$00CA_H$	Backplane Receive BER Length Register, BRXBLR
$00CB_H$	Backplane BER Start Receive Register, BBSRR
$00CC_H$	Backplane BER Count Register, BBCR
$00CD_H$ - $00EC_H$	Local Input Bit rate Register 0, LIBRR0 - Register 31, LIBRR31
$00ED_H$ - $010C_H$	Local Output Bit rate Register 0, LOBRR0 - Register 31, LOBRR31
$010D_H$ - $012C_H$	Backplane Input Bit rate Register 0, BIBRR0 - Register 31, BIBRR31
$012D_H$ - $014C_H$	Backplane Output Bit rate Register 0, BOBRR0 - Register 31, BOBRR31
$014D_H$	Memory BIST Register, MBISTR
$3FFF_H$	Revision control register, RCR

Table 15 - Address Map for Register (A14 = 0)

13.0 Detailed Register Description

This section describes the registers that are used in the device.

13.1 Control Register (CR)

Address 0000h.

The control register defines which memory is to be accessed. It initiates the memory block programming mode and selects the backplane data rate mode. The Control Register (**CR**) is configured as follows:

Bit	Name	Reset	Description
15-9	Reserved	0	**Reserved**.
8	FPW	0	**Frame Pulse Width** When LOW, an input frame pulse width of 122 ns shall be applied to $\overline{\text{FP8i}}$. When HIGH, an input frame pulse width of 244 ns shall be applied to $\overline{\text{FP8i}}$.
7	MODE32	0	**32 MHz Mode** When LOW, Backplane streams (BSTi0-31 and BSTo0-31) may be individually programmed for data-rates of 2, 4, 8, or 16 Mb/s. When HIGH, the Backplane streams (BSTi0-15 and BSTo0-15) operate in 32 Mb/s mode.
6	C8IPOL	0	**8 MHz Input Clock Polarity** The input frame boundary **MUST** be aligned to the $\overline{\text{C8i}}$ clock rising edge. This bit, C8IPOL, **MUST** be set HIGH to achieve correct frame boundary alignment. If this bit is LOW, the input frame boundary alignment will not work correctly.
5	COPOL	0	**Output Clock Polarity** When set LOW, the output clock is the same polarity as the input clock. When set HIGH, the output clock is inverted. This applies to both 8 MHz (C8o) and 16 MHz (C16o) output clocks.
4	MBP	0	**Memory Block Programming** When LOW, the memory block programming mode is disabled. When HIGH, the connection memory block programming mode is ready to program the Local Connection Memory (LCM), and the Backplane Connection Memory (BCM).
3	OSB	0	**Output Stand By** This bit enables the BSTo0 - 31 and the LSTo0 - 31 serial outputs**.** **Output Control with ODE pin and OSB bit** When LOW, the BSTo0-31 and LSTo0-31 are driven high or high impedance, dependent on the BORS and LORS pin settings respectively, and BCSTo0-3 and LCSTo0-3 are driven low. When HIGH, the BSTo0-31, LSTo0-31, BCSTo0-3 and LCSTo0-3 are enabled.

ODE Pin	OSB bit	BSTo0 - 31, LSTo0 - 31
0	X	Disable
1	0	Disable
1	1	Enable

Table 16 - Control Register Bits

Bit	Name	Reset	Description
2-0	MS(2:0)	0	**Memory Select Bits.** These three bits select the connection or data memory for subsequent micro-port memory access operations: 000, Local Connection Memory (LCM) is selected for Read or Write operations. 001, Backplane Connection Memory (BCM) is selected for Read or Write operations. 010, Local Data Memory is selected for Read-only operation. 011, Backplane Data Memory is selected for Read-only operation.

Table 16 - Control Register Bits

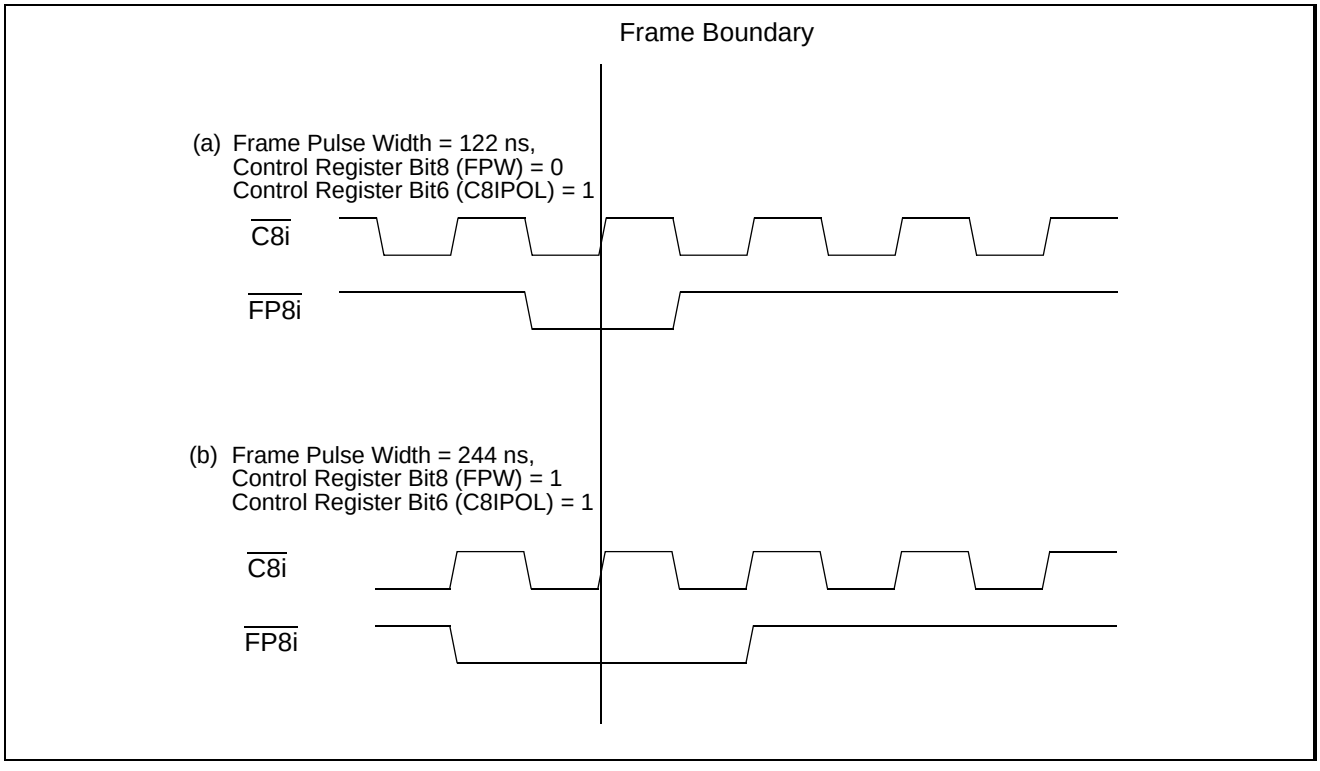


Figure 18 - Frame Boundary Conditions, ST- BUS Operation

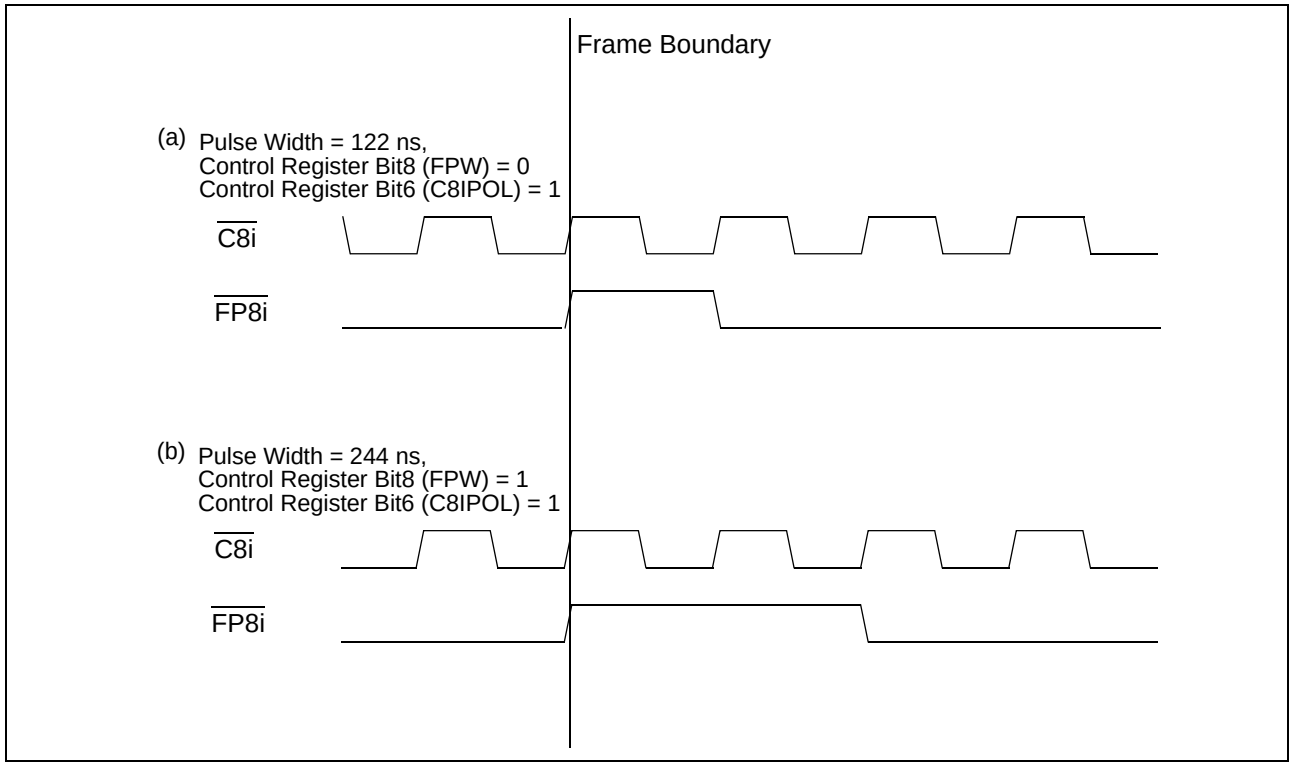


Figure 19 - Frame Boundary Conditions, GCI - BUS Operation

13.2 Block Programming Register (BPR)

Address 0001h.

The block programming register stores the bit patterns to be loaded into the connection memories when the Memory Block Programming feature is enabled. The BPE, LBPD2-0 and BBPD2-0 bits in the BPR register must be defined in the same write operation.

The BPE bit is set HIGH, to commence the block programming operation. Programming is completed in one frame period and may be instigated at any time within a frame. The BPE bit returns to LOW to indicate the block programming function has completed.

When BPE is HIGH, no other bits of the BPR register must be changed for at least a single frame period, except to abort the programming operation. The programming operation may be aborted by setting either BPE to LOW, or the Control Register bit, MBP, to LOW.

The **BPR** register is configured as follows.

Bit	Name	Reset	Description
15-7	Unused	0	**Set LOW.**
6-4	BBPD(2:0)	0	**Backplane Block Programming Data.** These bits refer to the value loaded into the Backplane Connection Memory (BCM) when the Memory Block Programming feature is activated. When the MBP bit in the Control Register (CR) is set HIGH and the BPE is set HIGH, the contents of Bits BBPD2-0 are loaded into Bits 15-13, respectively, of the BCM. Bits 12-0 of the BCM are set LOW.

Bit	Name	Reset	Description
3-1	LBPD(2:0)	0	**Local block Programming Data.** These bits refer to the value loaded into the Local Connection Memory (LCM), when the Memory Block Programming feature is activated. When the MBP bit in the Control Register is set HIGH and the BPE is set HIGH, the contents of Bits LBPD2-0 are loaded into Bits 15-13, respectively, of the LCM. Bits 12-0 of the LCM are set LOW.
0	BPE	0	**Block Programming Enable.** A LOW to HIGH transition of this bit enables the Memory Block Programming function. A LOW will be returned after 125 us, upon completion of programming. Set LOW to abort the programming operation.

Table 17 - Block Programming Register Bits

13.3 Bit Error Rate Test Control Register (BERCR)

Address 0002h.

The BER control register controls backplane and local port BER testing. It independently enables and disables transmission and reception. It is configured as follows:

Bit	Name	RESET	Description
15-12	Reserved	0	**Reserved.**
11	LOCKB	0	**Backplane Lock (READ ONLY).** This bit is automatically set HIGH when the receiver has locked to the incoming data sequence. The bit is reset by a LOW to HIGH transition on SBERRXB.
10	PRSTB	0	**PBER Reset for Backplane.** A LOW to HIGH transition initializes the backplane BER generator to the seed value.
9	CBERB	0	**Clear Bit Error Rate Register for Backplane.** A LOW to HIGH transition in this bit resets the backplane internal bit error counter and the backplane bit error (BBERR) register to zero.
8	SBERRXB	0	**Start Bit Error Rate Receiver for Backplane.** A LOW to HIGH transition enables the Backplane BER receiver. The receiver monitors incoming data for reception of the seed value. When detected, the LOCK state is indicated (LOCKB) and the receiver compares the incoming bits with the reference generator for bit equality and increments the Backplane Bit error Register (BBCR) on each failure. When set LOW, bit comparison is disabled and the error count is frozen. The error count is stored in the Backplane Bit Error Register (BBCR).
7	SBERTXB	0	**Start Bit Error Rate Transmitter for Backplane.** A LOW to HIGH transition starts the BER transmission. When set LOW, transmission is disabled.
6	PRBSB	0	**BER Mode Select for Backplane.** When set HIGH, a PRBS sequence of length 2^{23}-1 is selected for the Backplane port. When set LOW, a PRBS sequence of length 2^{15}-1 is selected for the Backplane port.

Table 18 - Bit Error Rate Test Control Register (BERCR) Bits

Bit	Name	RESET	Description
5	LOCKL	0	**Local Lock (READ ONLY).** This bit is automatically set HIGH when the receiver has locked to the incoming data sequence. The bit is reset by a LOW to HIGH transition on SBERRXL
4	PRSTL	0	**PBER Reset for Local.** A LOW to HIGH transition initializes the local BER generator to the seed value.
3	CBERL	0	**Clear Bit Error Rate Register for Local.** A LOW to HIGH transition resets the local internal bit error counter and the local bit error (LBERR) register to zero.
2	SBERRXL	0	**Start Bit Error Rate Receiver for Local.** A LOW to HIGH transition enables the Local BER receiver. The receiver monitors incoming data for reception of the seed value. When detected, the LOCK state is indicated (LOCKL) and the receiver compares the incoming bits with the reference generator for bit equality and increments the Local Bit error Register (LBCR) on each failure. When set LOW, bit comparison is disabled and the error count is frozen. The error count is stored in the Local Bit Error Register (LBCR).
1	SBERTXL	0	**Start Bit Error Rate Transmitter for Local.** A LOW to HIGH transition enables the Local BER transmission. When set LOW, transmission is disabled.
0	PRBSL	0	**BER Mode Select for Local.** When set HIGH, a PRBS sequence of length 2^{23}-1 is selected for the Local port. When set LOW, a PRBS sequence of length 2^{15}-1 is selected for the Local port.

Table 18 - Bit Error Rate Test Control Register (BERCR) Bits

13.4 Local Input Channel Delay Registers (LCDR0 to LCDR31)

Address 0003h to 0022h.

Thirty-two local input channel delay registers (LCDR0 to LCDR31) allow users to program the input channel delay for the local input data streams LSTi0-31. The possible adjustment is 255 channels and the LCDR0 to LCDR31 registers are configured as follows:

LCDRn Bit (where n = 0 to 31)	Name	Reset	Description
15-8	Reserved	0	**Reserved**
7-0	LCD(7:0)	0	**Local Channel Delay Register** The binary value of these bits refers to the channel delay value for the local input stream.

Table 19 - Local Channel Delay Register (LCDRn) Bits

13.4.1 Local Channel Delay Bits 7-0 (LCD7 - LCD0)

These eight bits define the delay, in channel numbers, the serial interface receiver take to store the channel data from the Local stream input pins. The input channel delay can be selected to 255 (16 Mb/s streams), 127 (8 Mb/s streams), 63 (4 Mb/s streams) or 31 (2 Mb/s streams) from the frame boundary.

Input Stream Channel Delay	Corresponding Delay Bits
	LCD7-LCD0
0 Channel (Default)	0000 0000
1 Channel	0000 0001
2 Channels	0000 0010
3 Channels	0000 0011
4 Channels	0000 0100
5 Channels	0000 0101
...	...
...	...
253 Channels	1111 1101
254 Channels	1111 1110
255 Channels	1111 1111

Table 20 - Local Input Channel Delay Programming Table

13.5 Local Input Bit Delay Registers (LIDR0 to LIDR31)

Address 0023h to 0042h.

Thirty-two local input delay registers (LIDR0 to LIDR31) allow users to program the input bit delay for the local input data streams LSTi0-31. The possible adjustment is up to 7 3/4 of the data rate, advancing forward with a resolution of 1/4 of the data rate. The data rate can be either 2 Mb/s, 4 Mb/s, 8 Mb/s or 16 Mb/s.

The LIDR0 to LIDR31 registers are configured as follows:

LIDRn Bit (where n = 0 to 31)	Name	Reset	Description
15-5	Reserved	0	**Reserved**
4-0	LIDn(4:0)	0	**Local Input Bit Delay Register** The binary value of these bits refers to the input bit delay value for the local input stream

Table 21 - Local Channel Delay Register (LIDRn) Bits

13.5.1 Local Input Delay Bits 4-0 (LID4 - LID0)

These five bits define the delay from the bit boundary that the receiver uses to sample each input. Input bit delay adjustment can range up to $7^3/_4$ bit periods forward, with resolution of $^1/_4$ bit period.

This can be described as: LIDn(4:0) = (number of bits delay) / 4

For example, if LIDn(4:0) is set to 10011 (19), the input bit delay = 19 * $^1/_4$ = $4^3/_4$.

Table 22, “Local Input Bit Delay Programming Table,” on page 57, illustrates the bit delay selection.

	Corresponding Delay Bits				
Data Rate	**LID4**	**LID3**	**LID2**	**LID1**	**LID0**
0 (Default)	0	0	0	0	0
1/4	0	0	0	0	1
1/2	0	0	0	1	0
3/4	0	0	0	1	1
1	0	0	1	0	0
1 1/4	0	0	1	0	1
1 1/2	0	0	1	1	0
1 3/4	0	0	1	1	1
2	0	1	0	0	0
2 1/4	0	1	0	0	1
2 1/2	0	1	0	1	0
2 3/4	0	1	0	1	1
3	0	1	1	0	0
3 1/4	0	1	1	0	1
3 1/2	0	1	1	1	0
3 3/4	0	1	1	1	1
4	1	0	0	0	0
4 1/4	1	0	0	0	1
4 1/2	1	0	0	1	0
4 3/4	1	0	0	1	1
5	1	0	1	0	0
5 1/4	1	0	1	0	1
5 1/2	1	0	1	1	0
5 3/4	1	0	1	1	1
6	1	1	0	0	0
6 1/4	1	1	0	0	1
6 1/2	1	1	0	1	0
6 3/4	1	1	0	1	1
7	1	1	1	0	0
7 1/4	1	1	1	0	1
7 1/2	1	1	1	1	0
7 3/4	1	1	1	1	1

Table 22 - Local Input Bit Delay Programming Table

13.6 Backplane Input Channel Delay Registers (BCDR0 to BCDR31)

Address 0043h to 0062h

Thirty-two backplane input channel delay registers (BCDR0 to BCDR31) allow users to program the input channel delay for the backplane input data streams BSTi0-31. The possible adjustment is 511 channels and the BCDR0 to BCDR31 registers are configured as follows:

BCDRn Bit (where n = 0 to 31 for non-32Mb/s mode, n = 0 to 15 for 32Mb/s mode)	**Name**	**Reset**	**Description**
15-9	Reserved	0	**Reserved**
8-0	BCD(8:0)	0	**Backplane Channel Delay Register** The binary value of these bits refers to the channel delay value for the backplane input stream

Table 23 - Backplane Channel Delay Register (BCDRn) Bits

13.6.1 Backplane Channel Delay Bits 8-0 (BCDn8 - BCDn0)

These nine bits define the delay, in channel numbers, the serial interface receiver takes to store the channel data from the Backplane input pins. The input channel delay can be selected to 511 (32 Mb/s streams), 255 (16 Mb/s streams), 127 (8 Mb/s streams), 63 (4 Mb/s streams) or 31 (2 Mb/s streams) from the frame boundary.

Input Stream Channel Delay	**Corresponding Delay Bits**
	BCD8-BCD0
0 Channel (Default)	0 0000 0000
1 Channel	0 0000 0001
2 Channels	0 0000 0010
3 Channels	0 0000 0011
4 Channels	0 0000 0100
5 Channels	0 0000 0101
...	...
...	...
509 Channels	1 1111 1101
510 Channels	1 1111 1110
511 Channels	1 1111 1111

Table 24 - Backplane Input Channel Delay (BCD) Programming Table

13.7 Backplane Input Bit Delay Registers (BIDR0 to BIDR31)

Address 0063h to 0082h

Thirty-two backplane input delay registers (BIDR0 to BIDR31) allow users to program the input bit delay for the backplane input data streams BSTi0-31. The possible adjustment is 7 3/4 of the data rate, in steps of 1/4 of the data rate. The data rate can be either 2 Mb/s, 4 Mb/s, 8 Mb/s, 16 Mb/s, or 32 Mb/s.

The BIDR0 to BIDR31 registers are configured as follows:

BIDRn Bit (where n = 0 to 31 for Non-32 Mb/s Mode, n = 0 to15 for 32 Mb/s Mode)	**Name**	**Reset**	**Description**
15-5	Reserved	0	**Reserved**
4-0	BID(4:0)	0	**Backplane Input Bit Delay Register** The binary value of these bits refers to the input bit delay value for the backplane input stream

Table 25 - Backplane Input Bit Delay Register (BIDRn) Bits

13.7.1 Backplane Input Delay Bits 4-0 (BID4 - BID0)

These five bits define how long in the cycle the serial interface receiver takes to recognize and stores the bit 0 from the BSTi input pins: i.e., start assuming a new frame. Input bit delay adjustment can range up to $7^3/_4$ bit periods forward with resolution of $^1/_4$ bit period.

This can be described as BIDn(4:0) = (number of bits delay) / 4

For example, if BID(4:0) is set to 10011 (19), the input bit delay = 19 * $^1/_4$ = $4^3/_4$.

Table 26 illustrates the bit delay selection.

	Corresponding Delay Bits				
Data Rate	**BID4**	**BID3**	**BID2**	**BID1**	**BID0**
0 (Default)	0	0	0	0	0
1/4	0	0	0	0	1
1/2	0	0	0	1	0
3/4	0	0	0	1	1
1	0	0	1	0	0
1 1/4	0	0	1	0	1
1 1/2	0	0	1	1	0
1 3/4	0	0	1	1	1
2	0	1	0	0	0
2 1/4	0	1	0	0	1
2 1/2	0	1	0	1	0
2 3/4	0	1	0	1	1
3	0	1	1	0	0
3 1/4	0	1	1	0	1
3 1/2	0	1	1	1	0
3 3/4	0	1	1	1	1

Table 26 - Backplane Input Bit Delay Programming Table

	Corresponding Delay Bits				
Data Rate	**BID4**	**BID3**	**BID2**	**BID1**	**BID0**
4	1	0	0	0	0
4 1/4	1	0	0	0	1
4 1/2	1	0	0	1	0
4 3/4	1	0	0	1	1
5	1	0	1	0	0
5 1/4	1	0	1	0	1
5 1/2	1	0	1	1	0
5 3/4	1	0	1	1	1
6	1	1	0	0	0
6 1/4	1	1	0	0	1
6 1/2	1	1	0	1	0
6 3/4	1	1	0	1	1
7	1	1	1	0	0
7 1/4	1	1	1	0	1
7 1/2	1	1	1	1	0
7 3/4	1	1	1	1	1

Table 26 - Backplane Input Bit Delay Programming Table

13.8 Local Output Advancement Registers (LOAR0 to LOAR31)

Address 0083h to 00A2h.

Thirty-two local output advancement registers (LOAR0 to LOAR31) allow users to program the output advancement for output data streams LSTo0 to LSTo31. The possible adjustment is -2, -4 or -6 cycles of the internal system clock (131.072 MHz).

The LOAR0 to LOAR31 registers are configured as follows:

LOARn Bit (where n = 0 to 31)	**Name**	**Reset**	**Description**
15-2	Reserved	0	**Reserved**
1-0	LOA(1:0)	0	**Local Output Advancement Register**

Table 27 - Local Output Advancement Register (LOARn) Bits

13.8.1 Local Output Advancement Bits 1-0 (LOA1-LOA0)

The binary value of these two bits is the amount of offset that a particular stream output can be advanced. When the advancement is 0, the serial output stream has the normal alignment with the local frame pulse.

Local Output Advancement	Corresponding Advancement Bits	
Clock Rate 131.072 MHz	**LOA1**	**LOA0**
0 (Default)	0	0
-2 cycle	0	1
-4 cycles	1	0
-6 cycles	1	1

Table 28 - Local Output Advancement (LOAR) Programming Table

13.9 Backplane Output Advancement Registers (BOAR0 - 31)

Address 00A3h to 00C2h

Thirty-two Backplane Output Advancement Registers (BOAR0 to BOAR3) allow users to program the output advancement for output data streams BSTo0 to BSTo31. For 2 Mb/s, 4 Mb/s, 8 Mb/s and 16 Mb/s stream operation the possible adjustment is -2, -4 or -6 cycles of the internal system clock (131.072 MHz). For 32 Mb/ s stream operation the possible adjustment is -1, -2 or -3 cycles of the internal system clock (131.072 MHz). The BOAR0 to BOAR3 registers are configured as follows:

BOARn Bit (where n = 0 to 31 for non-32 Mb/s mode, n = 0 to 15 for 32 Mb/s mode)	**Name**	**Reset**	**Description**
15-2	Reserved	0	**Reserved**
1:0	BOA(1:0)	0	**Backplane Output Advancement Register**

Table 29 - Backplane Output Advancement Register (BOAR) Bits

13.9.1 Backplane Output Advancement Bits 1-0 (BOA1-BOA0)

The binary value of these two bits is the amount of offset that a particular stream output can be advanced. When the advancement is 0, the serial output stream has the normal alignment with the backplane frame pulse.

Backplane Output Advancement For 2 Mb/s, 4 Mb/s, 8 Mb/s & 16 Mb/s	Backplane Output Advancement For 32 Mb/s	Corresponding Advancement Bits	
clock Rate 131.072 MHz	**clock Rate 131.072 MHz**	**BOA1**	**BOA0**
0 (Default)	0 (Default)	0	0
-2 cycle	-1 cycle	0	1
-4 cycles	-2 cycle	1	0
-6 cycles	-3 cycle	1	1

Table 30 - Backplane Output Advancement (BOAR) Programming Table

13.10 Local Bit Error Rate (BER) Registers

13.10.1 Local BER Start Send Register (LBSSR)

Address 00C3h.

Local BER Start Send Register defines the output channel and the stream in which the BER sequence starts to be transmitted. The LBSSR register is configured as follows:

Bit	Name	Reset	Description
15-13	Reserved	0	**Reserved.**
12-8	LBSSA(4:0)	0	**Local BER Send Stream Address Bits.** The binary value of these bits refers to the local output stream which carries the BER data.
7-0	LBSCA(7:0)	0	**Local BER Send Channel Address Bits.** The binary value of these bits refers to the local output channel in which the BER data starts to be sent.

Table 31 - Local BER Start Send Register (LBSSR) Bits

13.10.1.1 Local Transmit BER Length Register (LTXBLR)

Address 00C4h

Local BER Transmit Length Register (LTXBLR) defines how many channels the BER sequence will be transmitted during each frame. The LTXBLR register is configured as follows:

Bit	Name	Reset	Description
15-8	Reserved	0	**Reserved**.
7-0	LTXBL(7:0)	0	**Local Transmit BER Length Bits** The binary value of these bits define the number of channels in addition to the Start Channel that the BER data will be transmitted on. (i.e., Total Channels = Start Channel + LTXBL value)

Table 32 - Local BER Length Register (LTXBLR) Bits

13.10.2 Local Receive BER Length Register (LRXBLR)

Address 00C5h

Local BER Receive Length Register (LRXBLR) defines how many channels the BER sequence will be received during each frame. The LRXBLR register is configured as follows:

Bit	Name	Reset	Description
15-8	Reserved	0	**Reserved**.
7-0	LRXBL(7:0)	0	**Local Receive BER Length Bits** The binary value of these bits define the number of channels in addition to the Start Channel allocated for the BER receiver. (i.e., Total Channels = Start Channel + LRXBL value)

Table 33 - Local Receive BER Length Register (LRXBLR) Bits

13.10.3 Local BER Start Receive Register (LBSRR)

Address 00C6h

Local BER Start Receive Register defines the Input Stream and Start Channel and the stream in which the BER sequence shall be received. The LBSRR register is configured as follows:

Bit	Name	Reset	Description
15-13	Reserved	0	**Reserved.**
12-8	LBRSA(4:0)	0	**Local BER Receive Stream Address Bits** The binary value of these bits refers to the local input stream to receive the BER data.
7-0	LBRCA(7:0)	0	**Local BER Receive Channel Address Bits** The binary value of these bits refers to the local input channel in which the BER data starts to be compared.

Table 34 - Local BER Start Receive Register (LBSRR) Bits

13.10.4 Local BER Count Register (LBCR)

Address 00C7h

Local BER Count Register contains the number of counted errors. This register is read only. The LBCR register is configured as follows:

Bit	Name	Reset	Description
15-0	LBC(15:0)	0	**Local Bit Error Rate Count** The binary value of the bits define the Local Bit Error count.

Table 35 - Local BER Count Register (LBCR) Bits

13.11 Backplane Bit Error Rate (BER) Registers

13.11.1 Backplane BER Start Send Register (BBSSR)

Address 00C8h

Backplane BER Start Send Register defines the output channel and the stream in which the BER sequence is transmitted. The BBSSR register is configured as follows:

Bit	Name	Reset	Description
15-14	Reserved	0	**Reserved.**
13-9	BBSSA(4:0)	0	**Backplane BER Send Stream Address Bits** The binary value of these bits define the backplane output stream to transmit the BER data.
8-0	BBSCA(8:0)	0	**Backplane BER Send Channel Address Bits** The binary value of these bits define the backplane output Start Channel in which the BER data is transmitted.

Table 36 - Backplane BER Start Send Register (BBSSR) Bits

13.11.2 Backplane Transmit BER Length Register (BTXBLR)

Address 00C9h

Backplane Transmit BER Length Register (BTXBLR) defines how many channels in each frame the BER sequence will be transmitted. The BTXBLR register is configured as follows:

Bit	Name	Reset	Description
15-9	Reserved	0	**Reserved.**
8-0	BTXBL(8:0)	0	**Backplane Transmit BER Length Bits** The binary value of these bits define the number of channels in addition to the Start Channel allocated for the BER Transmitter. (i.e., Total Channels = Start Channel + BTXBL value)

Table 37 - Backplane Transmit BER Length (BTXBLR) Bits

13.11.3 Backplane Receive BER Length Register (BRXBLR)

Address 00CAh

Backplane Receive BER Length Register (BRXBLR) defines how many channels in each frame the BER sequence will be transmitted. The BRXBLR register is configured as follows:

Bit	Name	Reset	Description
15-9	Reserved	0	**Reserved.**
8-0	BRXBL(8:0)	0	**Backplane Receive BER Length Bits** The binary value of these bits define the number of channels in addition to the Start Channel allocated for the BER receiver. (i.e. Total Channels = Start Channel + BRXBL value)

Table 38 - Backplane Receive BER Length (BRXBLR) Bits

13.11.4 Backplane BER Start Receive Register (BBSRR)

Address 00CBh

Backplane BER Start Receive Register defines the Input Stream and the Start Channel in which the BER sequence shall be received. The BBSRR register is configured as follows:

Bit	Name	Reset	Description
15-14	Reserved	0	**Reserved.**
13-9	BBRSA(4:0)	0	**Backplane BER Receive Stream Address Bits** The binary value of these bits defines the backplane input stream that receives the BER data.
8-0	BBRCA(8:0)	0	**Backplane BER Receive Channel Address Bits** The binary value of these bits define the backplane input start channel in which the BER data will be received.

Table 39 - Backplane BER Start Receive Register (BBSRR) Bits

13.11.5 Backplane BER Count Register (BBCR)

Address 00CCh

Backplane BER Count Register contains the number of counted errors. This register is read only. The BBCR register is configured as follows:

Bit	Name	Reset	Description
15-0	BBC(15:0)	0	**Backplane Bit Error Rate Count** The binary value of these bits define the Backplane Bit Error count.

Table 40 - Backplane BER Count Register (BBCR) Bits

13.12 Local Bit Rate Registers

13.12.1 Local Input Bit Rate Registers (LIBRR0-31)

Address 00CDh to 00ECh

Thirty-two Local Input Bit Rate Registers allow the bit rate for each individual stream, to be set to 2, 4, 8 or 16 Mb/s. The LIBRR registers are configured as follows:

LIBRn (for n=0 to 31)	Name	Reset	Description
15-2	Reserved	0	**Reserved**
1-0	LIBR(1:0)	0	**Local Input Bit Rate**

Table 41 - Local Input Bit Rate Register (LIBRRn) Bits

LIBR1	LIBR0	Bit rate for stream n
0	0	2 Mb/s
0	1	4 Mb/s
1	0	8 Mb/s
1	1	16 Mb/s

Table 42 - Local Input Bit Rate (LIBR) Programming Table

13.12.2 Local Output Bit Rate Resisters (LOBRR0-31)

Address 00EDh to 010Ch

thirty-two Local Output Bit Rate Registers allow the bit rate for each individual stream to be set to 2, 4, 8 or 16 Mb/s. The LOBRR registers are configured as follows:

LOBRn Bit (where n = 0 to 31)	Name	Reset	Description
15-2	Reserved	0	**Reserved**
1-0	LOBR(1:0)	0	**Local Output Bit Rate**

Table 43 - Local Output Bit Rate Register (LOBRRn) Bits

LOBR1	LOBR0	Bit rate for stream n
0	0	2 Mb/s
0	1	4 Mb/s
1	0	8 Mb/s
1	1	16 Mb/s

Table 44 - Output Bit Rate (LOBR) Programming Register

13.13 Backplane Bit Rate Registers

13.13.1 Backplane Input Bit Rate Registers (BIBRR0-31)

Address 010Dh to 012Ch

Thirty-two Backplane Input Bit Rate Registers allow the bit rate for each individual stream to be set to 2, 4, 8 or 16 Mb/s. These registers may be overridden by setting 32 Mb/s mode in the control register, in which case, backplane streams 0-15 will operate at 32 Mb/s and backplane streams 16-31 will be unused. The BIBRR registers are configured as follows:

BIBRn Bit (for n=0 to 31)	Name	Reset	Description
15-2	Reserved	0	**Reserved**
1-0	BIBR(1:0)	0	**Backplane Input Bit Rate**

Table 45 - Backplane Input Bit Rate Register (BIBRRn) Bits

BIBR1	BIBR0	Bit rate for stream n
0	0	2 Mb/s
0	1	4 Mb/s
1	0	8 Mb/s
1	1	16 Mb/s

Table 46 - Backplane Input Bit Rate (BIBR) Programming Table

13.13.2 Backplane Output Bit Rate Registers (BOBRR0-31)

Address 012Dh to 014Ch

Thirty-two Backplane Output Bit Rate Registers allow the bit rate for each individual stream to be set to 2, 4, 8 or 16 Mb/s.These registers may be overridden by setting 32 Mb/s mode in the control register, in which case, backplane streams 0-15 will operate at 32 Mb/s and backplane streams 16-31 will be unused. The BOBRR registers are configured as follows:

BOBRn Bit (for n=0 to 31)	Name	Reset	Description
15-2	Reserved	0	**Reserved**
1-0	BOBR(1:0)	0	**Backplane Output Bit Rate**

Table 47 - Backplane Output Bit Rate Register (BOBRRn) Bits

BOBR1	BOBR0	Bit rate for stream n
0	0	2 Mb/s
0	1	4 Mb/s
1	0	8 Mb/s
1	1	16 Mb/s

Table 48 - Backplane Output Bit Rate (BOBRR) Programming Table

13.14 Memory BIST Register

Address 014Dh

The Memory BIST register enables the built-in-self-test function for the on-chip memory testing. Two consecutive write operations are required to start MBIST. The first with only Bit 12 (LV_TM) set High (i.e., 1000h), the second with Bit 12 maintained High but with the required start bit(s) set High.

The MBISTR register is configured as follows:

Bit	Name	Reset	Description
15-13	Reserved	0	**Reserved.**
12	LV_TM	0	**MBIST Test enable.** High for MBIST mode, Low for scan mode.
11	BISTSDB	0	**Backplane Data Memory Start BIST sequence.** Sequence enabled on LOW to HIGH transition.
10	BISTCDB	0	**Backplane Data Memory BIST sequence completed. (Read only).** High indicates completion of Memory BIST sequence.
9	BISTPDB	0	**Backplane Data Memory Pass/Fail Bit (Read only).** This bit indicates the Pass/Fail status following completion of the Memory BIST sequence. A HIGH indicates Pass, a LOW indicates Fail.
8	BISTSDL	0	**Local Data Memory Start BIST sequence.** Sequence enabled on LOW to HIGH transition.
7	BISTCDL	0	**Local Data Memory BIST sequence completed. (Read only).** High indicates completion of Memory BIST sequence.
6	BISTPDL	0	**Local Data Memory Pass/Fail Bit (Read only).** This bit indicates the Pass/Fail status following completion of the Memory BIST sequence. A HIGH indicates Pass, a LOW indicates Fail.
5	BISTSCB	0	**Backplane Connection Memory Start BIST sequence.** Sequence enabled on LOW to HIGH transition.
4	BISTCCB	0	**Backplane Connection Memory BIST sequence completed. (Read only).** High indicates completion of Memory BIST sequence.
3	BISTPCB	0	**Backplane Connection Memory Pass/Fail Bit (Read only).** This bit indicates the Pass/Fail status following completion of the Memory BIST sequence. A HIGH indicates Pass, a LOW indicates Fail.
2	BISTSCL	0	**Local Connection Memory Start BIST sequence.** Sequence enabled on LOW to HIGH transition.
1	BISTCCL	0	**Local Connection Memory BIST sequence completed. (Read only).** High indicates completion of Memory BIST sequence.
0	BISTPCL	0	**Local Connection Memory Pass/Fail Bit (Read only).** This bit indicates the Pass/Fail status following completion of the Memory BIST sequence. A HIGH indicates Pass, a LOW indicates Fail.

Table 49 - Memory BIST Register (MBISTR) Bits

13.15 Revision Control Register

Address 3FFFh

The revision control register stores the binary value of the silicon revision number. This register is read only. The RCR register is configured as follows:

Bit	Name	Reset Value	Description
15-4	Reserved	0	**Reserved.**
3-0	RC(3:0)	defined by silicon	**Revision Control Bits**

Table 50 - Revision Control Register (RCR) Bits

DC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Core Supply Voltage	V_{DD_CORE}	-0.5	2.5	V
2	I/O Supply Voltage	V_{DD_IO}	-0.5	5.0	V
3	PLL Supply Voltage	V_{DD_PLL}	-0.5	2.5	V
4	Input Voltage (non-5 V tolerant inputs)	V_I	-0.5	V_{DD_IO} +0.5	V
5	Input Voltage (5 V tolerant inputs)	V_{I_5V}	-0.5	7.0	V
6	Continuous Current at digital outputs	I_o		15	mA
7	Package power dissipation	P_D		2	W
8	Storage temperature	T_S	- 55	+125	°C

***** Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

	Characteristics	Sym.	Min.	Typ.	Max.	Units
1	Operating Temperature	T_{OP}	-40	25	+85	°C
2	Positive Supply	V_{DD_IO}	3.0	3.3	3.6	V
3	Positive Supply	V_{DD_CORE}	1.62	1.8	1.98	V
4	Positive Supply	V_{DD_PLL}	1.62	1.8	1.98	V
5	Input Voltage	V_I	0	3.3	V_{DD_IO}	V
6	Input Voltage on 5 V Tolerant Inputs	V_{I_5V}	0	5	5.5	V

Voltages are with respect to ground (V_{SS}) unless otherwise stated.

DC Electrical Parameters

		Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1a 1b	INPUTS	Supply Current	I_{DD_Core}			4	mA	Static I_{DD_Core} and PLL current
		Supply Current	I_{DD_Core}		160	200	mA	Applied clock C8i = 8.192 MHz
1c		Supply Current	I_{DD_IO}			100	µA	Static I_{DD_IO}
1d		Supply Current	I_{DD_IO}			110	mA	I_{AV} with all output streams at max. data-rate
2		Input High Voltage	V_{IH}	2.0			V	
3		Input Low Voltage	V_{IL}			0.8	V	
4		Input Leakage (input pins) Input Leakage (bi-directional pins)	I_{IL} I_{BL}			5 5	µA µA	$0 < V < V_{DD\_IO}$
		Weak Pullup Current	I_{PU}			-200	µA	Input at 0V
5		Weak Pulldown Current	I_{PD}			200	µA	Input at V_{DD_IO}
6		Input Pin Capacitance	C_I			5	pF	
7	OUTPUTS	Output High Voltage	V_{OH}	2.4			V	I_{OH} = 10mA
8		Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 10mA
9		High Impedance Leakage	I_{OZ}			5	µA	$0 \leq V_0 \leq V_{DD\_IO}$
10		Output Pin Capacitance	C_O			5	pF	

Voltages are with respect to ground (V_{SS}) unless otherwise stated.

AC Electrical Characteristics Timing Parameter Measurement: Voltage Levels

	Characteristics	Sym.	Level	Units	Conditions
1	CMOS Threshold	V_{CT}	$0.5V_{DD\_IO}$	V	$3.0V \leq V_{DD\_IO} \leq 3.6V$
2	Rise/Fall Threshold Voltage High	V_{HM}	$0.7V_{DD\_IO}$	V	$3.0V \leq V_{DD\_IO} \leq 3.6V$
3	Rise/Fall Threshold Voltage Low	V_{LM}	$0.3V_{DD\_IO}$	V	$3.0V \leq V_{DD\_IO} \leq 3.6V$

Backplane and Local Clock Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
1	Backplane Frame Pulse Width	$t_{BFPW244}$ $t_{BFPW122}$ t_{BGFPW}	210 10 10	244 122 122	350 220 220	ns	
2	Backplane Frame Pulse Setup Time before C8i clock rising edge	$t_{BFPS244}$ $t_{BFPS122}$ t_{BGFPS}	5 5 5		110 110 110	ns	
3	Backplane Frame Pulse Hold Time from C8i clock rising edge	$t_{BFPH244}$ $t_{BFPH122}$ t_{BGFPH}	5 5 5		110 110 110	ns	
4	$\overline{C8i}$ Clock Period	t_{BCP8}	120	122	124	ns	
5	$\overline{C8i}$ Clock Pulse Width High	t_{BCH8}	50	61	70	ns	
6	$\overline{C8i}$ Clock Pulse Width Low	t_{BCL8}	50	61	70	ns	
7	$\overline{C8i}$ Clock Rise/Fall Time	t_{rBC8i}, t_{fBC8i}	0	2	3	ns	
8	$\overline{C8i}$ Cycle to Cycle Variation	t_{CVC8i}			3	ns	
9	Local Frame Boundary Offset	t_{LFBOS}			7.5	ns	
10	$\overline{FP8o}$ Width	t_{LFPW8} t_{GFPW8}	117 117	122 122	127 127	ns	C_L=60pF
11	$\overline{FP8o}$ Output Delay from edge to Local Frame Boundary	t_{LFODF8} t_{GFPS8o}	56 56		68 56	ns	
12	$\overline{FP8o}$ Output Delay from Local Frame Boundary to Edge	t_{LFODR8} t_{GFPH8o}	59 59		61 61	ns	
13	$\overline{C8o}$ Clock Period	t_{LCP8}	117		127	ns	C_L=60pF
14	$\overline{C8o}$ Clock Pulse Width High	t_{LCH8}	56		68	ns	
15	$\overline{C8o}$ Clock Pulse Width Low	t_{LCL8}	59		61	ns	
16	$\overline{C8o}$ Clock Rise/Fall Time	t_{rLC8o}, t_{fLC8o}	3		7	ns	
17	$\overline{FP16o}$ Width	t_{FPW16}	62		66	ns	C_L=60pF
18	$\overline{FP16o}$ Output Delay from Falling edge to Local Frame Boundary	t_{FODF16}	-29		-36	ns	
19	$\overline{FP16o}$ Output Delay from Local Frame Boundary to Rising edge	t_{FODR16}	30		33	ns	
20	$\overline{C16o}$ Clock Period	t_{LCP16}	62		66	ns	C_L=60pF
21	$\overline{C16o}$ Clock Pulse Width High	t_{LCH16}	29		36	ns	
22	$\overline{C16o}$ Clock Pulse Width Low	t_{LCL16}	30		33	ns	
23	$\overline{C16o}$ Clock Rise/Fall Time	t_{rLC16o}, t_{fLC16o}	0		5	ns	

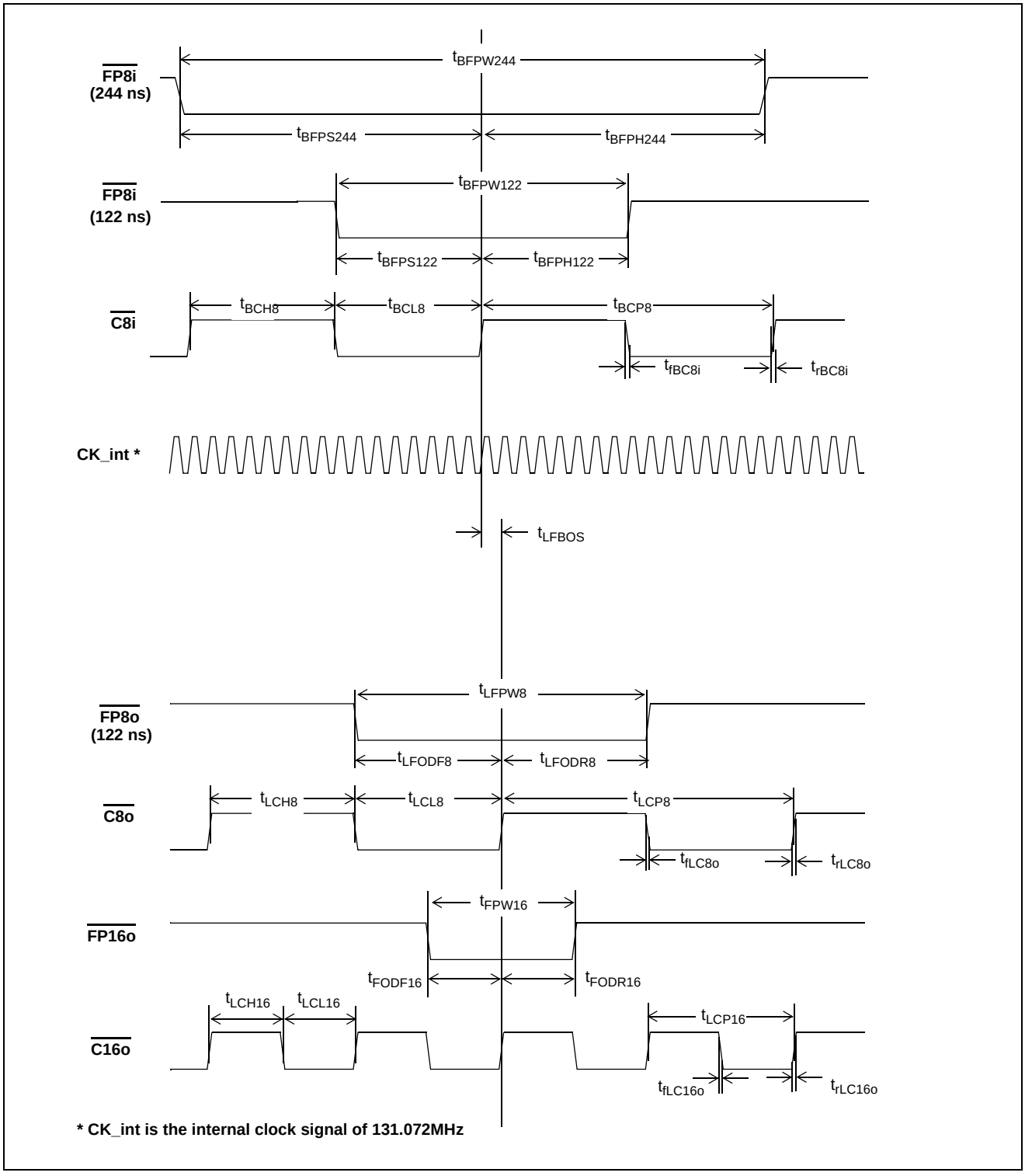


Figure 20 - Backplane and Local Clock Timing Diagram for ST-BUS

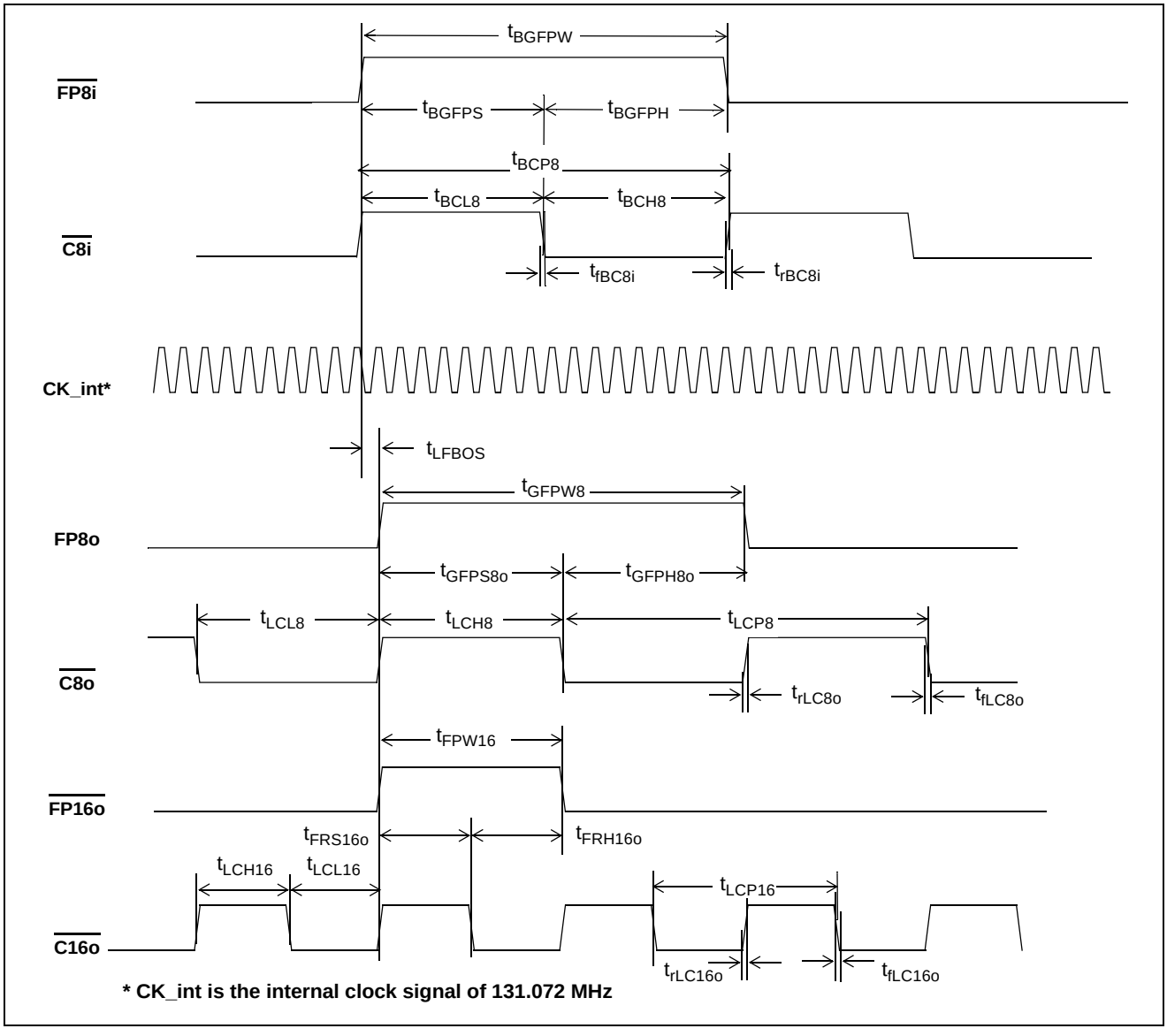


Figure 21 - Backplane and Local Clock Timing for GCI-BUS

Backplane Data Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
1	Backplane Input data sampling point	t_{BIDS32} t_{BIDS16} t_{BIDS8} t_{BIDS4} t_{BIDS2}	18 41 87 178 361	23 46 92 183 366	28 51 97 188 371	ns	With zero offset.
2	Backplane Serial Input Set-up Time	t_{BSIS32} t_{BSIS16} t_{BSIS8} t_{BSIS4} t_{BSIS2}	2.1 2.1 2.1 2.1 2.1			ns	
3	Backplane Serial Input Hold Time	t_{BSIH32} t_{BSIH16} t_{BSIH8} t_{BSIH4} t_{BSIH2}	3 3 3 3 3			ns	
4	Backplane Serial Output Delay	t_{BSOD32} t_{BSOD16} t_{BSOD8} t_{BSOD4} t_{BSOD2}	0 0 0 0 0		10.5 10.5 10.5 10.5 10.5	ns	C_L=50pF

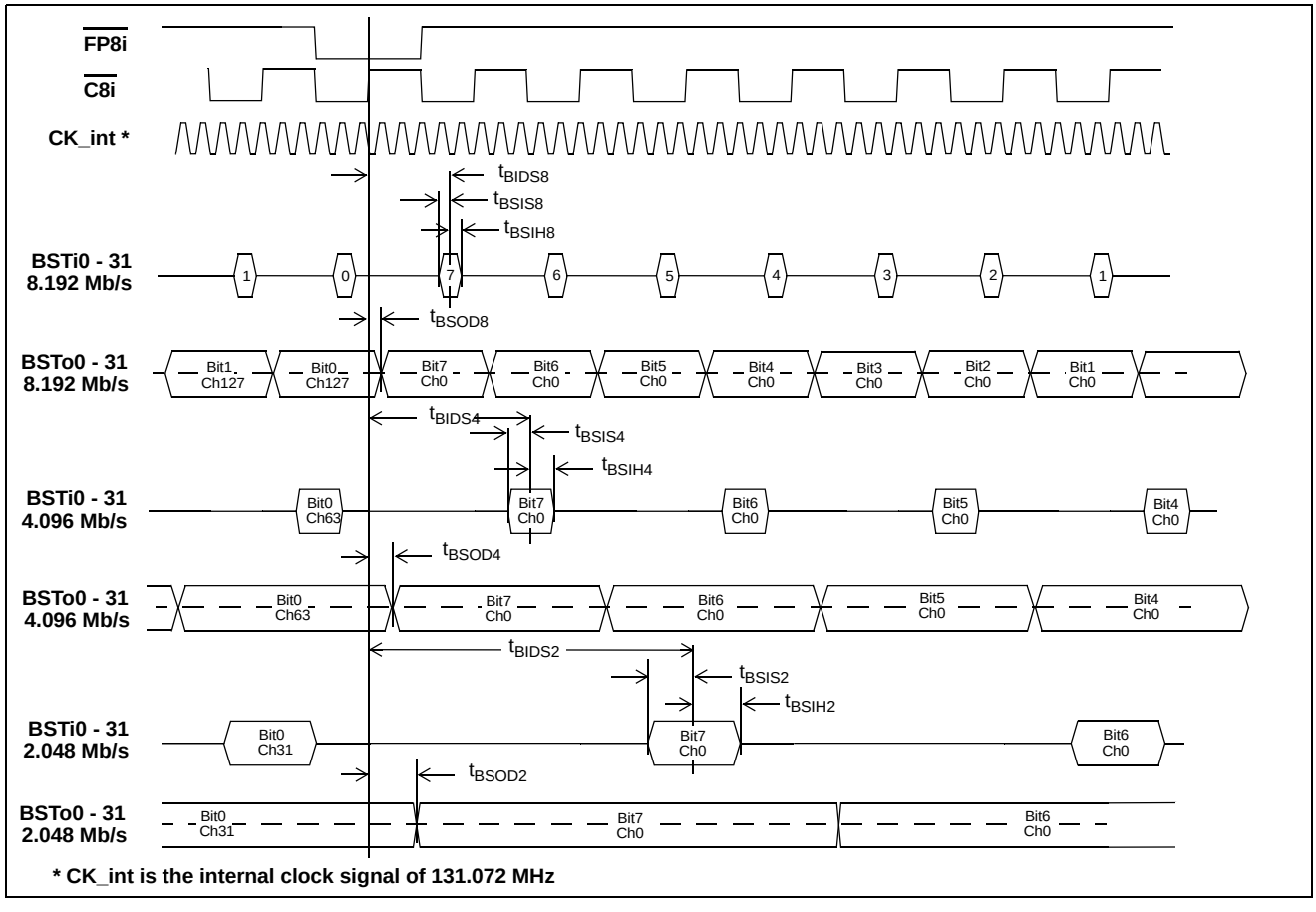


Figure 22 - ST-BUS Backplane Data Timing Diagram (8 Mb/s, 4 Mb/s, 2 Mb/s)

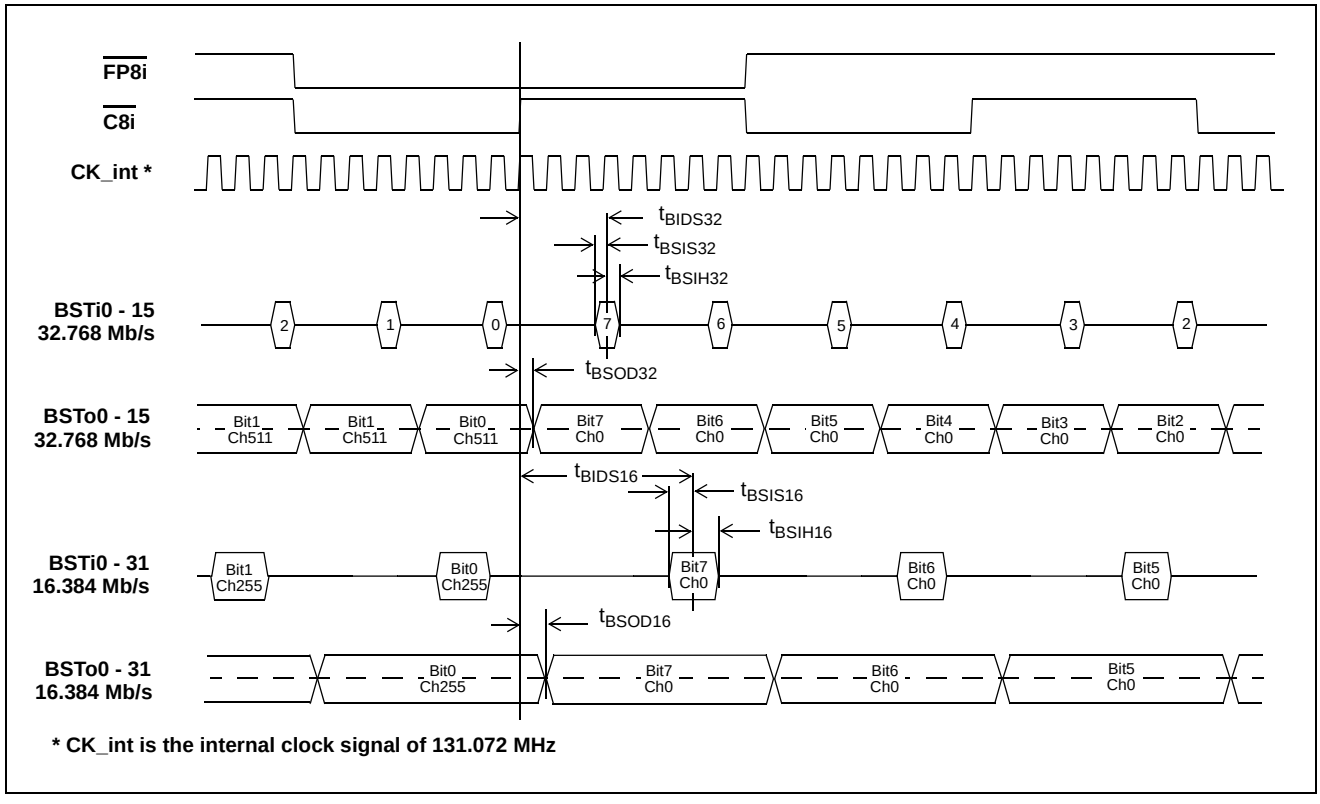


Figure 23 - ST-BUS Backplane Data Timing Diagram (32 Mb/s, 16 Mb/s)

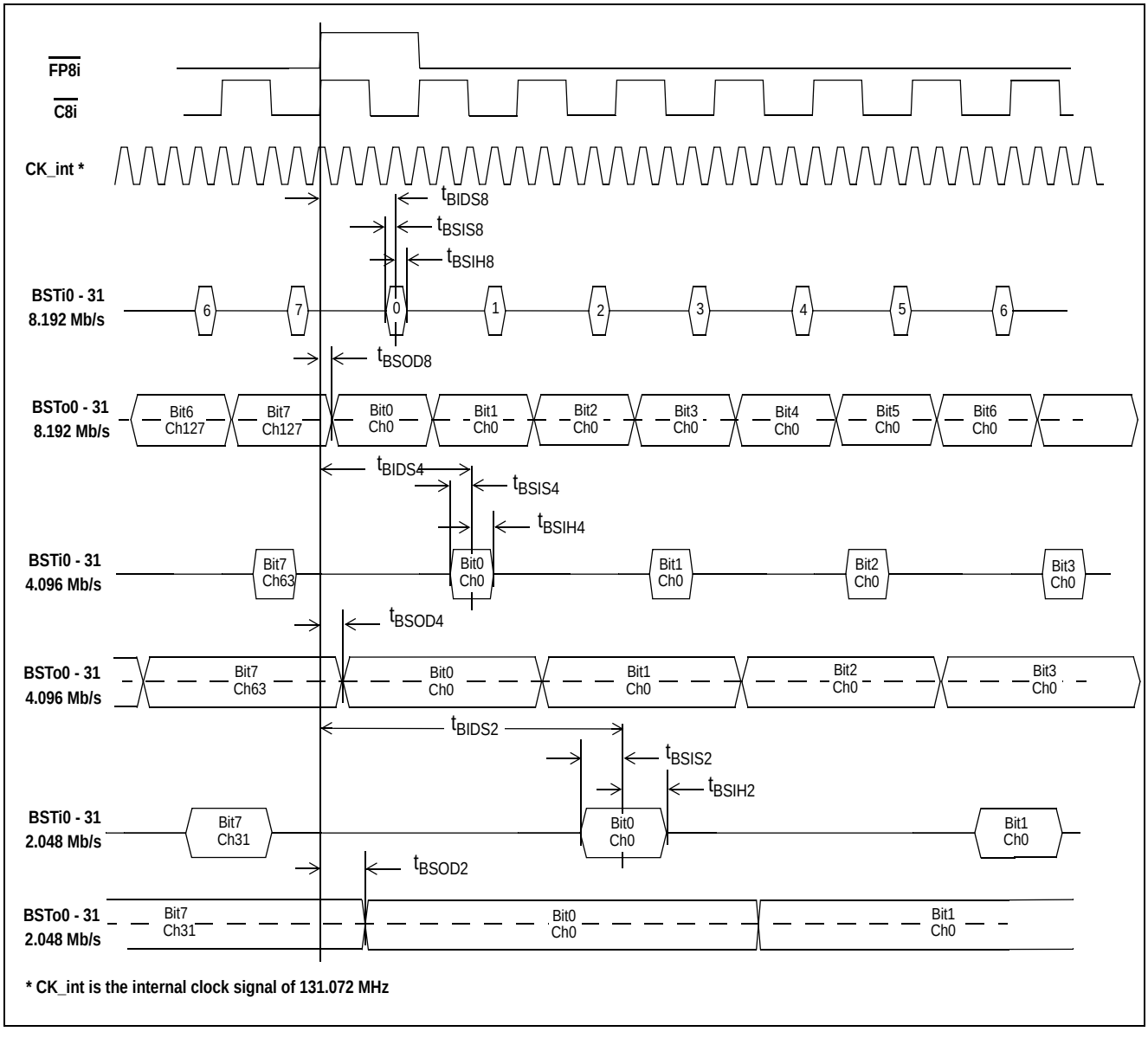


Figure 24 - GCI BUS Backplane Data Timing Diagram (8 Mb/s, 4 Mb/s, 2 Mb/s)

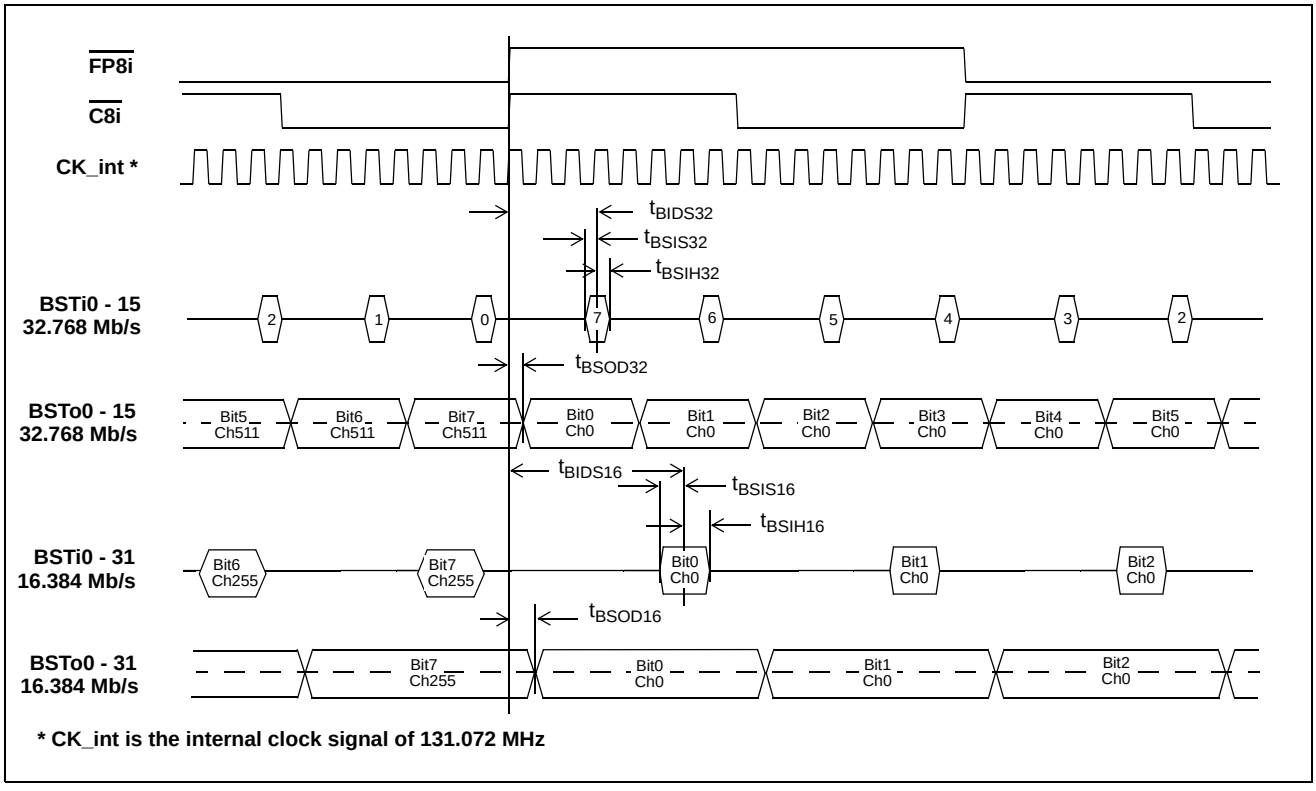


Figure 25 - GCI BUS Backplane Data Timing Diagram (32 Mb/s, 16 Mb/s)

Local Clock Data Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
1	Local Frame Boundary Offset	t_{LFBOS}			7.5	ns	
2	Input data sampling point	t_{LIDS16} t_{LIDS8} t_{LIDS4} t_{LIDS2}	41 87 178 361	46 92 183 366	51 97 188 371	ns	With zero offset.
3	Local Serial Input Set-up Time	t_{LSIS16} t_{LSIS8} t_{LSIS4} t_{LSIS2}	2.1 2.1 2.1 2.1			ns	
4	Local Serial Input Hold Time	t_{LSIH16} t_{LSIH8} t_{LSIH4} t_{LSIH2}	3 3 3 3			ns	
5	Local Serial Output Delay	t_{LSOD16} t_{LSOD8} t_{LSOD4} t_{LSOD2}	0 0 0 0		10.5 10.5 10.5 10.5	ns	C_L=50pF

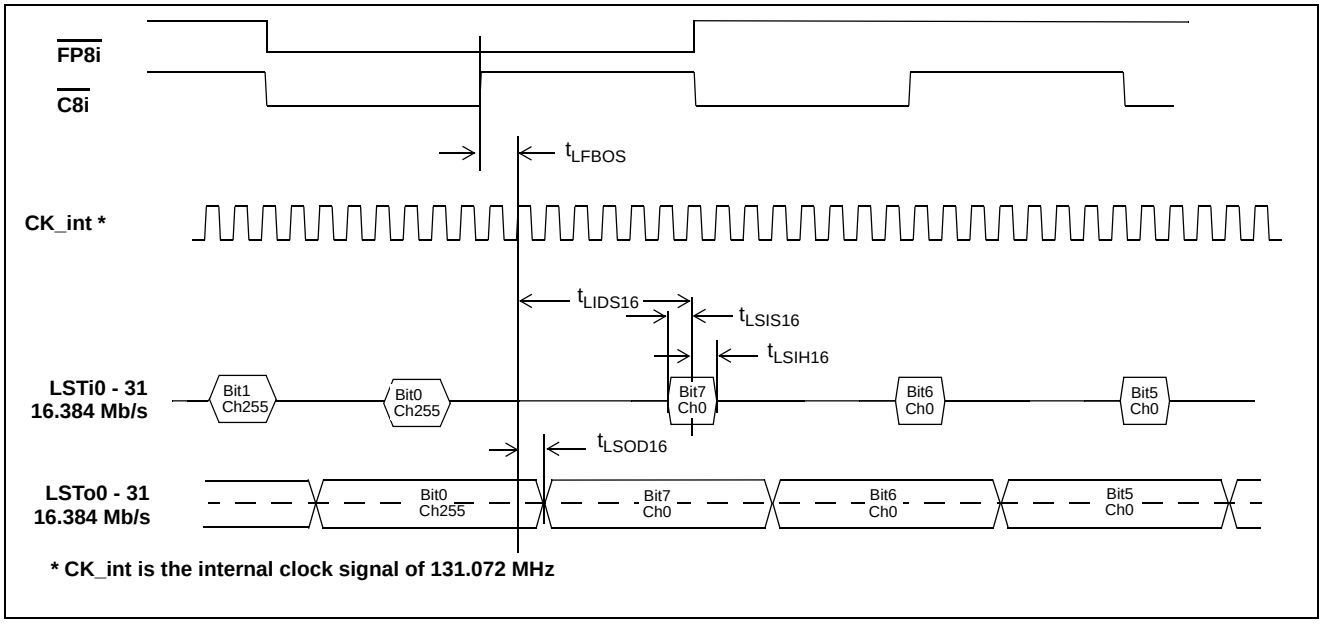


Figure 26 - ST-BUS Local Timing Diagram (16 Mb/s)

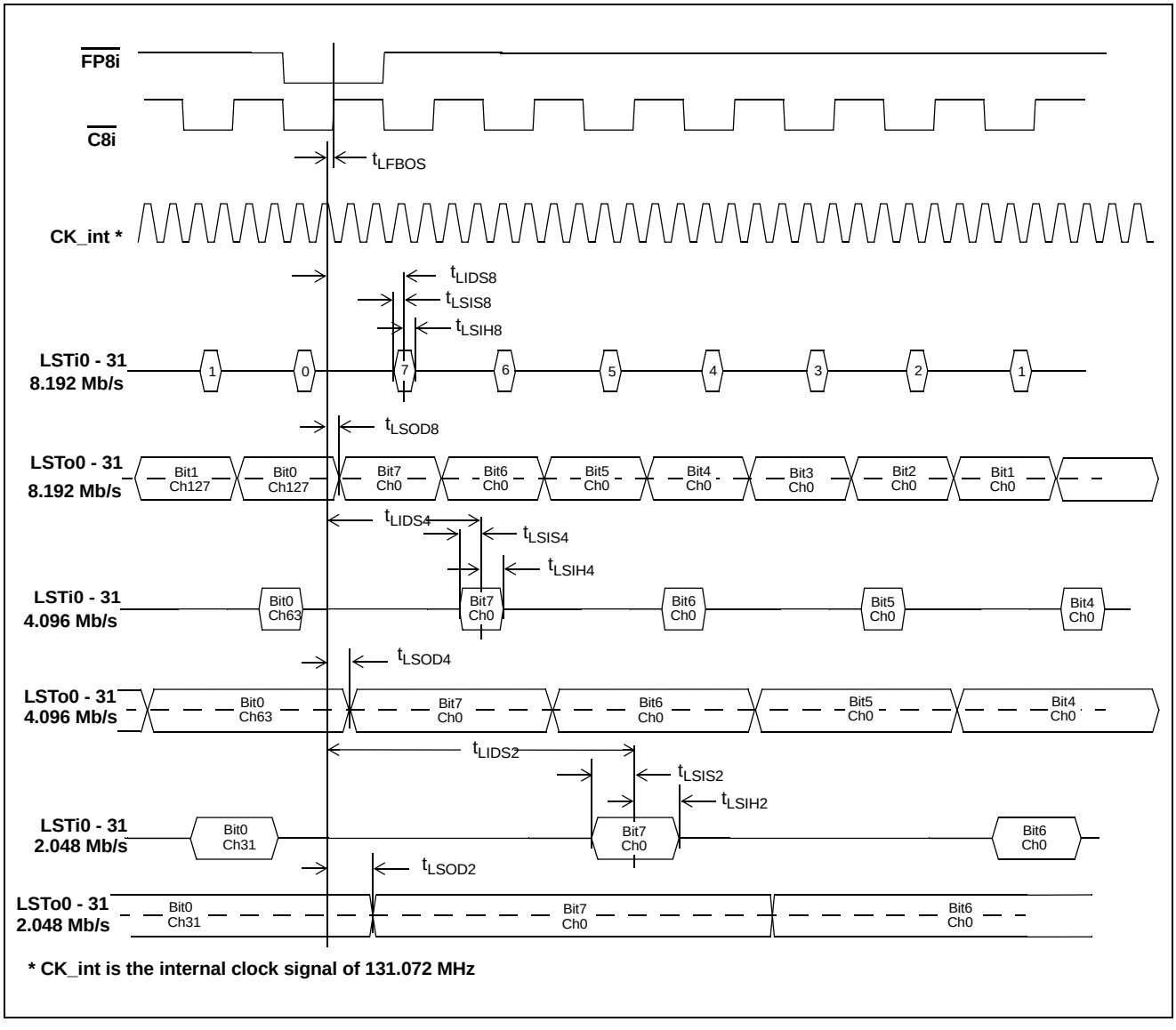


Figure 27 - ST-BUS Local Data Timing Diagram (8 Mb/s, 4 Mb/s, 2 Mb/s)

Backplane and Local Output High-Impedance Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	STo delay - Active to High-Z - High-Z to Active	t_{DZ} t_{ZD}			4 4	ns ns	R_L=1K, C_L=50pF, See Note 1
2	Output Driver Enable (ODE) Delay to Active Data Output Driver Enable (ODE) Delay to High-Impedance	t_{ODE} t_{ODZ}			15 14	ns ns	R_L=1K, C_L=50pF, See Note 1 R_L=1K, C_L=50pF, See Note 1

Note 1: High Impedance is measured by pulling to mid-rail with R_L = 1k//1k potential divider, with timing corrected for C_L.

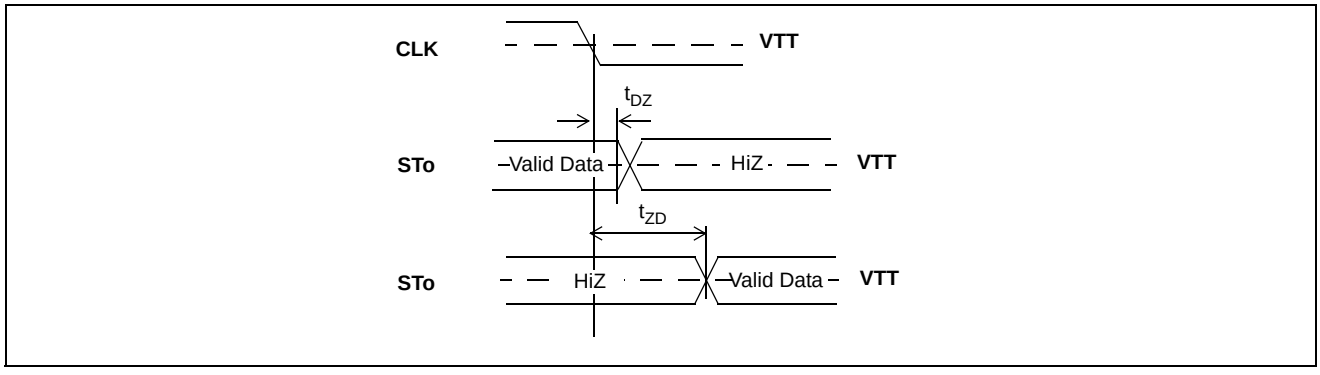


Figure 28 - Serial Output and External Control

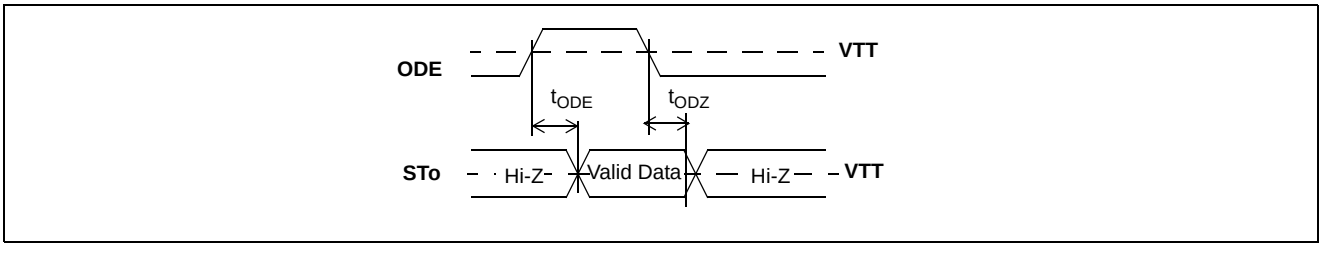


Figure 29 - Output Driver Enable (ODE)

Non-Multiplexed Microprocessor Port Timing

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	$\overline{CS}$ setup from $\overline{DS}$ falling	t_{CSS}	0			ns	
2	R/$\overline{W}$ setup from $\overline{DS}$ falling	t_{RWS}	8			ns	
3	Address setup from $\overline{DS}$ falling	t_{ADS}	8			ns	
4	$\overline{CS}$ hold after $\overline{DS}$ rising	t_{CSH}	0			ns	
5	R/$\overline{W}$ hold after $\overline{DS}$ rising	t_{RWH}	8			ns	
6	Address hold after $\overline{DS}$ rising	t_{ADH}	8			ns	
7	Data setup from $\overline{DTA}$ Low on Read	t_{DDR}	14			ns	C_L=60pF
8	Data hold on read	t_{DHR}			30	ns	C_L=60pF, R_L=1K Note 1
9	Data setup on write	t_{WDS}	8			ns	
10	Data hold on write	t_{DHW}	8			ns	
11	Acknowledgment Delay: Reading/Writing Registers Reading/Writing Memory	t_{AKD}			 85 70	 ns ns	 C_L=60pF C_L=60pF
12	Acknowledgment Hold Time	t_{AKH}			12	ns	C_L=60pF, R_L=1K, Note 1

Note1: High impedance is measured by pulling to the appropriate rail with R_L= 1k//1k potential divider, with timing corrected to cancel time taken to discharge C_L.

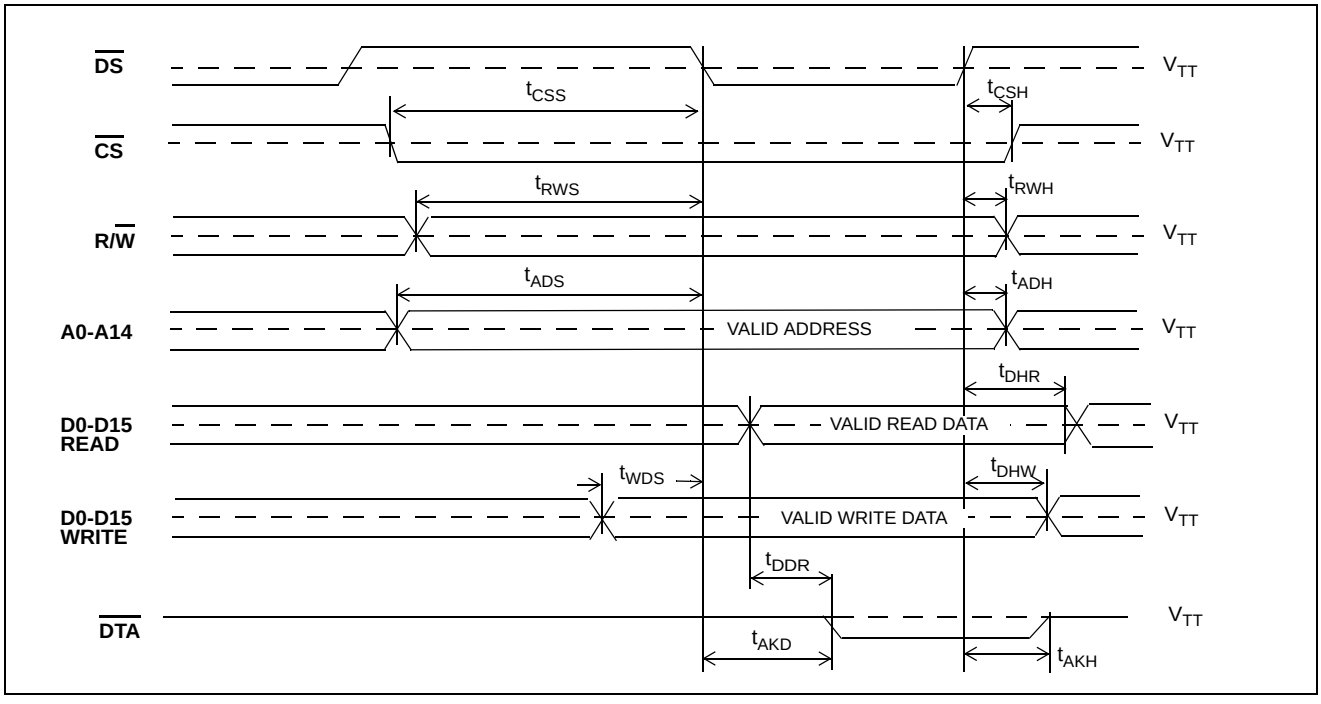
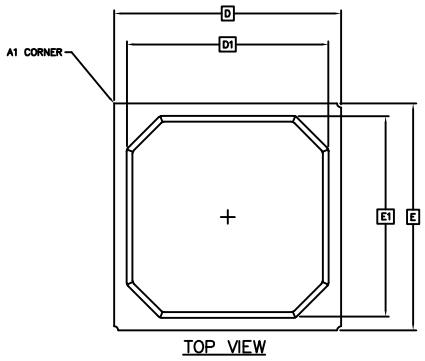
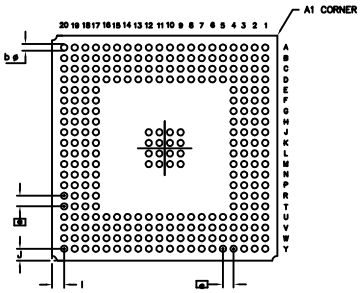


Figure 30 - Motorola Non-Multiplexed Bus Timing

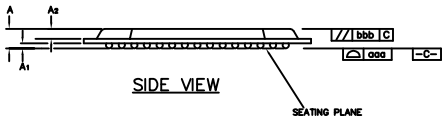
Note: There must be a minimum of 30 ns between CPU accesses, to allow the MT90869 device to recognize the accesses as separate (i.e., a minimum of 30 ns must separate the de-assertion of $\overline{DTA}$ (to high) and the assertion of $\overline{CS}$ and/or $\overline{DS}$ (to initiate the next access).



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SEATING PLANE

DIMENSION	MIN	MAX
A	1.92	2.32
A1	0.50	0.70
A2	1.12	1.22
D	26.80	27.20
D1	---	24.70
E	26.80	27.20
E1	---	24.70
I	1.44 REF.	
J	1.44 REF.	
b	0.60	0.90
e	1.27 BSC	
N	272	
2 LAYERS: substrate thickness is 0.36		

Conforms to JEDEC MS-034 BAL-2 Iss. A

NOTE:
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER
3. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. ALL DIMENSIONS ARE IN MILLIMETERS.

ISSUE	1	2	3	
DATE	12/17/10			
APPRD.	J. Kelly			

ZARLINK SEMICONDUCTOR

Previous package codes:
BP / G

Package Code GA

Package Outline for 272 Ball PBGA (27 x 27mm)

22-0016

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