



EFM32 Zero Gecko

EFM32ZG Errata



This document contains information on the errata of EFM32ZG. The latest available revision of this device is revision A.

For errata on older revisions, please refer to the errata history section for the device. The device revision is typically the first letter on the line immediately under the part number on the package marking. This is typically the second or third line.

Errata effective date: April 10th, 2017.

1. Active Errata Summary

These tables lists all known errata for the EFM32ZG and all unresolved errata in revision A of the EFM32ZG.

Table 1.1. Errata History Overview

Designator	Title/Problem	Exists on Re- vision:
		A
DI_E103	Flash Page Size	X
EMU_E109	Potential Brown Out in EM2	X
EMU_E110	Potential Hard Fault when Exiting EM2	X
IDAC_E101	IDAC Output Current Degradation	X
PCNT_E102	PCNT Pulse Width Filtering Does Not Work	X
RMU_E101	POR Calibration Initialization Issue	X
TIMER_E103	Capture/Compare Output is Unreliable with RSSCOIST Enabled	X

Table 1.2. Active Errata Status Summary

Errata #	Designator	Title/Problem	Workaround	Affected	Resolution
			Exists	Revision	
1	IDAC_E101	IDAC Output Current Degradation	Yes	A	—
2	DI_E103	Flash Page Size	Yes	A	—
3	EMU_E109	Potential Brown Out in EM2	Yes	A	—
4	EMU_E110	Potential Hard Fault when Exiting EM2	Yes	A	A, targeted for Q4 2017
5	PCNT_E102	PCNT Pulse Width Filtering Does Not Work	No	A	—
6	RMU_E101	POR Calibration Initialization Issue	Yes	A	A devices (date code \geq 1537 and PROD_REV \geq 0x89), B
7	TIMER_E103	Capture/Compare Output is Unreliable with RSSCOIST Enabled	No	A	—

2. Detailed Errata Descriptions

2.1 IDAC_E101 — IDAC Output Current Degradation

Description of Errata
The current output of the IDAC might degrade over time.
Affected Conditions / Impacts
Due to an undefined shut-down state of the IDAC, powered devices that do not use the IDAC continuously might experience some degradation in the current output over the lifetime of the device. The degradation is very small when the device is used at room temperature, but the output current will fall well outside specs if the device is exposed to higher temperatures for longer periods of time.
Workaround
If the IDAC output current stability is crucial to the application, the IDAC should never be completely disabled while the device is powered. Leaving the IDAC enabled in the lowest output code setting with duty-cycling enabled consumes ~50 nA extra current and eliminates the problem.
Resolution
There is currently no resolution for this issue.

2.2 DI_E103 — Flash Page Size

Description of Errata
The MEM_INFO_PAGE_SIZE value stored in the Device Information (DI) Page is incorrect.
Affected Conditions / Impacts
For devices with PROD_REV values of 23 or lower, the MEM_INFO_PAGE_SIZE register value in the Device Information Page is incorrect.
Workaround
Use fixed flash page size of 1024 bytes.
Resolution
There is currently no resolution for this issue.

2.3 EMU_E109 — Potential Brown Out in EM2

Description of Errata
There is an error with the calibration algorithm for a voltage regulator that is active during EM2 mode.
Affected Conditions / Impacts
There is an error with the calibration algorithm for a voltage regulator that is active during EM2 mode. This error can, in rare instances, cause the device to brown out and reset while operating in EM2 mode.
Workaround
The issue has been corrected with an updated and validated test program. Devices with a date code greater than or equal to 1626 have been tested with the corrected test program.
Firmware can also work around this issue by writing the calibration value for the low current regulator active in EM2 to 0x6 after any reset or wakeup from EM4. More information on this firmware workaround including example code can be found at the following KB article URL:
http://community.silabs.com/t5/32-bit-MCU-Knowledge-Base/EMU-E109-Potential-Brown-Out-in-EM2/ta-p/176459
Resolution
The issue has been corrected with an updated and validated test program. Devices with a date code and PROD_REV greater than or equal to 1626 and 0x8B respectively have been tested with the corrected test program.

2.4 EMU_E110 — Potential Hard Fault when Exiting EM2

Description of Errata
The flash is powered down in EM2 to save power. Some control registers in the flash can rarely enter an invalid state upon power-on, causing the first read of flash to be incorrect. If this occurs after exiting EM2, the core attempts to fetch the interrupt address, but the value will be incorrect and may be invalid. In the case of an invalid value, the core will then jump to the hard fault handler for attempting to execute code from an invalid address. All subsequent reads from the flash are unaffected, and it is only the first flash read after exit from EM2 that is potentially erroneous.
Affected Conditions / Impacts
When exiting EM2, some devices may intermittently execute code incorrectly or enter the hard fault handler instead of entering the expected ISR associated with the wake source.
Workaround
To workaround this issue, move the interrupt vector table and interrupt service routines for EM2 wake sources to RAM and perform a dummy read of the flash in the ISR. Additional information on the workaround and examples provided is available from the following Knowledge Base article URL: http://community.silabs.com/t5/32-bit-MCU-Knowledge-Base/EMU-E110-Potential-Hard-Fault-when-Exiting-EM2/ta-p/192479 This workaround will be included in v5.3.0 or later of the Gecko SDK, which will be included in the v1.1.0 Gecko SDK Suite.
Resolution
This issue will be resolved in future devices, but the date code of the fixed devices is not yet available. These devices are currently targeted to be available in Q4 2017. The Knowledge Base article will be updated as soon as the specific date code information is available.

2.5 PCNT_E102 — PCNT Pulse Width Filtering Does Not Work

Description of Errata
PCNT pulse width filtering does not work.
Affected Conditions / Impacts
The PCNT pulse width filter does not work as intended.
Workaround
Do not use the pulse width filter, i.e. ensure FILT = 0 in PCNTn_CTRL.
Resolution
There is currently no resolution for this issue.

2.6 RMU_E101 — POR Calibration Initialization Issue

Description of Errata
Upon initial power-on, some devices may not be able to access flash memory above the 4 kB boundary, or some calibration registers on some devices may not be set to their factory calibration values.
Affected Conditions / Impacts
The list of affected devices can be found in the Knowledge Base (KB) article listed under Fix/Workaround. Some devices are sensitive to the power supply ramp during initial power-on. Specific ramp profiles on these devices can cause an intermittent issue resulting in one of two failure modes (A) or (B): A. Flash memory above the 4 kB boundary is inaccessible. Reads of the flash will return zeros. Write attempts will return an invalid address error code in the MSC_STATUS register. Code execution will behave as though the memory above 4 kB was filled with zeros until the device resets itself. B. Some parts of the calibration initialization process do not complete successfully. On USB devices, the USB voltage regulator does not get calibrated. Specific peripheral registers that may not be calibrated are as follows (not all registers apply to all devices): ADC0_CAL, IDAC_CAL, DAC0_CAL, DAC0_BIASPROG, DAC0_OPACTRL, and DAC0_OPAOFFSET. A SYSRESETREQ reset will clear either failure mode, and the device will behave normally until the next power-on event.
Workaround
Additional information including a software workaround is available from the following KB article URL: http://community.silabs.com/t5/32-bit-MCU-Knowledge-Base/POR-calibration-initialization-issue/ta-p/154716
Resolution
Devices with a date code and PROD_REV greater than or equal to 1537 and 0x89 respectively will not have this issue.

2.7 TIMER_E103 — Capture/Compare Output is Unreliable with RSSCOIST Enabled

Description of Errata
The TIMER capture/compare output is unreliable when RSSCOIST is enabled and the clock is prescaled.
Affected Conditions / Impacts
When RSSCOIST is set and PRESC > 0 in TIMERN_CTRL, the capture/compare output value is not reliable.
Workaround
Do not use a prescaled clock, i.e. ensure PRESC = 0 in TIMERN_CTRL when RSSCOIST is enabled.
Resolution
There is currently no resolution for this issue.

3. Errata History

This section contains the errata history for EFM32ZG devices.

For errata on latest revision, please refer to the beginning of this document. The device data sheet explains how to identify chip revision, either from package marking or electronically.

3.1 Errata History Summary

This table lists all resolved errata for the EFM32ZG.

Table 3.1. Errata History Status Summary

Errata #	Designator	Title/Problem	Workaround Exists	Affected Revision	Resolution
There are no errata in the errata history for this device.					

4. Revision History

4.1 Revision 0.40

April 10th, 2017

Added EMU_E110.

Updated errata formatting.

Merged all errata documents for EFM32ZG devices into one document.

Merged errata history and errata into one document.

4.2 Revision 0.30

August 12th, 2016

Added EMU_E109.

4.3 Revision 0.20

October 5th, 2015

Added DI_E103, TIMER_E103, PCNT_E102, and RMU_E101.

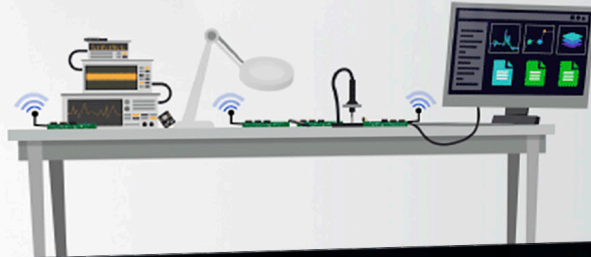
4.4 Revision 0.10

November 20th, 2013

Initial preliminary release.

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Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

<http://www.silabs.com>