TFA9800J

2 × 7 W stereo power amplifier

Rev. 01 — 17 March 2006 Preliminary data sheet

1. General description

The TFA9800 is an integrated class-AB dual output amplifier in a 9-pin DIL-bent-SIL (DBS9P) power package. The device is primarily developed for CRT and multi-media applications.

2. Features

- Requires very few external components
- High output power
- Fixed gain
- Good ripple rejection
- Mute/standby switch
- AC and DC short-circuit safe to ground and V_P
- Thermally protected
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Electrostatic discharge protection

3. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_P	supply voltage	operating	[1]	6.0	15.0	18.0	V
		no output signal	[1]	-	-	20.0	V
I_{ORM}	repetitive peak output current			-	-	2.5	A
$I_{q(tot)}$	total quiescent current			-	40	80	mA
I_{stb}	standby current			-	-	100	µA
$\|Z_i\|$	input impedance			50	60	75	kΩ
P_o	output power	R_L = 4 Ω; THD = 0.5 %	[2]	4.5	5.5	-	W
		R_L = 4 Ω; THD = 10 %	[2]	6.0	7.0	-	W
SVRR	supply voltage rejection ratio	on; f_i = 100 Hz to 10 kHz		48	-	-	dB
α_{cs}	channel separation	R_S = 10 kΩ		40	-	-	dB

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Table 1: Quick reference data *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_v	voltage gain	closed loop	19	20	21	dB
$V_{n(o)(rms)}$	noise output voltage (RMS value)	on; R_S = 0 Ω; f_i = 20 Hz to 20 kHz	-	50	-	μV
T_j	junction temperature		-	-	150	°C

[1] The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 V to 18 V.

[2] Output power is measured directly at the output pins of the TFA9800J.

4. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TFA9800J	DBS9P	plastic DIL-bent-SIL power package; 9 leads (lead length 12/11 mm); exposed die pad	SOT523-1

5. Block diagram

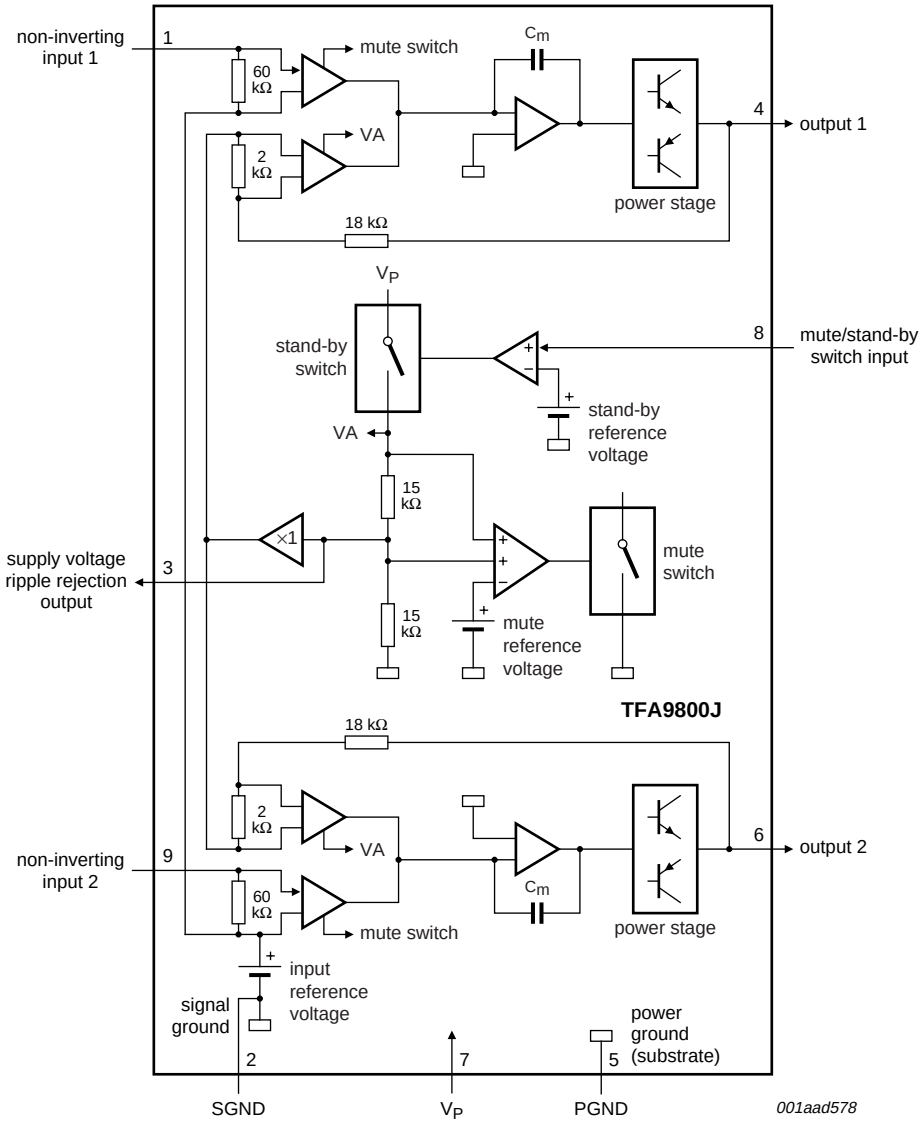


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

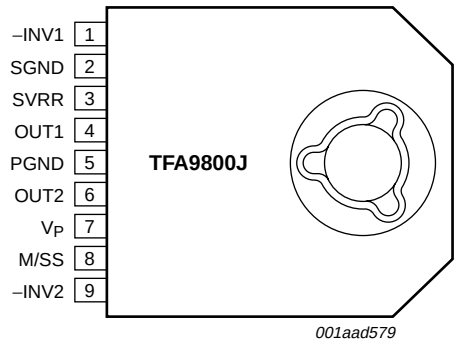


Fig 2. Pin configuration SOT523-1

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
–INV1	1	non-inverting input 1
SGND	2	signal ground
SVRR	3	supply voltage ripple rejection output
OUT1	4	output 1
PGND	5	power ground
OUT2	6	output 2
V_P	7	supply voltage
M/SS	8	mute/standby switch input
–INV2	9	non-inverting input 2

7. Functional description

The TFA9800J contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 20 dB. A special feature of the device is the mute/standby switch which has the following features:

- Low standby current (< 100 μA)
- Low mute/standby switching current (low cost supply switch)
- Mute condition

8. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_P	supply voltage	operating	[1]	6.0	15.0	18.0
		no output signal	[1]	-	-	20.0
$V_{P(sc)}$	short-circuit supply voltage			-	18	V
$V_{P(r)}$	reverse supply voltage			-	6	V
$E_{hand(O)}$	energy handling capacity at outputs	V_P = 0 V		-	200	mJ
I_{OSM}	non-repetitive peak output current			-	4	A
I_{ORM}	repetitive peak output current			-	2.5	A
P_{tot}	total power dissipation			-	25	W
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
T_j	junction temperature			-	150	°C

[1] The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 V to 18 V.

9. Thermal characteristics

Table 5: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case		4	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W

10. Static characteristics

Table 6: Static characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_P	supply voltage		[1]	6.0	15	18.0	V
$I_{q(tot)}$	total quiescent current			-	40	80	mA
I_{stb}	standby current			-	-	100	µA
V_O	output voltage			-	7.2	-	V
Mute/standby switch							
$I_{I(sw)}$	switch input current			-	12	40	µA

Table 6: Static characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th(on)}$	on threshold voltage		8.5	-	-	V
$V_{th(mute)}$	mute threshold voltage		3.3	-	6.4	V
$V_{th(stb)}$	standby threshold voltage		0	-	2	V

[1] The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 V to 18 V.

11. Dynamic characteristics

Table 7: Dynamic characteristics

V_P = 15 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in Figure 3; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	R_L = 4 Ω; THD = 0.5 %	[1]	4.5	5.5	-	W
		R_L = 4 Ω; THD = 10 %	[1]	6.0	7.0	-	W
THD	total harmonic distortion	P_o = 1 W		-	0.1	-	%
$f_{-3db(l)}$	low frequency −3 dB point		[2]	-	45	-	Hz
$f_{-1db(h)}$	high frequency −1 dB point			20	-	-	kHz
G_v	voltage gain	closed loop		19	20	21	dB
$\lvert\Delta G_v\rvert$	voltage gain difference			-	0.1	1	dB
SVRR	supply voltage rejection ratio	f_i = 100 Hz to 10 kHz					
		on	[3]	48	-	-	dB
		mute	[3]	48	-	-	dB
		standby	[3]	80	-	-	dB
$\lvert Z_i\rvert$	input impedance			50	60	75	kΩ
$V_{n(o)(rms)}$	noise output voltage (RMS value)	f_i = 20 Hz to 20 kHz					
		on; R_S = 0 Ω	[4]	-	50	-	μV
		on; R_S = 10 kΩ	[4]	-	70	100	μV
		mute	[5]	-	50	-	μV
$V_{O(mute)}$	mute output voltage	$V_{I(max)}$ = 1 V; f_i = 20 Hz to 15 kHz		-	-	2	mV
α_{cs}	channel separation	R_S = 10 kΩ		40	-	-	dB

[1] Output power is measured directly at the output pins of the IC.

[2] Frequency response externally fixed.

[3] Ripple rejection measured at the output with a source impedance of 0 Ω, maximum ripple amplitude of 2 V (p-p) and a frequency between 100 Hz and 10 kHz.

[4] Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.

[5] Noise output voltage independent of R_S (V_I = 0 V).

12. Application information

12.1 Printed-Circuit Board (PCB) layout and grounding

For high system performance level, certain grounding techniques are imperative. The input reference grounds have to be tied with their respective source grounds and must have separate traces from the power ground traces; this will prevent the large (output) signal currents from interfering with the small AC input signals. The small-signal ground traces should be physically located as far as possible from the power ground traces. The width of supply and output traces should be as large as practical for delivering maximum output power.

Proper supply bypassing is critical for low noise performance and high power supply rejection. The respective capacitor locations should be as close as possible to the device and grounded to the power ground. Proper power supply decoupling also prevents oscillations. For suppressing higher frequency transients (spikes) on the supply line a capacitor with low Equivalent Series Resistance (ESR), typical 0.1 μF, has to be placed as close as possible to the device. For suppressing lower frequency noise and ripple signals, a large electrolytic capacitor, e.g. 1000 μF or greater, must be placed close to the TFA9800J.

In a single-ended (stereo) application a bypass capacitor on the SVRR pin reduces the noise and ripple on the mid-rail voltage. For good THD and noise performance a low ESR capacitor is recommended.

12.2 Input configuration

It should be noted that the DC level of the input pins is about 2.1 V, therefore a coupling capacitor is necessary.

The input cut-off frequency is: $f_i = \frac{1}{2\pi R_i C_i} \Rightarrow f_i = \frac{1}{2\pi \times 30 \times 10^3 \times 220 \times 10^{-9}} = 24\ Hz$

This calculation shows that it is not necessary to use high capacitor values for the input; so the delay during switch-on, which is necessary for charging the input capacitors, can be minimized. This results in a good low frequency response and good switch-on behavior.

For stereo application (single-ended) coupling capacitors on both input and output are necessary.

12.3 Built-in protection circuits

The TFA9800J contains two kinds of protection circuits:

- Short-circuit of outputs to ground, supply and across the load: short-circuit is detected and controlled by a Safe Operating ARea (SOAR) protection circuit.
- Thermal shutdown protection: the junction temperature is measured by a temperature sensor; at a junction temperature of > 150 °C, thermal fold back is activated.

12.4 Output power

The output power versus supply voltage has been measured on the output pins and at THD = 10 %. The maximum output power is limited by the maximum allowable power dissipation and the maximum available output current: 2.5 A repetitive peak current; see Figure 13.

12.5 Supply voltage ripple rejection

The SVRR has been measured with an electrolytic capacitor of 100 μF on pin 3 and at a bandwidth of 10 Hz to 80 kHz. Both curves for operating and mute condition were measured with R_S = 25 Ω; see Figure 9.

12.6 Headroom

A typical music CD requires at least 12 dB (= factor 15.85) dynamic headroom compared with the average power output for passing the loudest portions without distortion. The following calculation can be made for this application at V_P = 15 V and R_L = 4 Ω:

P_o at THD = 0.2 % is about 4.5 W; see Figure 7. Average Listening Level (ALL) without any distortion yields: P_o = 4.5 W / 15.85 = 284 mW. From Figure 11, the power dissipation can be derived for a headroom of 0 dB and 12 dB respectively:

Table 8: Power rating

Condition	Headroom	Power dissipation
P_o = 4.5 W at THD = 0.2 %	0 dB	6 W
	12 dB	4 W

So for average listening level music power, a power dissipation of 4 W can be used for the thermal behavior calculation as described in Section 12.9 “Thermal behavior”.

12.7 Pin M/SS

For the three functional modes: Standby mode, Mute mode, and Operating mode, pin M/SS can be driven by a 3-state logic output stage, e.g. microcontroller with some extra components for DC-level shifting; see Figure 10 for the respective DC levels.

- Standby mode is activated by a low DC level, between 0 V and 2 V on pin M/SS. The power consumption of the TFA9800J will be reduced to < 0.1 mW
- Mute mode will be activated by a DC level between 3.3 V and 6.4 V. The outputs of the amplifier will be muted (no audio output), however the amplifier is DC biased and the DC level of the output pins remains on half the supply voltage. The input coupling capacitors are charged when in Mute mode to avoid plop noise.
- The TFA9800J will be in Operating mode at pin M/SS voltages between 8.5 V and V_P

12.8 Switch on and switch off

To avoid audible plops during switch on or switch off of the supply voltage, pin M/SS has to be set in Standby condition (GND level) before the voltage is applied (switch-on) or removed (switch-off). Via the Mute mode the input- and SVRR-capacitors are smoothly charged (or discharged). The slope of the SVRR-voltage should be well controlled and

slow. Unfortunately, the slope of the SVRR voltage is not well controlled in the phase where the SVRR voltage is between ground and ground + 0.7 V. In other words SVRR makes a step and so does the output. Consequently a plop sound can occur.

Solution is to give the SVRR pin a bias, see anti plop 1 in Figure 4. A second improvement is to give the DC-outputs of the load a bias, see anti plop 2 Figure 4.

The turn-on and turn-off time can be influenced by an RC-circuit on the pin M/SS; see anti plop 3 in Figure 4. Rapid on/off switching of the device or pin M/SS may cause click and plop noise. A proper timing on pin M/SS can prevent this; see Figure 4.

12.9 Thermal behavior

The typical thermal resistance of the TFA9800J in the DBS9P package ($R_{th(j-c)}$) is 4 K/W. The thermal resistance ($R_{th(h-a)}$) of an aluminium heat-sink with a (one-side) area of about 22 cm^2 is about 16 K/W. For a maximum ambient temperature of 60 °C the following calculation can be made for the application at V_P = 15 V, R_L = 4 Ω and the ALL music power dissipation is about 4 W:

$$T_{j(max)} = T_{amb} + P_{tot} \times (R_{th(j-c)} + R_{th(h-a)}) \Rightarrow T_{j(max)} = 60 + 4.0 \times (4 + 16) = 140\ °C$$

Remark: The calculation holds for applications at average listening level music output signals. Applying or testing with sine wave signals will produce about 1.5 × the music power dissipation. At worst-case condition this can activate the maximum temperature protection.

12.10 Application diagram and board layout

The single-ended application circuit diagram is shown in Figure 3. The PCB layout for this application is shown in Figure 5 and Figure 6.

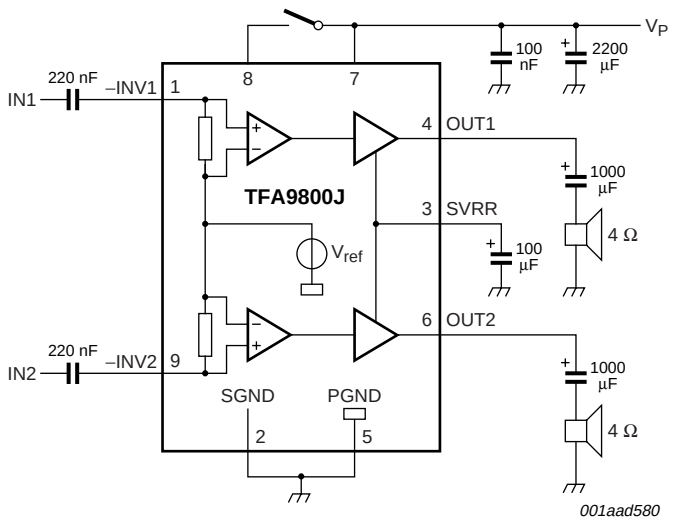


Fig 3. Single-ended application block diagram

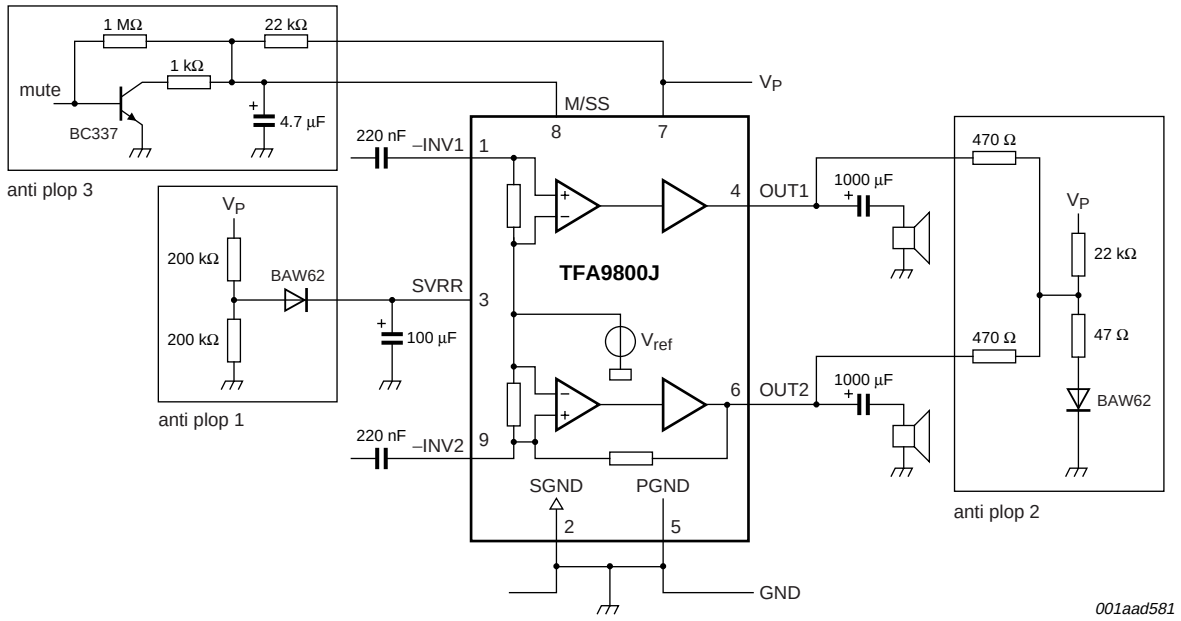
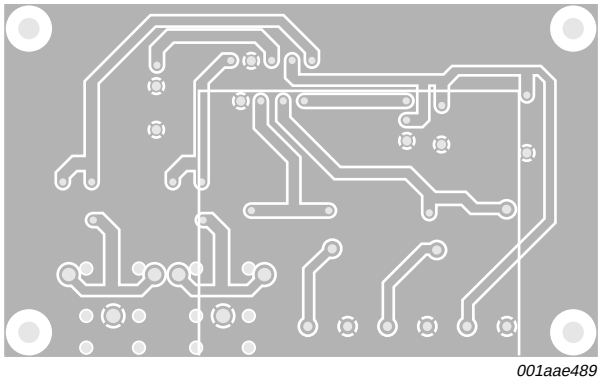


Fig 4. Implementation diagram for plop improvement



a. Bottom side

b. Component side

Fig 5. Printed-circuit board copper plane layout for single-ended application

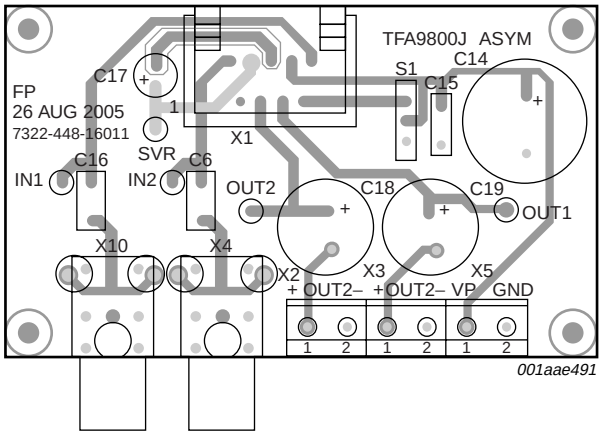


Fig 6. Printed-circuit board component layout for single-ended application

12.11 Typical performance characteristics for single-ended application

The test conditions, unless otherwise specified, are: T_{amb} = 25 °C; V_P = 15 V; f_i = 1 kHz; R_L = 4 Ω; single-ended stereo application; fixed gain equals 20 dB; audio band pass from 22 Hz to 22 kHz. All graphs show typical curves.

The graphs as a function of frequency use a band pass of 20 Hz to 80 kHz.

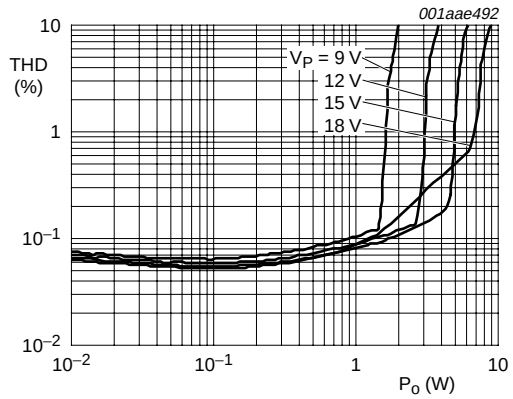


Fig 7. Total harmonic distortion as a function of output power

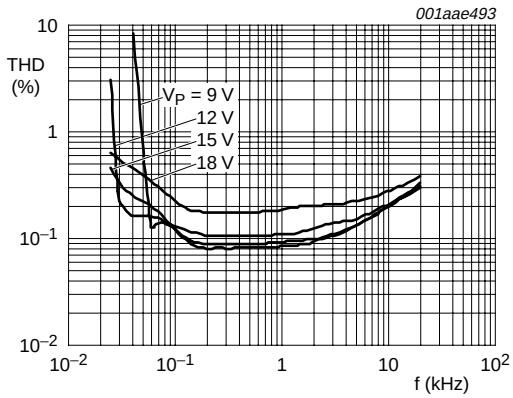
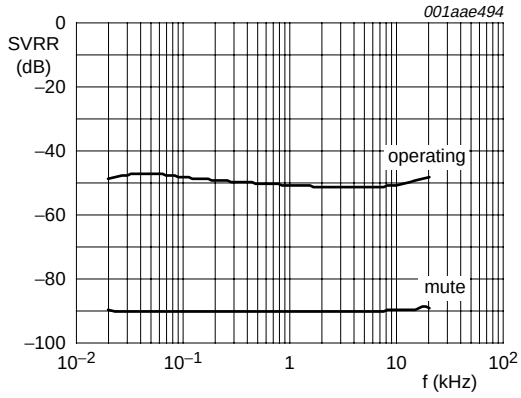


Fig 8. Total harmonic distortion as a function of frequency



R_S = 25 Ω

Fig 9. Supply voltage ripple rejection as a function of frequency

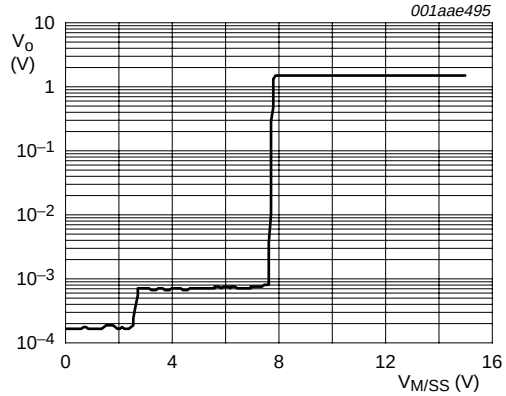


Fig 10. Output voltage as a function of voltage on pin M/SS

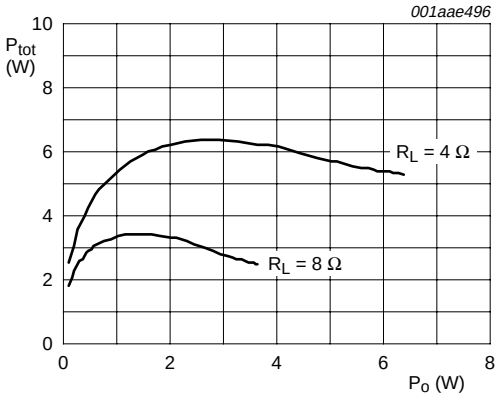


Fig 11. Total power dissipation (worst case, both channels driven) as a function of output power per channel

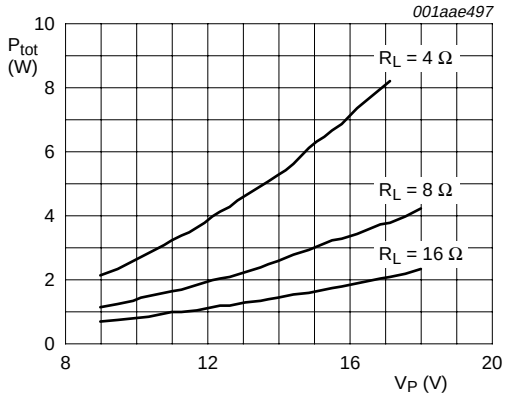


Fig 12. Total power dissipation (worst case, both channels driven) as a function of supply voltage

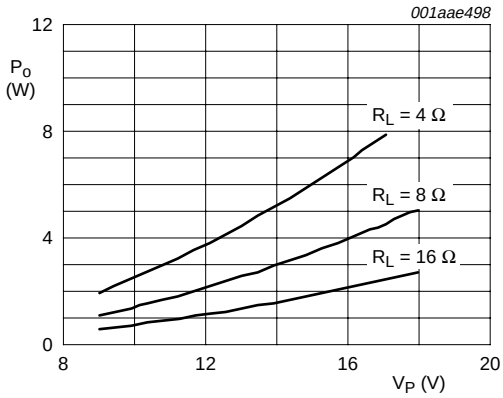
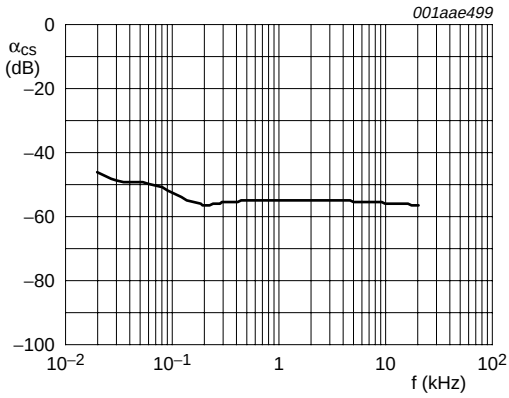


Fig 13. Output power (one channel) as a function of supply voltage

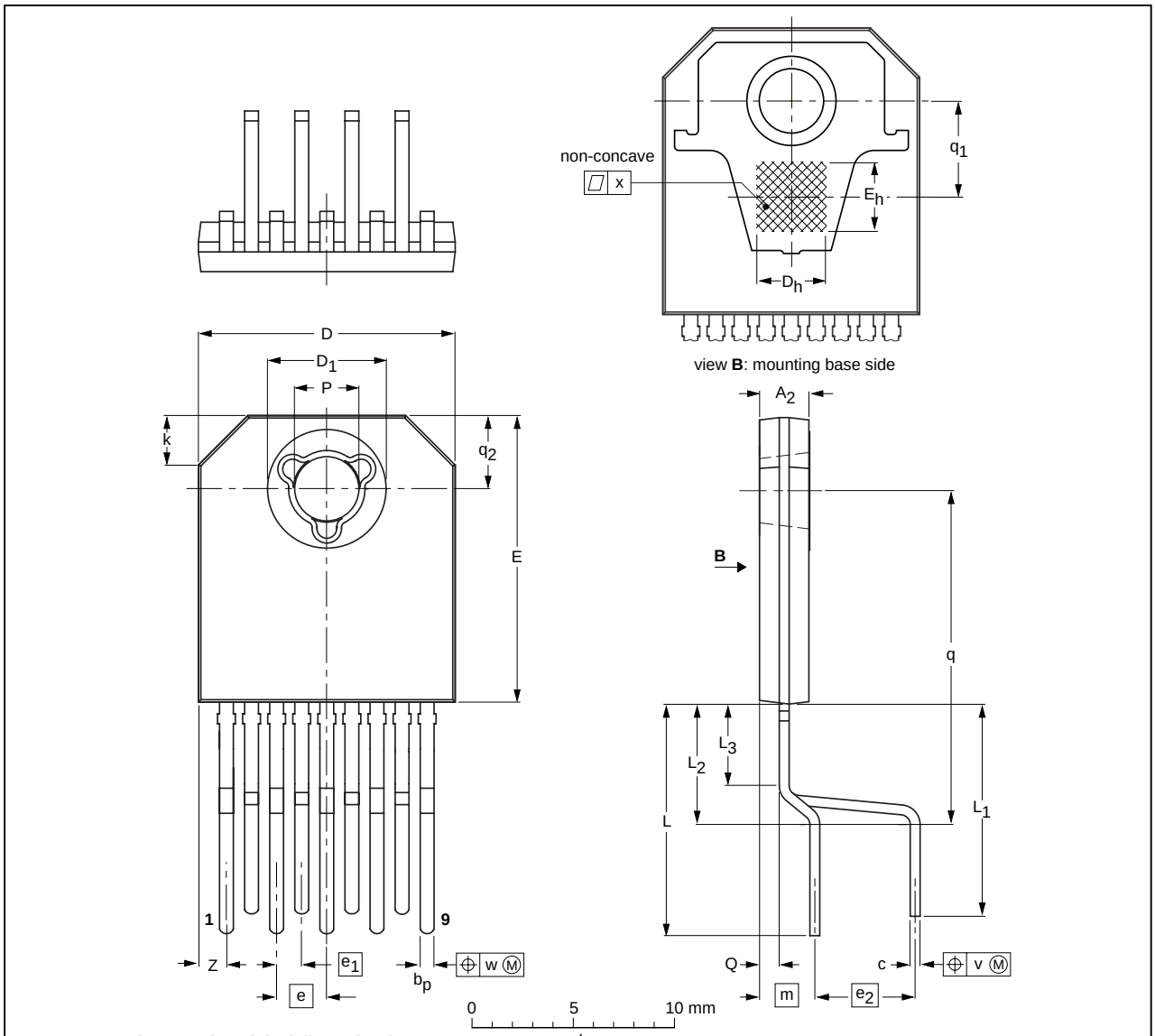


R_S = 25 Ω

Fig 14. Channel separation as a function of frequency

13. Package outline

DBS9P: plastic DIL-bent-SIL power package; 9 leads (lead length 12/11 mm); exposed die pad **SOT523-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A_2 (2)	b_p	c	D (1)	D_1 (2)	D_h	E (1)	E_h	e	e_1	e_2	k	L	L_1	L_2	L_3	m	P	Q	q	q_1	q_2	v	w	x	Z (1)
mm	2.7 2.3	0.80 0.65	0.58 0.48	13.2 12.8	6.2 5.8	3.5	14.7 14.3	3.5	2.54	1.27	5.08	3 2	12.4 11.0	11.4 10.0	6.7 5.5	4.5 3.7	2.8	3.4 3.1	1.15 0.85	17.5 16.3	4.85	3.8 3.6	0.8	0.3	0.02	1.65 1.10

Notes

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.
2. Plastic surface within circle area D_1 may protrude 0.04 mm maximum.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT523-1						~~00-07-03~~ 03-03-12

Fig 15. Package outline SOT523-1 (DBS9P)

14. Soldering

14.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

14.2 Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

14.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 °C and 400 °C, contact may be up to 5 seconds.

14.4 Package related soldering information

Table 9: Suitability of through-hole mount IC packages for dipping and wave soldering methods

Package	Soldering method	
	Dipping	Wave
CPGA, HCPGA	-	suitable
DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable	suitable [1]
PMFP [2]	-	not suitable

[1] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[2] For PMFP packages hot bar soldering or manual soldering is suitable.

15. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
TFA9800J_1	20060317	Preliminary data sheet	-	-	-

16. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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21. Contents

Date of release: 17 March 2006
Document number: TFA9800J_1

Published in The Netherlands