

Evaluation Board for the ADG854, 0.5 Ω CMOS, 1.8 V to 5.5 V, Dual SPDT/2:1 Mux in Mini LFCSP

FEATURES

Full-featured evaluation board for the ADG854

On-board audio connectors

GENERAL DESCRIPTION

This user guide describes the evaluation board for the ADG854, which is a low voltage CMOS device that contains two independently selectable, single-pole, double-throw (SPDT) switches. The ADG854 offers ultralow on resistance of less than 1 Ω over the full temperature range.

Figure 1 shows the EVAL-ADG854. The ADG854 is soldered onto the evaluation board in a tiny 1.3 mm \times 1.6 mm ultrathin LFCSP located in the center of the board and is designated as U1.

CONNECTING SIGNALS TO THE BOARD

The evaluation board is fitted with three audio connectors that allow switching between audio devices. All signals applied to the switch can be monitored using the test points provided on the evaluation board.

EVALUATION BOARD



Figure 1.

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REVISION HISTORY

5/12—Revision 0: Initial Version

HARDWARE DESCRIPTION

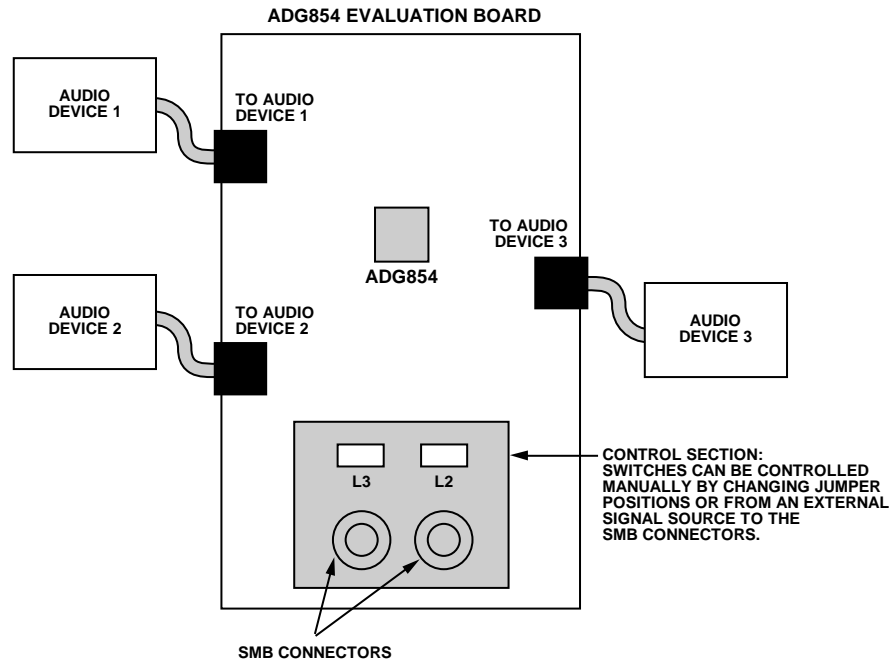


Figure 2. Evaluation Board Block Diagram

The [ADG854](#) evaluation kit contains a fully fitted PCB. The [ADG854](#) data sheet and this user guide are available on the [ADG854](#) product page.

The evaluation board allows the user to switch between two audio sources or to switch an audio source between two speakers by using the on-board jumpers or by applying the correct control signals to the appropriate connectors. The following sections describe in detail the function of the connectors and links.

POWER SUPPLY

The [ADG854](#) can operate from a 1.8 V to 5.5 V single supply and is fully specified for 5.5 V and 3.3 V supply operation.

Table 1. Control via Link L2/Link L3

L2 and L3 Position	Switch Status	
	Audio Device 1 Status	Audio Device 2 Status
B	Active	Inactive
A	Inactive	Active

Table 2. Control via SMB Connector Settings

L2 and L3 Position	Switch Status—Audio Device Status
B	SMB High = Audio Device 2 active SMB Low = Audio Device 1 active

SWITCH CONTROL CONNECTORS

The [ADG854](#) device offers a standard CMOS/LVTTL parallel interface consisting of two IN inputs. The IN1 and IN2 input pins control the switch state and operation mode of the [ADG854](#). The evaluation board allows the user to control the signals required to set the logic levels applied to these pins by using the L2 and L3 links as described in Table 1 or by applying external signals to the SMB connectors, IN1 and IN2, as described in Table 2.

To control the [ADG854](#) using the SMB connectors, L2 and L3 must be set to Position B. Note that there are 51 Ω termination resistors to GND at the IN1 and IN2 SMB connectors.

EVALUATION BOARD SCHEMATICS AND ARTWORK

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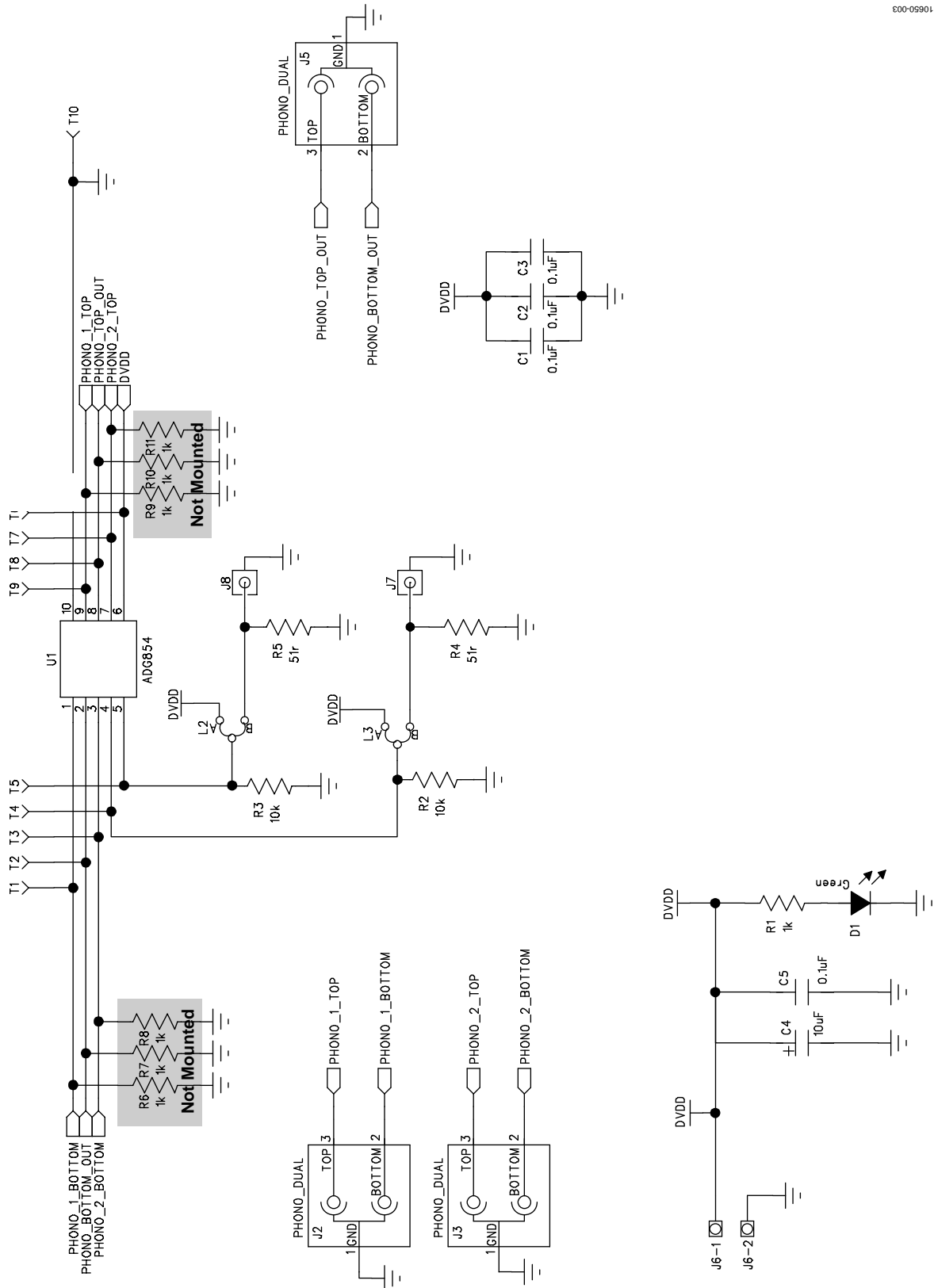


Figure 3. Evaluation Board Schematic

ADG854 SWITCH PINS, TEST POINTS, AND CONNECTIONS

Table 3.

Connector Name	Evaluation Board Pin Mnemonic	Pin Number	ADG854 Mnemonic	Test Point
J2	Phono top	1	S2A	T9
	Phono bottom	2	S1A	T1
J3	Phono top	1	S2B	T7
	Phono bottom	2	S1B	T3
J6-1	External 5 V	1	VDD	T6
J6-2	GND	2	GND	T10
J5	Phono top	3	D2	T8
	Phono bottom	2	D1	T2

PCB DRAWINGS

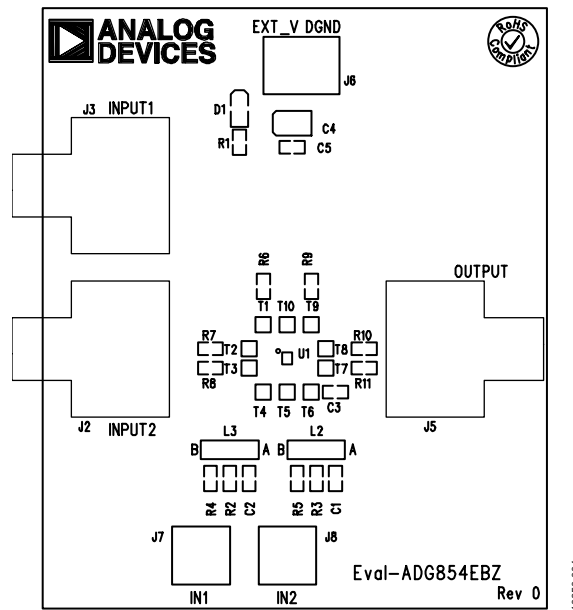
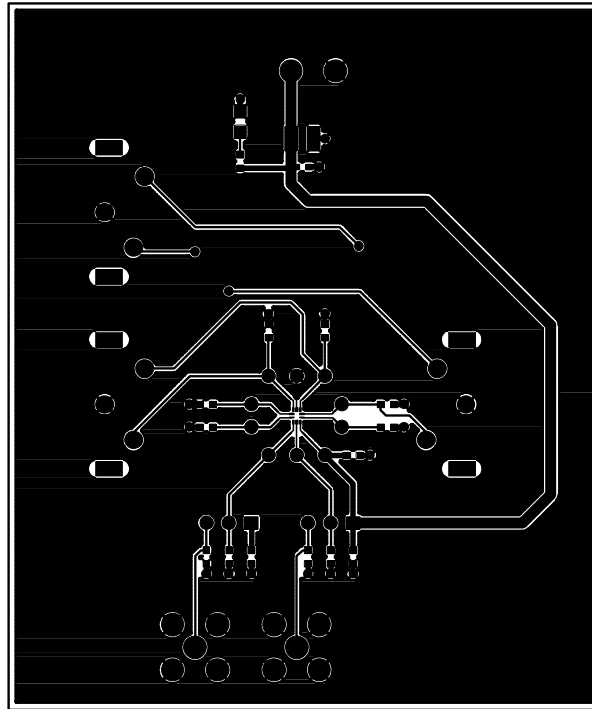
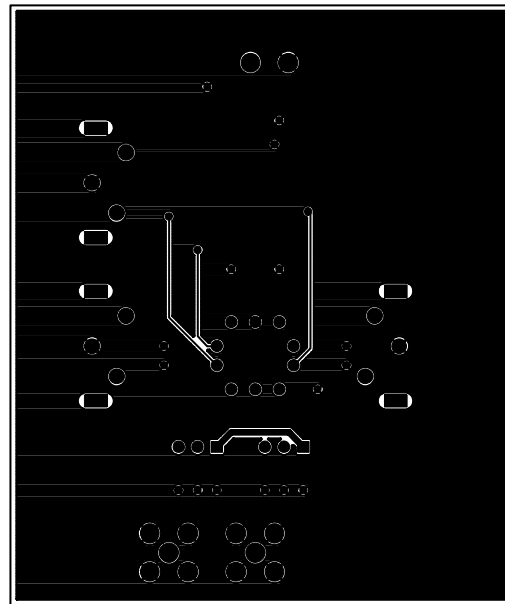


Figure 4. Silkscreen Image of the Evaluation Board



10650-005

Figure 5. PCB Drawing Layer 1 (Top Layer of the Evaluation Board)



10650-006

Figure 6. PCB Drawing Layer 2 (Bottom Layer)

COMPONENTS LIST

Table 4.

Reference Designator	Description	Value	Supplier Name and Number
C1 to C3,	Capacitor	0.1 μ F	FEC 9406140
C4, C5	Capacitor+	10 μ F	FEC 1190117
D1	LED		FEC 359-9681
J2, J3	Phono		Digi-Key CP-1435-ND
J6	CON\POWER		FEC 151785
J7, J8	SMB		FEC 1019324
J5	Phono		Digi-Key CP-1435-ND
L2 to L3	JUMPER2\SIP3		FEC 3291698 and FEC 150411
R1	Resistor	1 k Ω	FEC 1160322
R2, R3	Resistor	10 k Ω	FEC 1160359
R4, R5	Resistor	51 Ω	FEC 9331336
T1 to T10	Test point		FEC 8731128
U1	ADG854		Analog Devices, Inc., ADG854

NOTES

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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