FemtoClock® NG Jitter Attenuator and Clock Synthesizer

8V19N408

DATA SHEET

General Description

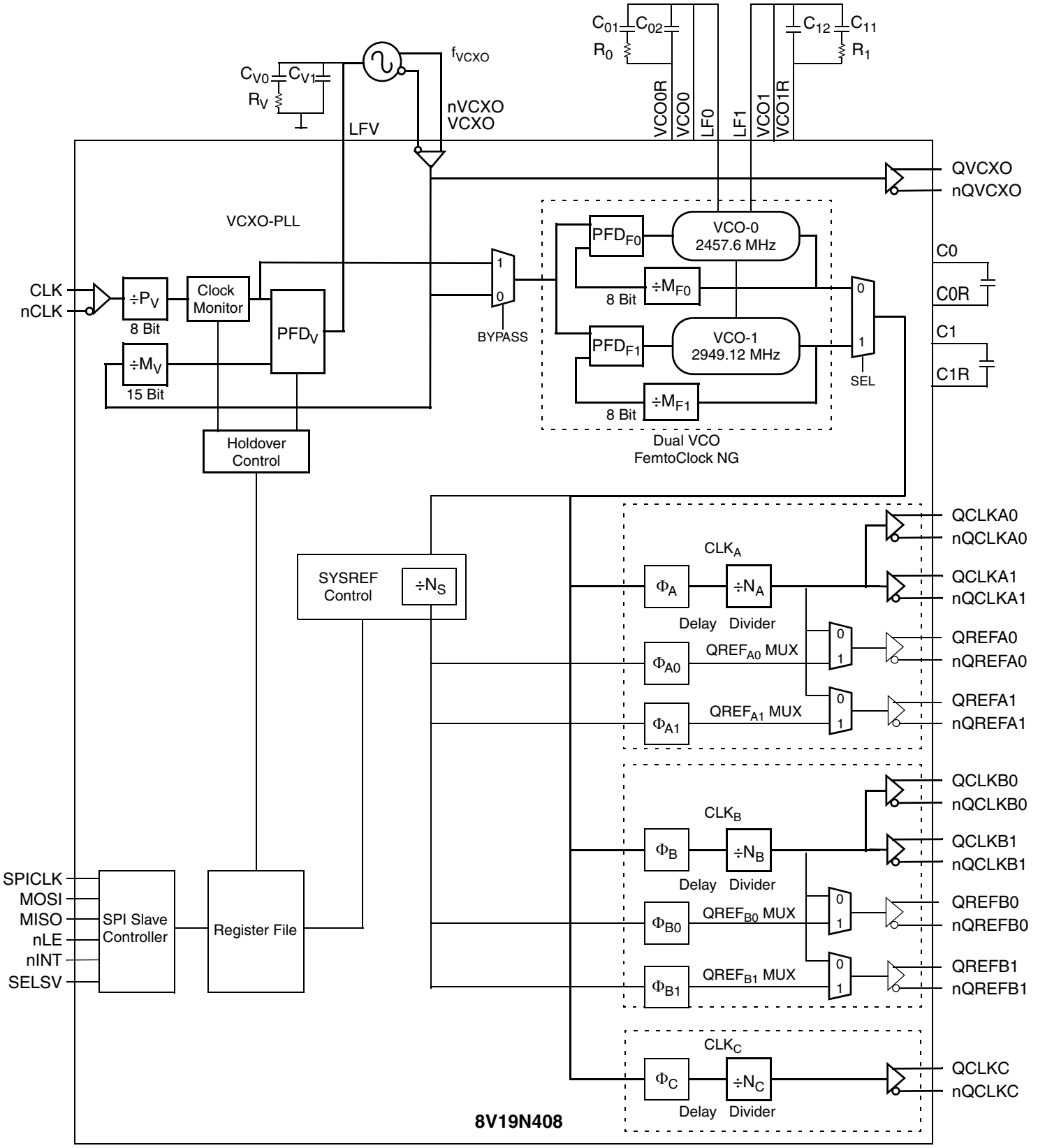
8V19N408 is a fully integrated FemtoClock® NG Jitter Attenuator and Clock Synthesizer. The device is a high-performance clock solution for conditioning and frequency/phase management of wireless base station radio equipment boards and is optimized to deliver excellent phase noise performance. The device supports JESD204B subclass 0 and 1 clock implementations. The device is very flexible in programming of the output frequency and phase. A two-stage PLL architecture supports both jitter attenuation and frequency multiplication. The first stage PLL is the jitter attenuator and uses an external VCXO for best possible phase noise characteristics.The second stage PLL lock on the VCXO-PLL output signal and synthesizes the target frequency. For flexibility, the second-stage PLL can use one of two VCOs at 2400MHz - 2500MHz (VCO-0) and 2920MHz - 3000MHz (VCO-1).

The device supports the clock generation of high-frequency clocks from the selected VCO and low-frequency system reference signals (SYSREF). The system reference signals are internally synchronized to the clock signals. Delay functions exist for achieving alignment and controlled phase delay between system reference and clock signals and to align/delay individual output signals. The input is monitored for activity. Short-term hold-over is provided to handle clock input failure scenarios. Auto-lock, individually programmable output frequency dividers and phase adjustment capabilities are added for flexibility. The device is configured through a 4-wire SP serial interface and reports lock and signal loss status in internal registers and optionally via lock detect (nINT) output. The device is packaged in a lead-free (RoHS 6) 72-lead VFQFN package. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements. The device is a member of the high-performance clock family from IDT.

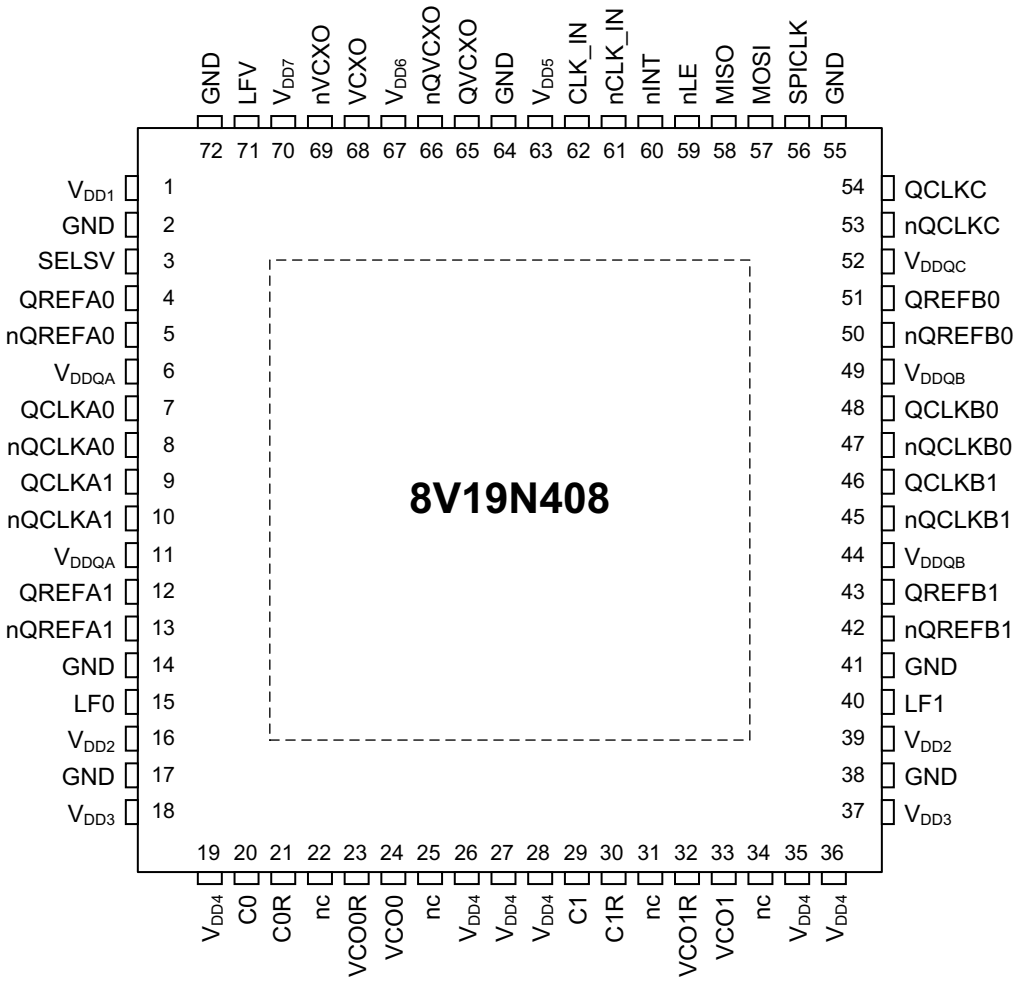
Features

- Core timing unit for JESD204B wireless infrastructure clocks
- Fourth generation FemtoClock® NG technology
- First stage PLL uses an external VCXO for jitter attenuation
- Second PLL stage facilitates a dual integrated VCO for flexible frequency synthesis
- Integrated VCO frequencies: 2400MHz - 2500MHz (VCO-0) and 2920MHz - 3000MHz (VCO-1)
- Five differential configurable LVPECL, LVDS clock outputs with a variable output amplitude
- Four differential LVDS system reference (SYSREF) signal outputs
- Synchronization between clock and system reference signals
- Wide input frequency range supported by 8-bit pre- and 15-bit VCOX-PLL feedback divider
- Output clock frequencies: 2457.6MHz ÷N (VCO-0) and 2949.12MHz ÷N (VCO-1) in wireless infrastructure applications
- Three independent output clock frequency dividers N (range of ÷1 to ÷96)
- Clock output frequency range (VC0-0): (2400MHz - 2500MHz) ÷N
- Clock output frequency range (VC0-1): (2920MHz - 3000MHz) ÷N
- Phase delay capabilities for alignment/delay for clock and SYSREF signals
- Individual output phase adjustment (Clock): one-period of the selected VCO frequency in 64 steps
- Individual output phase adjustment (SYSREF): approximately half-period of the selected VCO frequency in 8 steps
- Internal, SPI controlled SYSREF pulse generation
- SYSREF frequencies: $f_{VCO} \div N_S$ (10 dividers)
- N_S divider range: ÷64 to ÷2048
- SYSREF (wireless infrastructure): 1.2MHz – 46.08MHz
- Clock input compatible with LVPECL, LVDS, LVCMOS signals
- Dedicated power-down features for reducing power consumption
- Input clock monitoring
- Holdover for temporary loss of input signal scenarios
- Support of output power-down and output disable
- Typical clock output phase noise at 1228.8MHz:
  1kHz offset: -116.9dBc/Hz
  10kHz offset: -118.1dBc/Hz
  100kHz offset: -122.7dBc/Hz
  1MHz offset: -144.7dBc/Hz
  10MHz offset: -153.5dBc/Hz
- RMS phase noise (12kHz – 20MHz): <100fs (target)
- Status conditions with programmable functionality for loss-of-lock and loss-of-reference indication
- Lock detect (nINT) output for status change indication
- LVCMOS/LVTTL compatible SPI serial interface
- 3.3V core and output supply mode
- Control pins support 3.3V I/O logic levels:
  SPI interface levels support selectable 3.3V/1.8V logic levels
- -40°C to +85°C ambient operating temperature
- Lead-free (RoHS 6) 72-lead VFQFN packaging

Block Diagram



Pin Assignment



72-pin, 10mm x 10mm VFQFN Package

Pin Description Table

Table 1. Pin Descriptions [1]

Number	Name	Type		Description
1	V_{DD1}	Power		Positive supply (3.3V) for the VCXO-PLL front end (charge pump and P_V divider).
2	GND	Ground		Power supply ground. Ground current return path for pin V_{DD1}. Connect to board GND (0V).
3	SELSV	Input	Pullup	SPI voltage select. 3.3V LVCMOS/LVTTL interface levels
4	QREFA0	Output		Differential SYSREF/clock output A0. LVDS style for SYSREF operation, Configurable LVPECL, LVDS style and amplitude for clock operation.
5	nQREFA0	Output		
6	V_{DDQA}	Power		Output supply (3.3V) for the QCLKAn and QREFAn outputs.
7	QCLKA0	Output		Differential clock output A0. Configurable LVPECL, LVDS style and amplitude.
8	nQCLKA0	Output		

Table 1. Pin Descriptions (Continued)[1]

Number	Name	Type		Description
9	QCLKA1	Output		Differential clock output A1. Configurable LVPECL, LVDS style and amplitude.
10	nQCLKA1	Output		
11	V_{DDQA}	Power		Output supply (3.3V) for the QCLKAn and QREFAn outputs.
12	QREFA1	Output		Differential SYSREF/clock output A1. LVDS style for SYSREF operation, Configurable LVPECL, LVDS style and amplitude for clock operation.
13	nQREFA1	Output		
14	GND	Power		Power supply ground. Ground return path for the V_{DD2} pins. Connect to board GND (0V).
15	LF0	Output		Loop filter/charge pump output for the FemtoClock NG PLL, VCO-0. Connect LF0 and VCO0 (pin 24) to the external loop filter components.
16	V_{DD2}	Power		Positive supply (3.3V) for the LF0 and LF1 outputs.
17	GND	Power		Power supply ground. Ground return path for the V_{DD3} pins. Connect to board GND (0V).
18	V_{DD3}	Power		Positive supply (3.3V) for the internal PLLs.
19	V_{DD4}	Power		Positive supply (3.3V) for the internal oscillators VCO-1 and VCO-2.
20	C0	Analog		Regulator 0 bypass capacitor. Use a 4.7µF capacitor between the C0 and C0R pins.
21	C0R	Analog		
22	nc	Unused		No internal connection. Do not use.
23	VCO0R	Analog		Ground return path pin for the VCO-0 loop filter.
24	VCO0	Analog		Loop filter control voltage input to VCO0.
25	nc	Unused		No internal connection. Do not use.
26	V_{DD4}	Power		Positive supply (3.3V) for the internal VCO-1 and VCO-2.
27	V_{DD4}	Power		Positive supply (3.3V) for the internal VCO-1 and VCO-2.
28	V_{DD4}	Power		Positive supply (3.3V) for the internal VCO-1 and VCO-2.
29	C1	Analog		Regulator 1 bypass capacitor. Use a 4.7µF capacitor between the C1 and C1R pins.
30	C1R	Analog		
31	nc	Unused		No internal connection. Do not use.
32	VCO1R	Analog		Ground return path pin for the VCO-1 loop filter.
33	VCO1	Analog		Loop filter control voltage input to VCO-1
34	nc	Unused		No internal connection. Do not use.
35	V_{DD4}	Power		Positive supply (3.3V) for the internal oscillators VCO-1 and VCO-2.
36	V_{DD4}	Power		Positive supply (3.3V) for the internal oscillators VCO-1 and VCO-2.
37	V_{DD3}	Power		Positive supply (3.3V) for the internal PLLs.
38	GND	Power		Power supply ground. Ground return path for the V_{DD3} pins. Connect to board GND (0V).
39	V_{DD2}	Power		Positive supply (3.3V) for the LF0 and LF1 outputs.
40	LF1	Output		Loop filter/charge pump output for the FemtoClock NG PLL, VCO-1. Connect LF1 and VCO-1 (pin 33) to the external loop filter components.
41	GND	Power		Power supply ground. Ground return path for the V_{DD2} pins. Connect to board GND (0V).
42	nQREFB1	Output		Differential SYSREF/clock output B1. LVDS style for SYSREF operation, Configurable LVPECL, LVDS style and amplitude for clock operation.
43	QREFB1	Output		
44	V_{DDQB}	Power		Output supply (3.3V) for the QREFBn and QCLKBn outputs.

Table 1. Pin Descriptions (Continued)[1]

Number	Name	Type		Description
45	nQCLKB1	Output		Differential clock output B1. Configurable LVPECL, LVDS style and amplitude.
46	QCLKB1	Output		
47	nQCLKB0	Output		Differential clock output B0. Configurable LVPECL, LVDS style and amplitude.
48	QCLKB0	Output		
49	V_{DDQB}	Power		Output supply (3.3V) for the QREFBn and QCLKBn outputs.
50	nQREFB0	Output		Differential SYSREF/clock output B0. LVDS style for SYSREF operation, Configurable LVPECL, LVDS style and amplitude for clock operation.
51	QREFB0	Output		
52	V_{DDQC}	Power		Output supply (3.3V) for the QCLKC output.
53	nQCLKC	Output		Differential clock output C. Configurable LVPECL, LVDS style and amplitude.
54	QCLKC	Output		
55	GND	Power		Power supply ground. Ground return path for the V_{DD5} pins. Connect to board GND (0V).
56	SPICLK	Input	Pulldown	Serial Control Port SPI Clock input. 3.3V/1.8V selectable LVCMOS/LVTTL interface levels.
57	MOSI	Input	Pulldown	Serial Control Port SPI Data input. 3.3V/1.8V selectable LVCMOS/LVTTL interface levels.
58	MISO	Output		Serial Control Port SPI Data output. 3.3V/1.8V selectable LVCMOS/LVTTL interface levels.
59	nLE	Input	Pulldown	Serial Control Port SPI Load Enable input.3.3V/1.8V selectable LVCMOS/LVTTL interface levels.
60	nINT	Output		Status Output pin for signaling fault conditions. 3.3V/1.8V selectable LVCMOS/LVTTL interface levels.
61	nCLK_IN	Input	Pullup / Pulldown	Device clock inverting and non-inverting differential clock input. Inverting input is biased to 1.2V by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals.
62	CLK_IN	Input	Pulldown	
63	V_{DD5}	Power		Positive supply (3.3V) for the SPI interface and the CLK, nCLK input.
64	GND	Power		Power supply ground. Ground return path for the V_{DD6} pins. Connect to board GND (0V).
65	QVCXO	Output		Differential VCXO-PLL clock output. Configurable LVPECL, LVDS style and amplitude.
66	nQVCXO	Output		
67	V_{DD6}	Power		Positive supply (3.3V) for the QVCXO output and VCXO-PLL.
68	VCXO	Input	Pulldown	VCXO non-inverting and inverting differential clock input. Inverting input is biased to 1.2V by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals.
69	nVCXO	Input	Pullup / Pulldown	
70	V_{DD7}	Power		Positive supply (3.3V) for the VCXO-PLL charge pump output.
71	LFV	Output		VCXO-PLL charge pump output. Connect to the loop filter for the external VCXO.
72	GND	Power		Power supply ground. Ground return path for the V_{DD6} pins. Connect to board GND (0V).
—	Exposed pad	Power		Power supply ground. Ground return path for all differential outputs. Connect to board GND (0V) and to a thermally low resistive path on the board.

NOTE 1. *Pulldown and Pullup* refer to internal input resistors. See Table 4B, *Input/Output Characteristics,* for typical values.

Principles of Operation

The 8V19N408 is a dual stage PLL clock synthesizer. The first stage is the VCXO-PLL that uses an external VCXO device as a high-quality oscillator and provides jitter attenuation to the input clock signal. The second stage is a FemtoClock NG synthesizer PLL with a dual VCO for flexible output frequency generation. By configuring the 8-bit integer pre-scaler P_V and the 15-bit integer feedback divider M_V, the VCXO-PLL can accommodate a wide range of input and VCXO frequencies.The input (P_V) and VCXO-PLL feedback (M_V) dividers must be set to match the frequency of the phase detector (PFD_F). The VCO of the second stage PLL is designed to support center frequencies within the specified VCO range. Each VCO has its own PLL feedback divider (M_{F0} or M_{F1}) which must be set to match the VCXO-PLL frequency (first loop) to its center frequency range. Table 2A shows the supported input, feedback and output dividers.

The output signal of the second stage FemtoClock NG PLL is then distributed to the individual clock dividers, delay stages and outputs. The device has five clock outputs (QCLK), organized in the three output banks A, B and C. Each output bank has an individual integer clock divider N for clock frequency generation. See Table 2E for a list of supported output frequencies.

The jitter-attenuated clock signal from the VCXO-PLL is routed to the QVCXO output. The phase noise of this output corresponds to the quality of the used external VCXO.

The devices supports the generation of up to four non-periodic or periodic synchronization signals (SYSREF). The SYSREF signals are generated internally from the VCO clock source, therefore the SYSREF outputs (QREF) are synchronous to the QCLK outputs. The SYSREF signals have a pulse repetition rate of $f_{VCO} \div N_S$ (the N_S divider can be configured to one of 10 frequency dividers. See Table 2A).

Each QCLK output bank signal can be individually phase-delayed to achieve a specific phase alignment relative to each other and relative to any QREF (SYSREF) clock output. The four QREF outputs can be individually re-configured as device clocks for additional flexibility.

In an alternatively operation mode, the VCXO input stage can by bypassed for applications with multiple 8V19N408 devices locking to a common source clock. In such an application, the first device acts as a jitter attenuator and the second device acts as a low phase noise frequency synthesizer. The first device provides the input signal to the second 8V19N408 at e.g. 122.88MHz. The second 8V19N408 is used in VCXO-bypass mode and its second stage PLL locks to the jitter-attenuated clock input signal of the first device.

The device is configured through an SPI interface. Configurations are established by setting or resetting internal bits, which are organized in eight 32-bit words. The SPI interface also supports read-back of configuration settings.

Table 2A. PLL Divider Settings

PLL Divider	Range	Operation
Prescaler P_V	÷1 to ÷255 (8 bit)	Input Clock Frequency: $f_{CLK} = f_{VCXO} \cdot \frac{P_V}{M_V}$
VCXO-PLL Feedback Divider M_V	÷4 to ÷32767 (15 bit)	
FemtoClock NG Feedback Divider M_{F0}, M_{F1}	÷8 to ÷255 (8 bit)	VCXO Frequency: $f_{VCXO} = \frac{f_{VCO}}{M_{F0(1)}}$
Output Divider N (N_A to N_C)	÷1 to ÷96 (18 discrete dividers)	Output Frequency $f_{OUT} = \frac{f_{VCO}}{N_{A,B,C}}$
SYSREF Divider N_S	÷64 to ÷2048 (10 discrete dividers)	SYSREF Frequency/Rate $f_{SYSREF} = \frac{f_{VCO}}{N_S}$

Table 2B. Example FemtoClock NG PLL Divider Settings (f_{VCO} = 2457.6MHz)[1]

VCXO Frequency (MHz)	M_{F0} Divider Settings
153.6	÷16
122.88	÷20
76.8	÷32
61.44	÷40
38.4	÷64
30.72	÷80

NOTE 1. Example list of VCXO frequencies for VCO frequency of 2457.6MHz. The M_{F0} divider has a range from M_{F0} = 8 to M_{F0} = 255. $f_{VCXO} = 2457.6 \div M_{F0}$. See Table 3C for register configuration.

Table 2C. VCXO-PLL Bypass Settings[1]

BYPASS	Operation
0	VCXO-PLL operation.
1	VCXO-PLL bypassed. The reference clock for the 2nd PLL is the input clock. Clock monitoring is disabled. No jitter attenuation. No external VCXO component and loop filter required.

NOTE 1. See Table 3I for register configuration.

Input Reference

The 8V19N408 is designed for high-reliability applications and supports input frequency monitoring. If no activity has been detected on any clock input within a fixed time period, then the reference is considered to be invalid and an internal status flag is set. This is a loss of signal event (LOS) and sets the STAT0 status bit. See also Table 2Q for an overview of supported status functions. The VCXO-PLL provides a temporary hold-over in LOS situations.The device enters a hold-over state in any of the following cases:

- the clock signal is invalid (LOS)
- the HOLD bit is set to logic 1 (hold-over) (See Table 2D)

Table 2D. Holdover[1]

HOLD	Operation
0	Normal operation
1	VCXO-PLL is set to holdover. The control voltage of the external VCXO is set to $V_{DD}/2$.

NOTE 1. See Table 3I for register configuration.

VCXO-PLL

The charge pump current of the PLL is configurable in small steps by writing the desired charge pump current amount into a SPI register. 64 steps of 20µA are available, the range pump current range is 0µA to 1.26mA. See CPV[5:0], Table 3I for available settings.

Clock Outputs

Output Divider

From the VCO frequency the three independent clock output dividers N_A, N_B and N_C scale the frequency down to the desired clock output frequencies. (see Table 2E). The output dividers N_A, N_B and N_C can be set via internal registers. The configuration and re-configuration of any of the output dividers requires the SPI write sequence described in Section, “Clock Output Divider Reset Sequence, (Sequence S1)” on page 12.

Table 2E. $N_{A, B, C}$ Frequency Divider Settings[1]

Output Divider N_A, N_B, N_C	Output Clock Frequency
÷1	VCO Frequency ÷1
÷2	VCO Frequency ÷2
÷3	VCO Frequency ÷3
÷4	VCO Frequency ÷4
÷5	VCO Frequency ÷5
÷6	VCO Frequency ÷6
÷8	VCO Frequency ÷8
÷10	VCO Frequency ÷10
÷12	VCO Frequency ÷12
÷16	VCO Frequency ÷16
÷20	VCO Frequency ÷20
÷24	VCO Frequency ÷24
÷32	VCO Frequency ÷32
÷40	VCO Frequency ÷40
÷48	VCO Frequency ÷48
÷64	VCO Frequency ÷64
÷80	VCO Frequency ÷80
÷96	VCO Frequency ÷96

NOTE 1. Individual setting for each output bank A, B and C. See Table 3E for register configuration.

Table 2F. $N_{A, B, C}$ Example Frequency Divider Settings

Output Divider N_A, N_B, N_C	Output Clock Frequency in MHz for a VCO Frequency of:		
	2457.6MHz[1]	2500MHz[1]	2949.12MHz[2]
÷1	2457.600	2500.000	2949.120
÷2	1228.800	1250.000	1474.560
÷3			983.04
÷4	614.400	625.000	737.280
÷5	491.520	500.000	589.824
÷6			491.52
÷8	307.200	312.500	368.640
÷10	245.760	250.000	294.912
÷12			245.76
÷16	153.600	156.250	184.320
÷20	122.880	125.000	147.456
÷24			722.88
÷32	76.800	78.125	92.160
÷40	61.440	62.500	
÷48	51.2		61.44
÷64	38.4		
÷80	30.720	31.250	
÷96	25.600		30.720

NOTE 1. VCO-0
NOTE 2. VCO-1

Output Format

All differential device clock outputs (QCLK) can be individually configured in format (LVPECL, LVDS), output amplitude, state (enable, disable) and power state (power on, power off). Outputs in LVPECL format are terminated to a termination voltage V_T according to the configured output amplitude. Outputs in LVDS format are terminated 100Ω across the terminals. The output format of the 8V19N408 was designed for flexibility in amplitude control. The output offset voltage changes with amplitude. For strict LVDS compliance, it is recommended to AC-couple the LVDS outputs and re-bias to V_{BIAS} = 1.25V. The lowest output amplitude settings correspond with the least amount of power consumed. Unused clock outputs may not be terminated externally to save current consumption. The QCLK outputs LVPECL, LVDS format configuration is shown in Table 2G. For LVPECL format, set EF = 1 and terminate the LVPECL output pair 50Ω to the specified recommended termination voltage shown in Table 2G. For LVDS format, set EF = 0 and terminate the output pair 100Ω across the QCLK, nQCLK terminals. Independent on the state of the EF bit, the A[1:0] bits control the output amplitude of QCLK outputs.

Table 2G. QCLK Output Control[1]

EF	A1	A0	Output Operation	Output Termination
LVPECL (EF = 1)				
1	0	0	Power off	Do not terminate
1	0	1	400mV	50Ω to V_{DDx} - 1.5V
1	1	0	700mV	50Ω to V_{DDx} - 2V
1	1	1	1000mV, f_{OUT}>500MHz	50Ω to V_{DDx} - 2.5V
LVDS (EF = 0)				
0	0	0	Power off	100Ω across
0	0	1	400mV	100Ω across
0	1	0	700mV	100Ω across
0	1	1	1000mV, f_{OUT}>500MHz	100Ω across

NOTE 1. Individual setting for each output QCLKA[1:0], QCLKB[1:0] and QCLKC.

Each QCLK output can be individually disabled to the logic low state by clearing the corresponding OUTEN bit. See Table 2H for details.

Table 2H. QCLK Output Enable[1]

OUTEN	Output Operation
0	QCLK is disabled in logic low state
1	QCLK is enabled

NOTE 1. Individual setting for each output QCLKA[1:0], QCLKB[1:0] and QCLKC.

Clock channel power: Setting the corresponding nPOWER bit will power-down the N divider and delay stage of an clock output channel to save operating currents in situations of an output channel not used for frequency generation.

Table 2I. Clock Channel Power Operation[1]

nPOWER	Clock Channel
0	Divider N and delay stage Φ powered up
1	Divider N and delay stage Φ powered down

NOTE 1. Individual setting for each clock channel A, B and C (dividers N_A, N_B, N_C and clock delay stages Φ_A, Φ_B, Φ_C). See Table 3E for register configuration.

SYSREF Outputs (QREF)

Each QREF output can be individually configured as SYSREF output or as clock output by setting the corresponding MUX bit. For JESD204B-operation, configure QREF outputs as SYSREF outputs. See Table 2J for details

Table 2J. QREF Output Configuration[1]

QREF MUX	Operation
0	**Clock Mode** • Frequency divided by N • Output amplitude: use any setting in Table 2K • Set nPOWER = 1 to power down the corresponding (unused) SYSREF delay stage $\Phi_{A0\text{-}B1}$ • Set OUTEN = 1 (output enable)
1	**SYSREF Mode (JESD204B)** • Set nPOWER = 0 to power up the corresponding SYSREF delay stage $\Phi_{A0\text{-}B1}$ • Set the QREF output amplitude to 400mV (A[1:0] = 01) • Set OUTEN = 1 (output enable)

NOTE 1. Individual setting for each output QREF output QREFA[1:0], QREFB[1:0].

Clock mode (MUX = 0): QREF outputs operate as additional clock outputs, increasing the available clock signal fanout. In this mode, the output amplitude can be configured to one of three different values. In clock mode, the output frequency of is controlled by the N divider of the corresponding device clock output. For instance, the divider N_A controls the output frequency of both QCLKA0, A1 and QREFA0, A1. The QREF output delay setting is controlled by the delay circuit Φ of the associated clock output QCLK. See Table 2K for details.

Table 2K. QREF Output Control (MUX = 0)

OUTEN	A[1]	A[0]	Output Operation
X	0	0	QREF output buffer powered-down
0	0	1	QREF disabled in logic low state
0	1	0	
0	1	1	
1	0	1	$V_{O,\ PP}$ = 400mV
1	1	0	$V_{O,\ PP}$ = 700mV
1	1	1	$V_{O,\ PP}$ = 1000mV, f_{OUT}>500MHz

JESD204B (SYSREF) Operation (MUX = 1): The QREF outputs support the generation of SYSREF pulses in JESD204B applications. The delay stages can be used to establish repeatable phase relationships of QCLK outputs to each other and to the SYREF signals QREF: the QCLK delay stages support 64 steps of delay and the QREF outputs support additional 8 steps of fine-delay.

See Table 2P and Section, “SYSREF Generation” on page 11. Each individual QREF output can also be disabled into logic low state by clearing the OUTEN bit. For SYSREF operation, the QREF outputs should be configured as shown in Table 2L:

Table 2L. QREF Output Control[1] (SYSREF, MUX = 1)

A1	A0	Output Operation	Output Termination
0	0	Power off	100Ω across
0	1	$V_{O,\ PP}$ = 400mV	100Ω across

NOTE 1. Individual setting for each output QREF output QREFA[1:0], QREFB[1:0].

SYSREF power down features: Setting the corresponding nPOWER bit will power-down the Φ delay circuit. A QREF output buffer can be powered-down by setting A[1:0] = 00. The QREF outputs automatically power-down when SRO = 0 (counted pulse mode) and no SYSREF pulses are generated. QREF outputs will power up automatically for SYSREF pulse generation, controlled by the SYSREF generation sequence (see Section, “QREF Phase Delay and SYSREF Synchronization Sequence, (Sequence S2)” on page 12). Applications not using a QREF output should power the delay circuit down (nPOWER = 1) and also power off the output buffer (set MUX = 0, A[1:0] = 00). Powered-down output buffers save operating current, even with presence of external termination. See Table 2M and Table 2K for details.

Synchronization and Phase Alignment

QCLK Outputs

The 8V19N408 has output dividers which generate the supported clock frequencies at outputs QCLK synchronously. After the SPI controlled synchronization of output dividers, all output clocks QCLK will be in alignment with each other. Outputs which select different output dividers are aligned on the incident rising edge.

QCLK Delay Circuits

The clock outputs QCLK have an individual delay element (Φ) to advance/delay its clock output phase of an clock output bank if an offset is desired on a particular output. The delay circuit operates by inserting a delay into the clock signal coming out of the individual QCLK bank outputs by a discrete number of one clock period of the FemtoClock NG VCO. The user may select a number of steps to insert via the appropriate register. Each of the two output banks supports 64 steps of phase delay (the delay unit is a function of the internal VCO frequency. See Table 2O). For fine delay, the SYSREF outputs have individual phase delay circuits, each delay circuit supports eight steps. See Table 2P.

The delay capabilities of the clock and SYSREF outputs can be used to establish a specific, repeatable phase relationship between any QCLK and QREF outputs. QREF outputs that are configured with the same delay value are aligned to each other.

Table 2M. Φ_A,Φ_B, Φ_C QCLK Phase Delay[1]

Delay Unit	Phase Delay (Φ) in ns	Phase Delay (Φ) in ns for a VCO Frequency of:		
	$\frac{1}{f_{VCO}}$	2457.6MHz[2]	2500MHz[2]	2949.12MHz[3]
0	0	0	0	0
1	$1 \cdot 1/f_{VCO}$	0.406	0.400	0.339
2	$2 \cdot 1/f_{VCO}$	0.8138	0.800	0.678
...	...	...	...	...
Φ	$\Phi \cdot 1/f_{VCO}$	Φ · 0.406	Φ · 0.400	Φ · 0.339
...	...	...	...	...
63	$63 \cdot 1/f_{VCO}$	25.634	25.200	21.362

NOTE 1. Individual setting for each clock output Bank A, B and C.
NOTE 2. VCO-0
NOTE 3. VCO-1

Table 2N. Φ_{A0}, Φ_{A1}, Φ_{B0}, Φ_{B1} QREF Phase Delay[1, 2]

Delay Unit		Delay	Phase Delay (Φ) in ns for a VCO Frequency (f_{VCO}) of:		
			2457.6MHz	2500MHz	2949.12MHz
0	000	0	0.000	0.000	0.000
1	001	t_{Delay}	0.165	0.165	0.165
2	010	$1/f_{VCO}$	0.407	0.400	0.339
3	011	$t_{Delay} + 1/f_{VCO}$	0.572	0.565	0.504
4	100	$2/f_{VCO}$	0.814	0.800	0.678
5	101	$t_{Delay} + 2/f_{VCO}$	0.979	0.965	0.843
6	110	$3/f_{VCO}$	1.221	1.200	1.017
7	111	$t_{Delay} + 3/f_{VCO}$	1.386	1.365	1.182

NOTE 1. t_{Delay} is implemented by inserting a buffer delay of 165ps (±20% tolerance).
NOTE 2. Individual setting for each SYSREF delay stages. See Table 3G for register configurations.

QREF to QCLK Phase Alignment

The QREF outputs have a deterministic phase relation to the QCLK outputs. The delay circuits in both QCLK and QREF paths add phase offset to configure the phase relationship of each QCLK and QREF pair. There are 64 delay steps for each QCLK output bank and additional 8 delay steps on each QREF output. The QCLK delay unit is equal to one VCO period, the QREF delay unit is equal to approximately one half VCO period (fine delay). Each QCLK output bank and each QREF output can be individually advanced, aligned or delayed with respect to an incident QCLK rising edge. See Figure 1: For phase alignment between the incident edge of QCLK outputs and QREF, set the phase delay to Φ = 9 (QCLK) and Φ = 0 (QREF). As a pre-condition for alignment of SYSREF pulses to the incident clock edge, set the SYSREF synchronizer divider to the least common multiple value of clock dividers N_A and N_B (see Table 3K).

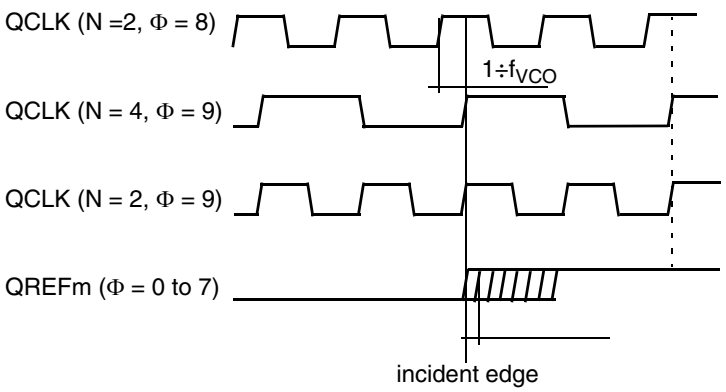


Figure 1. QREF to QCLK Phase Relationship

SYSREF Generation

The QREF outputs generate SYSREF signal pulses that support JESD204B synchronization functions. Following SYSREF pulse generation modes are available and configurable by SPI:

- Counted pulse mode: 1 to 255 pulses are generated by the device. SYSREF activity stops automatically after the transmission of the selected number of pulses and the QREF output powers down.
- Continuous mode. The SYSREF signal is a clock signal.

The generation of SYSREF pulses is configured by SPI commands and is available after the initial setup of output clock divider and QREF phase delay stages.

An essential part of the SYSREF generation is the sequence of SPI commands to apply to synchronize the SYSREF pulses to the clock divider and delay state machines.

Table 2O. SYSREF Generation[1, 2]

SRO	NS				N_S	SYSREF Operation (f_{SYSREF}) for f_{VCO} (MHz)		
	3	2	1	0		f_{VCO} = 2457.6MHz	2500	2949.12
Counted Pulse Mode (Use the SRPC register to configure the number of generated SYSREF pulses)								
0	0	0	0	0	÷64	38.4	39.0625	46.08
	0	0	0	1	÷96	25.6	26.04166	30.72
	0	0	1	0	÷128	19.2	19.53125	23.04
	0	0	1	1	÷192	12.8	13.02083	15.36
	0	1	0	0	÷256	9.6	9.76562	11.52
	0	1	0	1	÷384	6.4	6.51041	7.68
	0	1	1	0	÷512	4.8	4.88281	5.76
	0	1	1	1	÷768	3.2	3.25520	3.84
	1	0	0	0	÷1024	2.4	2.44140	2.88
	1	0	0	1	÷2048	1.2	1.22070	1.44
Continues Pulse Mode								
1	0	0	0	0	÷64	38.4	39.0625	46.08
	0	0	0	1	÷96	25.6	26.04166	30.72
	0	0	1	0	÷128	19.2	19.53125	23.04
	0	0	1	1	÷192	12.8	13.02083	15.36
	0	1	0	0	÷256	9.6	9.76562	11.52
	0	1	0	1	÷384	6.4	6.51041	7.68
	0	1	1	0	÷512	4.8	4.88281	5.76
	0	1	1	1	÷768	3.2	3.25520	3.84
	1	0	0	0	÷1024	2.4	2.44140	2.88
	1	0	0	1	÷2048	1.2	1.22070	1.44

NOTE 1. SRO and SRPC are global settings. See Table 2P for the setting sequence to apply.
NOTE 2. SYSREF setting should only be used with 400mV and 700mV amplitude setting.

QCLK Phase Delay and SYSREF Synchronization Sequence (S2)

Precondition: Delay circuits are set to powered-up (nPOWER = 0). Set MUX = 1 to assign the SYSREF function to the QREF outputs, N_S to the SYSREF pulse rate and configure the SYSREF synchronizer divider value to the least common multiple value of N_A and N_B.

- Write SR_REQ0 = 1 (register 5). QREF outputs will power up.
- Write SR_REQ1 = 1 (register 25): N_S dividers are reset and synchronize.
- Write SR_RESET = 1 (register 29): Continuous clocks or a number of specified pulses will be generated at QREF outputs.

See Table 2P for detailed description of the sequences.

Table 2P. SYSREF Generation Sequence

SRO	SYSREF Pulse Mode	Operation
0	Counted	**Pre-condition:** • OUTEN = 1, MUX = 1, nPOWER = 0, A[1:0] = 01 • SPRC[7:0] contains the number of pulses to generate (1...255) • NS[3:0] contains the SYSREF divider • SYNC[3:0] is set to the least common multiple value of N_A and N_B.
		Start operation: apply sequence S2 • QREF output will power-up for SYSREF pulse generation. • The programmed number of SYSREF pulses is generated • QREF output will power down automatically • The three SR_REQ0, 1 and SR_RESET bits clear automatically
		Repeated use: apply sequence (S2) at any time
1	Continues	**Pre-condition:** • A[1:0] = 01 • MUX = 1, nPOWER = 0 • OUTEN = 1 • NS[3:0] contains the SYSREF divider • SYNC[3:0] is set to the least common multiple value of N_A and N_B.
		Start operation: apply sequence S2
		Stop operation: Set SRO = 0
		Restart function: Set SRO = 1 and apply sequence S2

Device Start-up, Reset and Synchronization

After the 8V19N408 first powers-up, an internal reset signal is auto-generated. The registers are initialized with the default values listed in the table for each register.

During startup, it is not required to apply an input clock to the CLK input: the VCXO-PLL will “free-run” with the frequency of the external VCXO. The control voltage of the external VCXO (LFV pin) will be held at $V_{DD}/2$ to support fast PLL lock and the VCXO-PLL will begin operation with their charge pumps in the middle of their operating range.

As a second step, the user should write the desired PLL dividers. Configure other operation settings such the output divider, SYSREF divider and output phase delay settings into the registers and apply software-controlled divider reset and QREF phase delay stage synchronization sequences. This is done by two separate SPI-controlled reset procedures which should be applied in the order below. First, apply the output divider reset sequence:

Clock Output Divider Reset Sequence, (Sequence S1)

- step 1: write logic 1 to the NR_REQ0 register bit
- step 2: write logic 1 to the NR_REQ1 register bit
- step 3: write logic 1 to the NR_RESET bit

This completes the reset of the output divider stages. Each subsequent change of any N output divider value requires to re-apply above divider reset sequence.

Then, configure the delay stages and when completed, apply the second sequence to synchronize the QREF output delay stages:

QREF Phase Delay and SYSREF Synchronization Sequence, (Sequence S2)

- step 1: write logic 1 to the SR_REQ0 register bit
- step 2: write logic 1 to the SR_REQ1 register bit
- step 3: write logic 1 to the SR_RESET bit

This completes the synchronization of the delay stages.
The clock divider reset sequence and the QREF phase delay & SYSREF synchronization sequence must be done in two separate SPI write cycles (do not combine both sequences in a single SPI write).

If sequences S1 and S2 are programmed in any order other than that which is recommended, this could result in an unknown state of the SYSREF generation. In order to reactivate the SYSREF Synchronization Sequence, power down QREF outputs by programming nPOWER bits to “1”. The device is now ready for a new SYSREF Synchronization Sequence.

Any change of the output divider values or delay stage configuration require to re-apply initialization/ synchronization through the respective SPI sequence individually.

When synchronizing the output delay stages through the synchronization sequence, care must be taken prevent writing a logic 1 to the NR_REQ0, NR_REQ1, NR_RESET register bits in the same base register write cycle (write a logic 0 to these bits, which will not affect them).

The QREF phase delay and SYSREF synchronization sequence is also used to trigger the synchronized generation of SYSREF pulses. The last steps, it is recommended to clear all interrupts in preparation to start monitoring the devices status bits.

Status Conditions & Interrupts

The 8V19N408 has an interrupt output to signal changes in status conditions. Settings for status conditions may be accessed in the Status and Interrupt Enable registers. The 8V19N408 has several conditions that can indicate faults and status changes in the operation of the device. These are shown in Table 2Q and can be monitored directly in the status registers. A changed bit on any or all of these can be programmed to generate an interrupt signal (nINT) via settings in the Interrupt Enable registers.

Table 2Q. Status Bit Functions

Bit Name	Function	Status if Bit is:	
		1	0
STAT[2]	VCO calibration	Completed	Not completed
STAT[1]	VCXO-PLL	Locked	Unlocked
STAT[0]	CLK state	Active	LOS

For the reference monitor circuit, if there has been no activity on the reference input for three consecutive clock edges (of the feedback 1st-stage VCXO signal) then the appropriate status bit will transition to a 0. It will not return to 1 until activity has resumed for three clock edges.

The lock detect circuit operate by monitoring the loop filter voltage on the first PLL (VCXO-PLL). If the monitored voltage exceeds a range, this indicates an out-of-lock condition.

It is normal when attempting to achieve lock for there to be multiple times when an out-of-lock condition as described above would occur before a full, stable lock is achieved. To prevent a bouncing status, the lock detect bit will not become asserted until the lock is stable. Once a stable lock has been achieved, this de-bounce circuit is deactivated so the lock-detect bit will de-assert immediately if a subsequent out-of-lock condition occurs.

The Interrupt and Interrupt Enable registers are used to control the behavior of the nINT output based on changes in the status indicators. If any of the status indicators STAT[1:0] change, that will set the corresponding INT[1:0] bit of the Interrupt registers. If any of the INT[1:0] bits are set and their corresponding interrupt enable bit INTEN[1:0] is asserted, it will generate an interrupt (low level on nINT).

Interrupts are cleared by writing a 1 to the appropriate INT[1:0] bit(s) in the Interrupt register after the underlying fault condition has been resolved. When all valid interrupt sources have been cleared in this manner, this will release the nINT output until the next unmasked fault.

SPI Mode Operation with MISO Output in High Impedance

SPI mode slave operation requires that some function external to the 8V19N408 has performed any necessary serial bus arbitration and/or address decoding at the level of the board or system. By default, the MISO data output is in high-impedance state. The 8V19N408 begins a cycle by detecting an asserted (low) state on the nLE input at a rising edge of SPICLK. This is also coincident with the first bit of data being shifted into the device. In SPI mode, the first bit is the Most Significant Bit (MSB) of the data word being written. Data must be written in 32-bit words, with nLE remaining asserted and one data bit being shifted in to the 8V19N408 on every rising edge of SPICLK. If nLE is deasserted (high) at any time except following the 32nd falling edge of SPICLK, then this is treated as an error and the shift register contents are discarded. No data is written to any internal registers. If nLE is deasserted (high) as expected after the 32nd falling edge of SPICLK, then this will result in the shift register contents being acted on according to the instructions (address + R/W) in it. During write operation, the MISO output remains in high-impedance state. The word format of the 32-bit quantity in the shift register is shown in Table 2S. The register fields in the 8V19N408 have been organized so that the 4 LSBs in each 32-bit register row are not used for data transfer. Three of these bits will represent the base address for the eight 32-bit base registers and the 4th bit indicates whether a read or write operation is requested. If a read operation is requested, 32-bits of read data will be provided in the immediately subsequent access. The nLE must be deasserted (high) and then reasserted (low). On the first SPICLK rising edge, once nLE is re-asserted to low state, the MISO output will turn to active state and one data bit will be placed on the MISO output at each rising edge of SPICLK as long as nLE remains asserted (low). If nLE is deasserted (high) before 32-bits of read data have been shifted out, the read cycle will be considered to be completed. If nLE remains asserted (low) longer than 32-bit times, then the data during those extra clock periods will be undefined. The MSB of the data will be presented first. When nLE is de-asserted (high), the MISO output will go into high impedance state and the SPI bus is available for transactions with other devices.

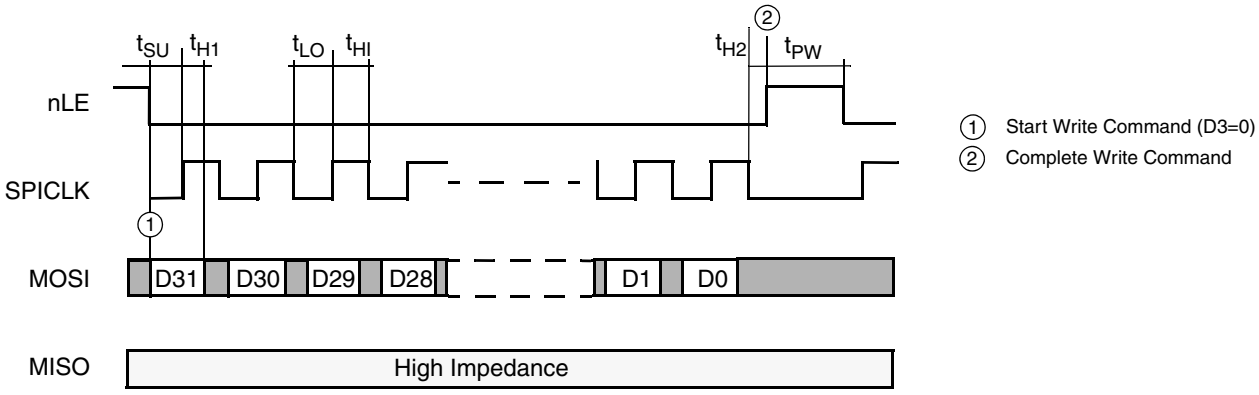


Figure 2. SPI Write Cycle Timing Diagram, MISO High Impedance

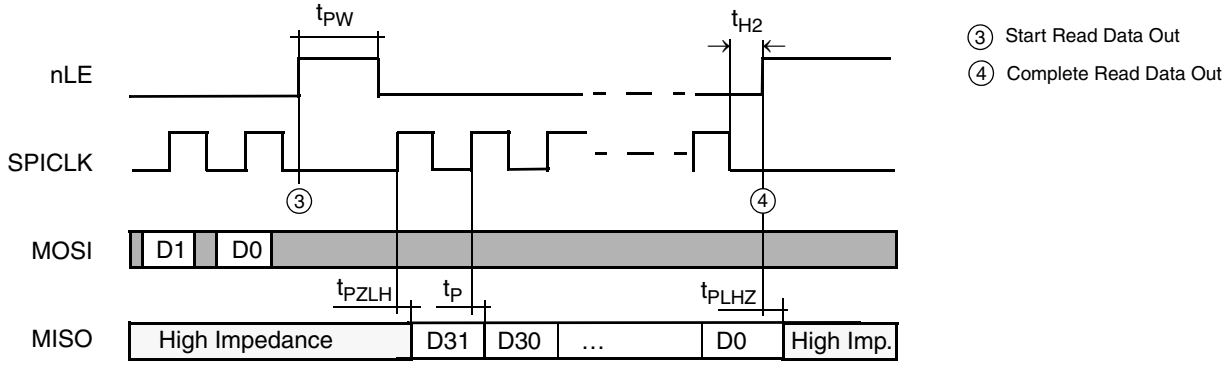


Figure 3. SPI Read Cycle Timing Diagram, MISO High Impedance

Table 2R. SPI Read / Write Cycle Timing Parameters

Symbol	Parameter	Test Condition	Minimum	Maximum	Unit
f_{CLK}	SPICLK frequency		-	20	MHz
t_{SU}	nLE, MOSI setup time to SPICLK		15	-	ns
t_{H1}	SPICLK to nLE, MOSI hold time		10	-	ns
t_{H2}	SPICLK falling edge to nLE rising edge, hold time		10	-	ns
t_{LO}	SPICLK low period		25	-	ns
t_{HI}	SPICLK high period		25	-	ns
t_{PW}	nLE deasserted pulse width		50	-	ns
t_{PZLH}	Propagation Delay, MISO Output High Impedance to Active High or Low	External pullup = 5kΩ		16	ns
t_{PLHZ}	Propagation Delay, MISO Output Active High or Low to High Impedance	External pullup = 5kΩ		2	ns
t_P	Propagation Delay, SPICLK to MISO	External pullup = 5kΩ		20	ns

Table 2S. SPI Interface I/O Voltage Select

SELSV	SPI Interface I/O Voltage (SPICLK, MOSI, MISO, nLE, nINT)
0	1.8V
1 (default)	3.3V

Register Descriptions

The Serial Control port of the 8V19N408 supports SPI mode operation.
Below indicates how registers may be accessed.

Table 3A. Register Map

Base Address	Register	Register Name	See	Default Setting	D7	D6	D5	D4	D3	D2	D1	D0
0	0	QCLKC Control	Table 3E	0000 XXXX	QC **DLY[5]**	QC **DLY[4]**	QC **DLY[3]**	QC **DLY[2]**	R/Wn	0	0	0
	1	M_V Feedback Divider Control	Table 3C	1111 1111	**MV[7]**	**MV[6]**	**MV[5]**	**MV[4]**	**MV[3]**	**MV[2]**	**MV[1]**	**MV[0]**
	2	M_{F0} Feedback Divider	Table 3C	0001 0000	**MF0[7]**	**MF0[6]**	**MF0[5]**	**MF0[4]**	**MF0[3]**	**MF0[2]**	**MF0[1]**	**MF0[0]**
	3	SYSREF Control	—	1000 0001	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	**SRO**
1	4	QCLKC Control QCLKB Control	Table 3E	0000 XXXX	QC **DLY[1]**	QC **DLY[0]**	QB **DLY[1]**	QB **DLY[0]**	R/Wn	0	0	1
	5	Reset Control M_V Feedback Divider Control	Table 3S Table 3C	X000 0000	**SR_REQ0**	**MV[14]**	**MV[13]**	**MV[12]**	**MV[11]**	**MV[10]**	**MV[9]**	**MV[8]**
	6	QREFA1, A0 Control	Table 3G	1000 1000	QREFA1 **A[1]**	QREFA1 **A[0]**	QREFA1 **EF**	QREFA1 **MUX**	QREFA0 **A[1]**	QREFA0 **A[0]**	QREFA0 **EF**	QREFA0 **MUX**
	7	Reset Control SYSREF Control	Table 3S Table 3K	X000 1000	**NR_REQ0**	Reserved	SYNC **nPOWER**	Reserved	SYNC **N[3]**	SYNC **N[2]**	SYNC **N[1]**	SYNC **N[0]**
2	8	QCLKB Control	Table 3E	0000 XXXX	QB **DLY[5]**	QB **DLY[4]**	QB **DLY[3]**	QB **DLY[2]**	R/Wn	0	1	0
	9	P_V Pre-Divider	Table 3C	1111 1111	**PV[7]**	**PV[6]**	**PV[5]**	**PV[4]**	**PV[3]**	**PV[2]**	**PV[1]**	**PV[0]**
	10	Status Control	Table 3O	XXXX X0XX	Reserved	**STAT2**	**STAT1**	**STAT0**	Reserved	Reserved	**INT1**	**INT0**
	11	SYSREF Control QREF B1, B0 Control	Table 3K Table 3G	0100 1111	**NS[3]**	**NS[2]**	**NS[1]**	**NS[0]**	QREFB1 **OE**	QREFB0 **OE**	QREFA1 **OE**	QREFA0 **OE**
3	12	QCLKA Control	Table 3E	0000 XXXX	QA **DLY[5]**	QA **DLY[4]**	QA **DLY[3]**	QA **DLY[2]**	R/Wn	0	1	1
	13	VCXO-PLL Control	Table 3I	0010 0000	**POLV**	**HOLD**	**CPV[5]**	**CPV[4]**	**CPV[3]**	**CPV[2]**	**CPV[1]**	**CPV[0]**
	14	M_{F1} Feedback Divider	Table 3C	0001 0000	**MF1[7]**	**MF1[6]**	**MF1[5]**	**MF1[4]**	**MF1[3]**	**MF1[2]**	**MF1[1]**	**MF1[0]**
	15	Reserved	—	1000 0000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4	16	QCLKA Control VCXO-PLL Control	Table 3E Table 3I	0000 XXXX	QA **DLY[1]**	QA **DLY[0]**	Reserved	**BYPASS**	R/Wn	1	0	0
	17	QREFA1 Control QREFA0 Control	Table 3G	0001 0001	QREFA1 **DLY[2]**	QREFA1 **DLY[1]**	QREFA1 **DLY[0]**	QREFA1 **nPOWER**	QREFA0 **DLY[2]**	QREFA0 **DLY[1]**	QREFA0 **DLY[0]**	QREFA0 **nPOWER**
	18	QCLKA Control	Table 3E	0000 0100	QCLKA **N[4]**	QCLKA **N[3]**	QCLKA **N[2]**	QCLKA **N[1]**	QCLKA **N[0]**	QA **OE**	Ch A **nPOWER**	Reserved
	19	QCLKB Control QCLKC Control	Table 3E	0000 0100	QCLKB **N[4]**	QCLKB **N[3]**	QCLKB **N[2]**	QCLKB **N[1]**	QCLKB **N[0]**	QB **OE**	Ch B **nPOWER**	QCLKC **N[0]**
5	20	QCLKC Control	Table 3E	0000 XXXX	QCLKC **N[4]**	QCLKC **N[3]**	QCLKC **N[2]**	QCLKC **N[1]**	R/Wn	1	0	1
	21	QREFB1 Control QREFB0 Control	Table 3G	0001 0001	QREFB1 **DLY[2]**	QREFB1 **DLY[1]**	QREFB1 **DLY[0]**	QREFB1 **nPOWER**	QREFB0 **DLY[2]**	QREFB0 **DLY[1]**	QREFB0 **DLY[0]**	QREFB0 **nPOWER**
	22	QREFB1 Control QREFB0 Control	Table 3G	1000 1000	QREFB1 **A[1]**	QREFB1 **A[0]**	QREFB1 **EF**	QREFB1 **MUX**	QREFB0 **A[1]**	QREFB0 **A[0]**	QREFB0 **EF**	QREFB0 **MUX**
	23	SYSREF Control	Table 3K	0000 0000	**SRPC[7]**	**SRPC[6]**	**SRPC[5]**	**SRPC[4]**	**SRPC[3]**	**SRPC[2]**	**SRPC[1]**	**SRPC[0]**

Table 3A. Register Map (Continued)

Base Address	Register	Register Name	See	Default Setting	D7	D6	D5	D4	D3	D2	D1	D0
6	24	QCLKC Control	Table 3E Table 3M	1000 XXXX	QC **OE**	Ch C **nPOWER**	Reserved	**SPI_REL**	R/Wn	1	1	0
	25	Reset Control QCLKB1, B0 Control	Table 3S Table 3E	X010 0100	**SR_REQ1**	Reserved	QCLKB1 **A[1]**	QCLKB1 **A[0]**	QCLKB1 **EF**	QCLKB0 **A[1]**	QCLKB0 **A[0]**	QCLKB0 **EF**
	26	QCLKA1, A0 Control	Table 3E	0010 0100	Reserved	Reserved	QCLKA1 **A[1]**	QCLKA1 **A[0]**	QCLKA1 **EF**	QCLKA0 **A[1]**	QCLKA0 **A[0]**	QCLKA0 **EF**
	27	Reset Control QVCXO Control	Table 3S Table 3E	X100 0001	**NR_REQ1**	QVCXO **A[1]**	QVCXO **A[0]**	QVCXO **EF**	Reserved	Reserved	Reserved	Reserved
7	28	QCLKC Control	Table 3E	1000 XXXX	QCLKC **A[1]**	QCLKC **A[0]**	QCLKC **EF**	Reserved	R/Wn	1	1	1
	29	Reset Control VCO Control	Table 3S Table 3M	X000 1010	**SR_RESET**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	30	VCO Control Interrupt Enable	Table 3M Table 3Q	0011 0000	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**VCO_SEL**	Reserved	**INTEN1**	**INTEN0**
	31	Reset Control	Table 3S	X011 1110	**NR_RESET**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	Reserved

PLL Divider Control Registers

The divider control registers contains the frequency divider settings for the VCXO-PLL and FemtoClock NG PLL.

Table 3B. PLL Divider Control Register Bit Allocations

Register	Register Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
1	**MV[7]**	**MV[6]**	**MV[5]**	**MV[4]**	**MV[3]**	**MV[2]**	**MV[1]**	**MV[0]**
2	**MF0[7]**	**MF0[6]**	**MF0[5]**	**MF0[4]**	**MF0[3]**	**MF0[2]**	**MF0[1]**	**MF0[0]**
5	SR_REQ0	**MV[14]**	**MV[13]**	**MV[12]**	**MV[11]**	**MV[10]**	**MV[9]**	**MV[8]**
9	**PV[7]**	**PV[6]**	**PV[5]**	**PV[4]**	**PV[3]**	**PV[2]**	**PV[1]**	**PV[0]**
14	**MF1[7]**	**MF1[6]**	**MF1[5]**	**MF1[4]**	**MF1[3]**	**MF1[2]**	**MF01[1]**	**MF1[0]**

Table 3C. PLL Divider Control Register Function Descriptions

Bits	Name	Factory Default	Function
M_V[14:0]	VCXO-PLL Feedback Divider	000 0000 1111 1111	VCXO-PLL Feedback Divider. Range: M_V = ÷4 to ÷32767. Binary encoding. Default divider: M_V = ÷255
P_V[7:0]	VCXO-PLL Pre-Divider	1111 1111	VCXO-PLL Pre Divider. Range: P_V = ÷1 to ÷255. Binary encoding. Default divider: P_V = ÷255
M_{F0}[7:0]	FemtoClock NG Feedback Divider	0001 0000	FemtoClock NG Feedback Divider for VCO-0. Range: M_{F0} = ÷8 to ÷255. Binary encoding. Default divider: M_{F0} = ÷16
M_{F1}[7:0]	FemtoClock NG Feedback Divider	0001 1000	FemtoClock NG Feedback Divider for VCO-1. Range: M_{F1} = ÷8 to ÷255. Binary encoding. Default divider: M_{F1} = ÷24

QCLK, QVCXO Control Registers

The QCLK, QVCXO Device Clock Output Control Registers contain the settings for the clock frequency divider, phase delay, power state, enable state, signal format and signal amplitude.

Table 3D. QCLKn, QVCXO Control Register Bit Allocations

Register	Register Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
0	QC **DLY[5]**	QC **DLY[4]**	QC **DLY[3]**	QC **DLY[2]**	R/W	0	0	0
4	QC **DLY[1]**	QC **DLY[0]**	QB **DLY[1]**	QB **DLY[0]**	R/W	0	0	1
8	QB **DLY[5]**	QB **DLY[4]**	QB **DLY[3]**	QB **DLY[2]**	R/W	0	1	0
12	QA **DLY[5]**	QA **DLY[4]**	QA **DLY[3]**	QA **DLY[2]**	R/W	0	1	1
16	QA **DLY[1]**	QA **DLY[0]**	Reserved	BYPASS	R/W	1	0	0
18	QCLKA **N[4]**	QCLKA **N[3]**	QCLKA **N[2]**	QCLKA **N[1]**	QCLKA **N[0]**	QA **OE**	Ch A **nPOWER**	Reserved
19	QCLKB **N[4]**	QCLKB **N[3]**	QCLKB **N[2]**	QCLKB **N[1]**	QCLKB **N[0]**	QB **OE**	Ch B **nPOWER**	QCLKC **N[0]**
20	QCLKC **N[4]**	QCLKC **N[3]**	QCLKC **N[2]**	QCLKC **N[1]**	R/Wn	1	0	1
24	QC **OE**	Ch C **nPOWER**	Reserved	SPI_REL	R/Wn	1	1	0
25	**SR_REQ1**	Reserved	QCLKB1 **A[1]**	QCLKB1 **A[0]**	QCLKB1 **EF**	QCLKB0 **A[1]**	QCLKB0 **A[0]**	QCLKB0 **EF**
26	Reserved	Reserved	QCLKA1 **A[1]**	QCLKA1 **A[0]**	QCLKA1 **EF**	QCLKA0 **A[1]**	QCLKA0 **A[0]**	QCLKA0 **EF**
27	NR_REQ1	QVCXO **A[1]**	QVCXO **A[0]**	QVCXO **EF**	Reserved	Reserved	Reserved	Reserved
28	QCLKC **A[1]**	QCLKC **A[0]**	QCLKC **EF**	Reserved	0	1	1	1

Table 3E. QCLK, QVCXO Control Register Function Descriptions

<table>
<tr><th>Bits</th><th>Name</th><th>Factory Default</th><th>Function</th></tr>
<tr><td>OE</td><td>QCLK Output Enable</td><td>1</td><td>1 = $QCLK_x$ output(s) are enabled
0 = $QCLK_x$ output(s) are disabled in the active low state
x denominate(s) the clock output(s) (e.g. x = B denominates QCLKB0 and CLKB1).</td></tr>
<tr><td>nPOWER</td><td>Clock Output Channel Power</td><td>0</td><td>1 = Output channel X is powered down
0 = Output channel X is powered up
x denominates the output channel A, B or C. A channel consists of the output divider and delay stage, e.g. Φ_A and N_A for channel A.</td></tr>
<tr><td>N_A[4:0],
N_B[4:0],
N_C[4:0]</td><td>Clock Divider Setting</td><td>00000</td><td>These bits control the value of the clock frequency divider and output frequency
<table>
<tr><th>N[4:0]</th><th>Clock Divider</th><th>N[4:0]</th><th>Clock Divider</th></tr>
<tr><td>00000</td><td>÷2</td><td>01000</td><td>÷16</td></tr>
<tr><td>00001</td><td>÷3</td><td>01001</td><td>÷20</td></tr>
<tr><td>00010</td><td>÷4</td><td>01010</td><td>÷24</td></tr>
<tr><td>00011</td><td>÷5</td><td>01011</td><td>÷32</td></tr>
<tr><td>00100</td><td>÷6</td><td>01100</td><td>÷40</td></tr>
<tr><td>00101</td><td>÷8</td><td>01101</td><td>÷48</td></tr>
<tr><td>00110</td><td>÷10</td><td>01110</td><td>÷80</td></tr>
<tr><td>00111</td><td>÷12</td><td>01111</td><td>÷96</td></tr>
<tr><td>10000</td><td>÷1</td><td>11011</td><td>÷64</td></tr>
</table></td></tr>
<tr><td>DLY[5:0]</td><td>Clock Phase Delay</td><td>000000</td><td>These bits control the selection of phase delay Φ of the clock outputs. One unit of Φ corresponds to the delay of $1/f_{VCO}$. For fine delay adjustments, use the delay circuits of the QREF outputs.
<table>
<tr><th>Φ</th><th>Delay</th></tr>
<tr><td>000000</td><td>0</td></tr>
<tr><td>000001</td><td>$1/f_{VCO}$</td></tr>
<tr><td>000010</td><td>$2\cdot (1/f_{VCO})$</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>Φ</td><td>$\Phi \cdot (1/f_{VCO})$</td></tr>
</table></td></tr>
<tr><td>EF</td><td>QCLK, QVCXO Output Format</td><td>0</td><td>Sets the output format:
0 = LVDS (Requires LVDS 100Ω output termination across a differential pair.
1 = LVPECL (Requires LVPECL 50Ω termination to the specified recommended termination voltage).</td></tr>
<tr><td>A[1:0]</td><td>QCLK,QVCXO Output Amplitude</td><td>10</td><td>
<table>
<tr><th colspan="3">QCLK, QVCXO Amplitude Control</th><th colspan="2">Output Termination</th></tr>
<tr><th>A[1]</th><th>A[0]</th><th>Amplitude</th><th>LVPECL (EF = 1)</th><th>LVDS (EF = 0)</th></tr>
<tr><td>0</td><td>0</td><td>Output is powered- down</td><td>Should not have any termination</td><td rowspan="4">100Ω across differential pair</td></tr>
<tr><td>0</td><td>1</td><td>400mV</td><td>50Ω to V_{DDx} - 1.5V</td></tr>
<tr><td>1</td><td>0</td><td>700mV</td><td>50Ω to V_{DDx} - 2V</td></tr>
<tr><td>1</td><td>1</td><td>1000mV, f_{OUT} >500MHz</td><td>50Ω to V_{DDx} - 2.5V</td></tr>
</table></td></tr>
</table>

QREF Output Control Registers

The QREF Control Registers contain the settings for the SYSREF output enable, power state, signal source and phase delay. Since the registers have an identical format and bit meaning, they are described only once.

Table 3F. QREF Output Control Register Bit Allocations

Register	Register Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
6	QREFA1 **A[1]**	QREFA1 **A[0]**	QREFA1 **EF**	QREFA1 **MUX**	QREFA0 **A[1]**	QREFA0 **A[0]**	QREFA0 **EF**	QREFA0 **MUX**
11	NS[3]	NS[2]	NS[1]	NS[0]	QREFB1 **OE**	QREFB0 **OE**	QREFA1 **OE**	QREFA0 **OE**
17	QREFA1 **DLY[2]**	QREFA1 **DLY[1]**	QREFA1 **DLY[0]**	QREFA1 **nPOWER**	QREFA0 **DLY[2]**	QREFA0 **DLY[1]**	QREFA0 **DLY[0]**	QREFA0 nPOWER
21	QREFB1 **DLY[2]**	QREFB1 **DLY[1]**	QREFB1 **DLY[0]**	QREFB0 **nPOWER**	QREFB0 **DLY[2]**	QREFB0 **DLY[1]**	QREFB0 **DLY[0]**	QREFB0 **nPOWER**
22	QREFB1 **A[1]**	QREFB1 **A[0]**	QREFB1 **EF**	QREFB1 **MUX**	QREFB0 **A[1]**	QREFB0 **A[0]**	QREFB0 **EF**	QREFB0 **MUX**

Table 3G. QREF Output Control Register Function Descriptions[1]

Bits	Name	Factory Default	Function				
MUX	QREF Signal Source	0	1 = $QREF_n$ signal source is the $QREF_n$ delay circuit (SYSREF mode) 0 = $QREF_n$ signal source is the respective N clock divider (Clock mode)				
nPOWER	Output Power	1	1 = $QREF_n$ and delay block is powered down 0 = $QREF_n$ and delay block is powered up				
DLY[2:0]	SYSREF Phase Delay Φ	000	These bits control the selection of phase-delay Φ of the QREF outputs.				
EF	QREF Output Format	0	Sets the QREF output format: 0 = $QREF_n$ is LVDS (Requires LVDS 100Ω output termination across a differential pair). Use this format for SYSREF or clock signals. 1 = $QREF_n$ is LVPECL (Requires LVPECL 50Ω output termination to the specified recommended termination voltage). Use this format for clock signals.				
A[1:0]	QREF Output Amplitude	10	**$QREF_n$ Amplitude Control**			**Output Termination**	
			A[1]	**A[0]**	**QREF Amplitude**	**LVPECL (EF = 1)**	**LVDS (EF = 0)**
			0	0	Powered-down	Should not have any termination.	100Ω across differential pair
			0	1	400mV	50Ω to V_{DDx} - 1.5V	
			1	0	700mV	50Ω to V_{DDx} - 2V	
			1	1	1000mV, f_{OUT} >500MHz	50Ω to V_{DDx} - 2.5V	
OE	QREF Enable	1	1 = QREF output is enabled 0 = QREF output is disabled in the active low state				

NOTE 1. n represents the output number.

VCXO-PLL Control Registers

The device control register contains settings for the VCXO-PLL charge pump and VCXO control voltage polarity and VCXO-bypass.

Table 3H. VCXO-PLL Control Register Bit Allocations

Register	Register Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
13	**POLV**	**HOLD**	**CPV[5]**	**CPV[4]**	**CPV[3]**	**CPV[2]**	**CPV[1]**	**CPV[0]**
16	QA DLY[1]	QA DLY[0]	Reserved	**BYPASS**	R/Wn	1	0	0

Table 3I. VCXO-PLL Control Register Function Descriptions

Bits	Name	Factory Default	Function
CPV[5:0]	VCXO-PLL Charge-Pump Current	10 0000	Controls the charge pump current of the VCXO-PLL. Charge pump current is the binary value of this register multiplied by 20µA. ICP = 20µA · CPV[5:0]. Default setting is 640µA (32 · 20µA)
POLV	VCXO Polarity	0	0 = Positive polarity. Use for an external VCXO with a positive f(V_C) characteristics. 1 = Negative polarity. Use for an external VCXO with a negative f(V_C) characteristics.
HOLD	Holdover Control	0	0 = Normal operation 1 = VCXO-PLL is set to holdover. The control voltage of the external VCXO is set to V_{DD}/2.
BYPASS	VCXO-PLL Bypass	0	0 = VCXO-PLL is enabled 1 = VCXO-PLL is bypassed

SYSREF Control Registers

The SYSREF pulse count register (SRPC) contains the binary setting for the number of SYSREF pulses generated by the device.

Table 3J. SYSREF Control Register Bit Allocations

Register	Register Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
3	VCO_DIV nPOWER	VCO N[3]	VCO N[2]	VCO N[1]	VCO N[0]	VCO nPOWER	Reserved	**SRO**
7	NR_REQ0	Reserved	SYNC **nPOWER**	Reserved	SYNC **N[3]**	SYNC **N[2]**	SYNC **N[1]**	SYNC **N[0]**
11	**NS[3]**	**NS[2]**	**NS[1]**	**NS[0]**	QREFB1 OE	QREFB0 OE	QREFA1 OE	QREFA0 OE
23	**SRPC[7]**	**SRPC[6]**	**SRPC[5]**	**SRPC[4]**	**SRPC[3]**	**SRPC[2]**	**SRPC[1]**	**SRPC[0]**

Table 3K. SYSREF Control Register Function Descriptions

Bits	Name	Factory Default	Function
SRPC[7:0]	SYSREF Pulse Count	0000 0000	Binary value of the SYSREF pulses generated by the 8V19N408 and output at all enabled QREF outputs. Allows to generate 1 to 255 pulses after each write access. Requires SRO = 0. The programmed number of SYSREF pulses is generated after the SYSREF synchronization procedure completes. See Section, "SYSREF Generation" on page 11.
NS[3:0]	SYSREF Frequency Divider	0100	**SYSREF Divider Value**

NS3	NS2	NS1	NS0	Value
0	0	0	0	÷64
0	0	0	1	÷96
0	0	1	0	÷128
0	0	1	1	÷192
0	1	0	0	÷256
0	1	0	1	÷384
0	1	1	0	÷512
0	1	1	1	÷768
1	0	0	0	÷1024
1	0	0	1	÷2048
1	0	X	X	1010-1111 are undefined.

Bits	Name	Factory Default	Function
SYNC nPOWER	Synchronizer Power Control	0	0 = SYSREF synchronizer power up 1 = SYSREF synchronizer power down Power down the SYSREF synchronizer if all QREFn outputs are used as clock outputs.
SYNC N[3:0]	SYSREF Synchronizer Divider	1000	SYSREF Synchronizer divider value. This divider controls the release of SYSREF pulses at coincident QCLKAn and QCLKBn clock edges. For SYSREF operation, set this divider value to the least common multiple of the clock divider values N_A and N_B. For instance, if N_A = ÷2 and N_B = ÷3, set the SYNC divider to ÷6 (SYNC[3:0] = 0100).

SYNC3	SYNC2	SYNC1	SYNC0	Value
0	0	0	0	÷2
0	0	0	1	÷3
0	0	1	0	÷4
0	0	1	1	÷5
0	1	0	0	÷6
0	1	0	1	÷8
0	1	1	0	÷10
0	1	1	1	÷12
1	0	0	0	÷16
1	0	0	1	÷20
1	0	1	0	÷24
1	0	1	1	÷32
1	1	0	0	÷40
1	1	0	1	÷48
1	1	1	0	÷80
1	1	1	1	÷96

Bits	Name	Factory Default	Function
SRO	SYSREF Operation	1	0 = Single SYSREF pulse generation mode. Number of pulses is controlled by SRPC[7:0]. 1 = Continuous SYSREF pulse generation

FemtoClock NG PLL Control Registers

The FemtoClock NG registers contain the setting for the divider, selection and power state.

Table 3L. FemtoClockNG PLL Control Register Bit Allocations

Register	Register Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
24	QC OE	Ch C nPOWER	Reserved	**SPI_REL**	R/Wn	1	1	0
30	Reserved	Reserved	Reserved	Reserved	**VCO_SEL**	Reserved	INTEN1	INTEN0

Table 3M. FemtoClockNG PLL Control Register Function Descriptions

Bits	Name	Factory Default	Function
VCO_SEL	VCO Frequency Select	0	0 = VCO-0 1 = VCO-1
SPI_REL	FemtoClock NG PLL Relock	0	0 = no effect 1 = Creates a pulse that forces a re-lock on the FemtoClock NG PLL. Bit auto-clears. (Any changes of VCO-PLL parameters, such as Feedback Divider M_{F0} and M_{F1} require re-locking using SPI_REL bit.)

Status Registers

This register contains the clock status bits STAT[2:0] and latched copies of these bits (INT[1:0]).

Table 3N. Status Register Bit Allocations

Register	Register Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
10		**STAT2**	**STAT1**	**STAT0**		Reserved	**INT1**	**INT0**

Table 3O. Status Register Function Descriptions

Bits	Name	Factory Default	Function
STAT2	VCO Calibration	-	VCO calibration status: 1 = Completed 0 = Not completed
STAT1	VCXO-PLL Lock Status	-	VCXO-PLL (1st stage) lock status: 1 = VCXO-PLL is locked 0 = VCXO-PLL is unlocked
STAT0	Clock Input CLK Status	-	CLK Input clock status: 1 = CLK input clock is present 0 = CLK input clock not detected
INT[1:0]	Individual Interrupt Status & Clear Bits	-	These bits contain a latched version of the STAT[1:0] bits: The INT[1:0] bits indicate a fault condition (0) since the last interrupt clear command. Writing a 1 to a INT[1:0] bit position will clear that interrupt latch, provided the corresponding fault condition has also been cleared. Clearing the latch with the corresponding STAT[1:0] bit still indicating a fault (0) will result in an immediate re-trigger of the latch.

Interrupt Enable Register

This register controls the interrupt functions of the 8V19N408.

Table 3P. Interrupt Enable Register Bit Allocations

Register	Register Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
30	Reserved	Reserved	Reserved	Reserved	SEL	Reserved	**INTEN1**	**INTEN0**

Table 3Q. Interrupt Enable Register Function Descriptions

Bits	Name	Factory Default	Function
INTEN[1:0]	Interrupt Enable Bits	00	A setting of 0 in any of these bit positions will mask the corresponding INT[1:0] latch bit from affecting the interrupt output signal (nINT). A setting of 1 in any bit position will enable that INT[1:0] latch bit to drive the interrupt signal nINT. Setting all INTEN[1:0] to 0 has the effect of disabling interrupts from the device.

Reset Control Registers

The Reset Control Registers contain the settings for the register controlled-reset and restart capabilities of the device. Output divider reset (NR_REQ0, NR_REQ1, NR_RESET): the divider reset sequence is required after device startup and after any N divider value change. See Section, “Clock Output Divider Reset Sequence, (Sequence S1)” on page 12.

The QREF phase delay and SYSREF synchronization sequence is required for the synchronization of the delay stages after each delay stage configuration, and is also applicable for the generation of SYSREF pulses. Sequence: write a logic 1 to SR_REQ0, SR_REQ1 and SR_RESET in this order to generate a programmable number of SYSREF pulses at all enabled QREF outputs. See Section, “QREF Phase Delay and SYSREF Synchronization Sequence, (Sequence S2)” on page 12.

Table 3R. Reset Control Register Bit Allocations

Register	Register Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
5	**SR_REQ0**	MV[14]	MV[13]	MV[12]	MV[11]	MV[10]	MV[9]	MV[8]
7	**NR_REQ0**	Reserved	SYNC nPOWER	Reserved	SYNC N[3]	SYNC N[2]	SYNC N[1]	SYNC N[0]
25	**SR_REQ1**	Reserved	QCLKB1 A[1]	QCLKB1 A[0]	QCLKB1 EF	QCLKB0 A[1]	QCLKB0 A[0]	QCLKB0 EF
27	**NR_REQ1**	QVCXO A[1]	QVCXO A[0]	QVCXO EF	Reserved	Reserved	Reserved	Reserved
29	**SR_RESET**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31	**NR_RESET**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 3S. Reset Control Register Function Descriptions

Bits	Name	Factory Default	Function
NR_REQ0	N_A, N_B, N_C Output Divider Reset Request 0[1], Auto-clear	X	Writing a 1 to the bit position D7 in register 7 is the first step of the reset/re-synchronization sequence for the frequency dividers N_{A-C}. All QCLK outputs are set to the logic low stage. This bit auto-clears after the reset sequence. Writing a 0 to this bit position has no effect.
NR_REQ1	N_A, N_B, N_C Output Divider Reset Request 1, Auto-clear	X	Writing a 1 to the bit position D7 in register 29 is the second step of the reset/re-synchronization sequence for the frequency dividers N_{A-C}. After this bit is set to logic 1, the dividers N_{A-C} can be reset synchronously by writing a logic 1 to the NR_RESET bit (register 31, bit position D7) Independent on the selected output dividers N_{A-C}, the QCLK outputs will then restart with a rising edge simultaneously. This bit clears itself after the completion of the reset sequence and QCLKA-C outputs are reset. Writing a 0 to this bit position has no effect.
NR_RESET	N_A, N_B, N_C Output Divider Divider Reset Auto-clear	X	Writing a 1 to the bit position D7 in register 31 is the third and final step of the reset/re-synchronization sequence for the frequency dividers N_{A-C}. The dividers re-start synchronously up to 10 clock periods after this reset bit is written. This bit clears itself after the completion of the reset sequence and QCLK[A:C] outputs are reset. Writing a 0 to this bit position has no effect.
SR_REQ0	SYSREF Synchronization Request 0[2], Auto-clear	X	Writing a 1 to the bit position D7 in register 5 is the first step of the synchronization sequence for the SYSREF outputs (QREF). This bit auto-clears after the reset sequence. Writing a 0 to this bit position has no effect. Requires SRO = 0, otherwise no function.
SR_REQ1	SYSREF Synchronization Request 1, Auto-clear	X	Writing a 1 to the bit position D7 in register 27 is the second step of the synchronization sequence for the SYSREF outputs (QREF). The N_S divider is reset. The SYSREF outputs are active and set to logic low level in preparation to the last step (SR_RESET). SRO = 0, otherwise no function. This bit clears itself after the completion of the reset sequence and QREF outputs are reset. Writing a 0 to this bit position has no effect.
SR_RESET	SYSREF Synchronization Reset Auto-clear	X	Writing a 1 to the bit position D7 in register 29 is the third and final step of the synchronization sequence for the SYSREF outputs (QREF). After writing a 1 to SR_RESET, the number of SYSREF pulses programmed in SRPC[7:0] are synchronously output at all enabled QREF outputs. This bit clears itself after the completion of the synchronization sequence. Writing a 0 to this bit position has no effect. SRO = 0, otherwise no function.

NOTE 1. See Section, “Clock Output Divider Reset Sequence, (Sequence S1)” on page 12.
NOTE 2. See Section, “QREF Phase Delay and SYSREF Synchronization Sequence, (Sequence S2)” on page 12.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DDx}	4.6V
Inputs	-0.5V to V_{DDx} + 0.5V
Outputs, V_O (LVCMOS)	-0.5V to V_{DDx} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Outputs, I_O (LVDS) Continuous Current Surge Current	 10mA 15mA
Junction Temperature, T_J	125°C
Storage Temperature, T_{STG}	-65°C to 150°C

Table 4B. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	nLE, MOSI, SPICLK			4		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	MISO, nINT	SELSV = 1 (3.3V)		30		Ω
			SELSV = 0 (1.8V)		40		Ω

DC Electrical Characteristics

Table 5A. Power Supply DC Characteristics, V_{DDx} = V_{DDQx} = 3.3V ± 5%, T_A = -40°C to +85°C[1, 2, 3, 4]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DDx}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDQx}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DDx}	Power Supply Current[5]	LVPECL Output Setting		327	350	mA
		LVDS Output Setting		345	370	mA
I_{DDQx}	Output Supply Current: LVPECL[5, 6]	400mV Amplitude Setting		295	400	mA
		700mV Amplitude Setting		311	420	mA
		1000mV Amplitude Setting, f_{OUT} >500MHz		349	460	mA
	Output Supply Current: LVDS[5, 7]	400mV Amplitude Setting		432	550	mA
		700mV Amplitude Setting		499	620	mA
		1000mV Amplitude Setting, f_{OUT} >500MHz		585	670	mA

NOTE 1. V_{DDx} denotes V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}, V_{DD5}, V_{DD6} and V_{DD7}.
NOTE 2. V_{DDQx} denotes V_{DDQA}, V_{DDQB} and V_{DDQC}.
NOTE 3. I_{DDx} denotes I_{DD1}, I_{DD2}, I_{DD3}, I_{DD4}, I_{DD5}, I_{DD6} and I_{DD7}.
NOTE 4. I_{DDQx} denotes I_{DDQA}, I_{DDQB} and I_{DDQC}.
NOTE 5. Both VCXO-PLL and FemtoClock NG PLL are locked and all output clocks are running (QREFn are in QCLK mode). SYSREF delay stages and synchronizer control are disabled.
NOTE 6. Outputs not terminated.
NOTE 7. Outputs not terminated with 100Ω across the differential pair.

Table 5B. LVCMOS/LVTTL DC Characteristics, V_{DDx} = V_{DDQx} = 3.3V ± 5%, T_A = -40°C to +85°C[1, 2]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		SELSV = 0	1.3		1.8	V
			SELSV = 1	2.3		V_{DDX}	V
V_{IL}	Input Low Voltage		SELSV = 0	-0.3		0.35	V
			SELSV = 1	-0.3		0.6	V
I_{IH}	Input High Current	SPICLK, nLE, MOSI	V_{DD5} = 3.3V, V_{IN} = 3.3V			150	µA
		SELSV	V_{DD5} = 3.3V, V_{IN} = 3.3V			5	µA
I_{IL}	Input Low Current	SPICLK, nLE, MOSI	V_{DD5} = 3.465V, V_{IN} = 0V	-5			µA
		SELSV	V_{DD5} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage	nINT, MISO	V_{DDQx} = 3.465V, SELSV = 0 I_{OH} = -2mA	1.65			V
			V_{DDQx} = 3.465V, SELSV = 1 I_{OH} = -4mA	2.0			V
V_{OL}	Output Low Voltage	nINT, MISO	V_{DDQx} = 3.465V, SELSV = 0 I_{OL} = 2mA			0.15	V
			V_{DDQx} = 3.465V, SELSV = 1 I_{OL} = 4mA			0.5	V

NOTE 1. V_{DDx} denotes: V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}, V_{DD5}, V_{DD6} and V_{DD7}.
NOTE 2. V_{DDQx} denotes V_{DDQA}, V_{DDQB}, V_{DDQC}.

Table 5C. Differential Input DC Characteristics, V_{DD5} = 3.3V ± 5%, T_A = -40°C to +85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK, VCXO, nVCXO	V_{DD5} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK, VCXO	V_{DD5} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK, nVCXO	V_{DD5} = 3.465V, V_{IN} = 0V	-150			µA

Table 5D. LVPECL DC Characteristics (QCLKn, EF = 1), V_{DDQx} = 3.3V ± 5%, GND = 0V, T_A = -40°C to +85°C[1]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage[2]	400mV Amplitude Setting	V_{DDQX} – 1.41	V_{DDQX} – 0.9	V_{DDQX} – 0.55	V
		700mV Amplitude Setting				
		1000mV Amplitude Setting, f_{OUT} >500MHz				
V_{OL}	Output Low Voltage[2]	400mV Amplitude Setting	V_{DDQX} – 1.66	V_{DDQX} – 1.3	V_{DDQX} – 1.11	V
		700mV Amplitude Setting	V_{DDQX} – 1.965	V_{DDQX} – 1.6	V_{DDQX} – 1.35	V
		1000mV Amplitude Setting, f_{OUT} >500MHz	V_{DDQX} – 2.22	V_{DDQX} – 2.0	V_{DDQX} – 1.5	V

NOTE 1. V_{DDQx} denotes V_{DDQA}, V_{DDQB} and V_{DDQC}.
NOTE 2. Outputs terminated with 50Ω to V_{DDQx} – 1.5V (400mV amplitude setting), V_{DDQx} – 2.0V (700mV amplitude setting), V_{DDQx} – 2.5V (1000mV amplitude setting).

Table 5E. LVDS DC Characteristics (QCLKn, EF = 0), V_{DDQx} = 3.3V ± 5%, GND = 0V, T_A = -40°C to +85°C[1]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OS}	Offset Voltage[2]	400mV Amplitude Setting		2.3		V
		700mV Amplitude Setting		2.1		V
		1000mV Amplitude Setting, f_{OUT} >500MHz		1.9		V
ΔV_{OS}	V_{OS} Magnitude Change			20		mV

NOTE 1. V_{DDQx} denotes V_{DDQA}, V_{DDQB} and V_{DDQC}.
NOTE 2. V_{OS} changes with V_{DD}.

Table 5F. LVDS DC Characteristics (QREFn), V_{DDQx} = 3.3V ± 5%, GND = 0V, T_A = -40°C to +85°C[1]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OS}	Offset Voltage[2]	400mV Amplitude Setting		2.3		V
		700mV Amplitude Setting		2.1		V
		1000mV Amplitude Setting, f_{OUT} >500MHz		1.9		V
ΔV_{OS}	V_{OS} Magnitude Change			20		mV

NOTE 1. V_{DDQx} denotes V_{DDQA}, V_{DDQB} and V_{DDQC}.
NOTE 2. V_{OS} changes with V_{DD}.

AC Electrical Characteristics

Table 6A. AC Characteristics, V_{DDx} = V_{DDQx} = 3.3V ± 5%, GND = 0V, T_A = -40°C to +85°C[1, 2, 3]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{VCO}	VCO Frequency Range		VCO-0	2400		2500	MHz
			VCO-1	2920		3000	MHz
f_{OUT}	Output Frequency	QCLKx	400mV Amplitude Setting	f_{VCO} ÷ 96		f_{VCO}	MHz
			700mV Amplitude Setting	f_{VCO} ÷ 96			
			1000mV Amplitude Setting	500			
		QREFx	400mV Amplitude Setting	f_{VCO} ÷ 96		f_{VCO}	MHz
			700mV Amplitude Setting	f_{VCO} ÷ 96			
			1000mV Amplitude Setting	500			
V_{PP}	Peak-to-Peak Input Voltage[4]	CLK, nCLK		0.2		1.4	V
V_{CMR}	Common Mode Input Voltage[5]			1.1		V_{DD} – 0.3	V
$V_{O(PP)}$[6]	LVPECL Output Voltage Swing, Peak-to-Peak		400mV Amplitude Setting	310	425	570	mV
			700mV Amplitude Setting	500	730	1020	mV
			1000mV Amplitude Setting	870	1080	1200	mV
	LVPECL Differential Output Voltage Swing, Peak-to-peak		400mV Amplitude Setting	620	850	1140	mV
			700mV Amplitude Setting	1000	1460	2040	mV
			1000mV Amplitude Setting	1740	2160	2400	mV
V_{OD}	LVDS Differential Output Voltage[7]		400mV Amplitude Setting	600	800	1000	mV
			700mV Amplitude Setting	950	1400	1850	mV
			1000mV Amplitude Setting	1450	2140	2600	mV
ΔV_{OD}	LVDS V_{OD} Magnitude Change					50	mV
*t*sk(o)	Output Skew[8, 9]	QCLKx	Same N Divider, Delay = 0		65	110	ps
		QCLKx	Any N Divider, Incident Rising Edge, Delay = 0		75	140	ps
		QREFx	Delay = 0		20	50	ps
		QREFx	Any Equal Delay Settings		20	50	ps
		QREFx to QCLKx	Any Divider, Incident Rising QCLK Edge, Delay = 0		110	200	ps
t_R / t_F	Output Rise/Fall Time, Differential	QCLK (LVPECL)	20% to 80% 700mV Amplitude Setting		150	300	ps
		QCLK (LVDS)	20% to 80% 700mV Amplitude Setting		150	300	ps
	Output Rise/Fall Time[10]	nINT, MISO (LVCMOS)	20%-80% - SELSV = 0		1000	2650	ps
			20%-80% - SELSV = 1		600	1000	ps
	Output Isolation		f_{OUT} = 1228.8MHz	52	58	77	dB
			f_{OUT} = 614.4MHz	55	59	80	dB
			f_{OUT} = 307.2MHz	58	69	79	dB

Table 6A. AC Characteristics, V_{DDx} = V_{DDQx} = 3.3V ± 5%, GND = 0V, T_A = -40°C to +85°C[1, 2, 3] (Continued)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
odc	Output Duty Cycle	QCLK[8:0], QREF[6:0]	Divide by1	42	48	54	%
			Other Dividers	45	50	55	%
t_{LOCK}	PLL Lock Time		VCXO-PLL Bandwidth = 30Hz, Device fully powered, measured from the first presence of a valid PLL reference clock to the complete lock of all PLLs		210	1000	ms

NOTE 1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2. V_{DDx} denotes V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}, V_{DD5}, V_{DD6} and V_{DD7}.

NOTE 3. V_{DDQx} denotes V_{DDQA}, V_{DDQB} and V_{DDQC}.

NOTE 4. V_{IL} should not be less than -0.3V.

NOTE 5. Common mode input voltage is defined as the signal crosspoint.

NOTE 6. LVPECL outputs terminated with 50Ω to V_{DDQx} – 1.5V (400mV amplitude setting), V_{DDQx} – 2.0V (700mV amplitude setting), V_{DDQx} – 2.5V (1000mV amplitude setting).

NOTE 7. LVDS outputs terminated 100Ω across terminals.

NOTE 8. This parameter is defined in accordance with JEDEC standard 65.

NOTE 9. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

NOTE 10. Single-ended output nINT terminated according to Figure 12.

Table 6B. VCO-0 QCLK Phase Noise and Jitter Characteristics, $V_{DDx} = V_{DDQx} = 3.3V \pm 5\%$, GND = 0V, T_A = -40°C to +85°C[1, 2, 3, 4, 5, 6, 7]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f = 1228.8MHz						
tjit(Ø)	RMS Phase Jitter (Random)	Integration Range: 1kHz - 76.8MHz		82.5	114.1	fs
		Integration Range: 12kHz - 20MHz		73.7	103.5	fs
$\Phi_N(10)$	Single-side Band Phase Noise	10Hz offset from Carrier		-52.5		dBc/Hz
$\Phi_N(100)$		100Hz offset from Carrier		-86.8		dBc/Hz
$\Phi_N(1k)$		1kHz offset from Carrier		-116.9	-111.7	dBc/Hz
$\Phi_N(10k)$		10kHz offset from Carrier		-118.1	-114.1	dBc/Hz
$\Phi_N(100k)$		100kHz offset from Carrier		-122.7	-119.4	dBc/Hz
$\Phi_N(800k)$		800kHz offset from Carrier		-142.7	-139.8	dBc/Hz
$\Phi_N(1M)$		1MHz offset from Carrier		-144.7	-141.7	dBc/Hz
$\Phi_N(\infty)$		Noise Floor		-154		dBc/Hz
	Spurious Attenuation	300Hz - 100kHz		-92	-75	dBc
		>100kHz		-85	-74	dBc
		Phase Detector Spurious		-68	-60	dBc
f = 614.4MHz						
tjit(Ø)	RMS Phase Jitter (Random)	Integration Range: 1kHz - 76.8MHz		90.9	127.7	fs
		Integration Range: 12kHz - 20MHz		80.4	112.2	fs
$\Phi_N(10)$	Single-side Band Phase Noise	10Hz offset from Carrier		-56.8		dBc/Hz
$\Phi_N(100)$		100Hz offset from Carrier		-90.9		dBc/Hz
$\Phi_N(1k)$		1kHz offset from Carrier		-121.9	-115.0	dBc/Hz
$\Phi_N(10k)$		10kHz offset from Carrier		-123.8	-119.3	dBc/Hz
$\Phi_N(100k)$		100kHz offset from Carrier		-128.4	-125.1	dBc/Hz
$\Phi_N(800k)$		800kHz offset from Carrier		-147.7	-144.7	dBc/Hz
$\Phi_N(1M)$		1MHz offset from Carrier		-149.4	-146.3	dBc/Hz
$\Phi_N(\infty)$		Noise Floor		-154		dBc/Hz
	Spurious Attenuation	300Hz - 100kHz		-95	-81	dBc
		>100kHz		-85	-69	dBc
		Phase Detector Spurious		-79	-68	dBc
f = 307.2MHz						
tjit(Ø)	RMS Phase Jitter (Random)	Integration Range: 1kHz - 76.8MHz		91.6	129.8	fs
		Integration Range: 12kHz - 20MHz		81.0	112.2	fs
$\Phi_N(10)$	Single-side Band Phase Noise	10Hz offset from Carrier		-63.6		dBc/Hz
$\Phi_N(100)$		100Hz offset from Carrier		-97.6		dBc/Hz
$\Phi_N(1k)$		1kHz offset from Carrier		-128.5	-118.3	dBc/Hz
$\Phi_N(10k)$		10kHz offset from Carrier		-130.8	-122.0	dBc/Hz
$\Phi_N(100k)$		100kHz offset from Carrier		-135.8	-115.7	dBc/Hz
$\Phi_N(800k)$		800kHz offset from Carrier		-153.4	-146.3	dBc/Hz
$\Phi_N(1M)$		1MHz offset from Carrier		-154.6	-148.3	dBc/Hz
$\Phi_N(\infty)$		Noise Floor		-160		dBc/Hz

Table 6B. VCO-0 QCLK Phase Noise and Jitter Characteristics, V_{DDx} = V_{DDQx} = 3.3V ± 5%, GND = 0V, T_A = -40°C to +85°C[1, 2, 3, 4, 5, 6, 7]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
	Spurious Attenuation	300Hz - 100kHz		-98	-81	dBc
		>100kHz		-96	-79	dBc
		Phase Detector Spurious		-80		dBc

NOTE 1. V_{DDx} denotes V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}, V_{DD5}, V_{DD6} and V_{DD7}.
NOTE 2. V_{DDQx} denotes V_{DDQA}, V_{DDQB} and V_{DDQC}.
NOTE 3. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 4. Voltage regulator to supply V_{DDX} was used with a typical power supply rejection ratio of 80dB at 1kHz and ultra low noise generation with a typical value of 3nV/√Hz at 10kHz and 7nV/√Hz at 1kHz.
NOTE 5. A VCXO has been used with Phase Noise and Spurious Attenuation measurements with typical values of 1kHz -131dBc/Hz, 10kHz -155dBc/Hz, 100kHz -160dBc/Hz and 1MHz -162dBc/Hz.
NOTE 6. Phase noise and spurious specifications apply for device operation with QREFn outputs inactive (no SYSREF pulses generated).
NOTE 7. Outputs configured as LVDS 700MHz.

Table 6C. VCO-0 QREF Phase Noise and Spurious Characteristics, V_{DDx} = V_{DDQx} = 3.3V ± 5%, GND = 0V, T_A = -40°C to +85°C[1, 2, 3, 4, 5, 6, 7]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Φ_N(1k)	Single-side Band Phase Noise (SYSREF = 19.2MHz)	1kz offset from Carrier		-137.8		dBc/Hz
Φ_N(10k)		10kHz offset from Carrier		-147.8		dBc/Hz
Φ_N(100k)		100kHz offset from Carrier		-154.8		dBc/Hz
Φ_N(1M)		1MHz offset from Carrier		-156		dBc/Hz
	Spurious Attenuation	300Hz - 100kHz		-80		dBc
		>100kHz		-75		dBc
		Phase Detector Spurious		-80		dBc

NOTE 1. V_{DDx} denotes V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}, V_{DD5}, V_{DD6} and V_{DD7}.
NOTE 2. V_{DDQx} denotes V_{DDQA}, V_{DDQB} and V_{DDQC}.
NOTE 3. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 4. Phase noise and spurious specifications apply for device operation with QREFn outputs inactive (no SYSREF pulses generated)..
NOTE 5. Voltage regulator to supply V_{DDX} was used with a typical power supply rejection ratio of 80dB at 1kHz and ultra low noise generation with a typical value of 3nV/√Hz at 10kHz and 7nV/√Hz at 1kHz.
NOTE 6. A VCXO has been used with Phase Noise and Spurious Attenuation measurements with typical values of 1kHz -131dBc/Hz, 10kHz -155dBc/Hz, 100kHz -160dBc/Hz and 1MHz -162dBc/Hz.
NOTE 7. Outputs configured as LVDS 700MHz.

Table 6D. VCO-1 QCLK Phase Noise and Jitter Characteristics, V_{DDx} = V_{DDQx} = 3.3V ± 5%, GND = 0V, T_A = -40°C to +85°C[1, 2, 3, 4, 5, 6, 7]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f = 1474.56MHz						
fjit(Ø)	RMS Phase Jitter (Random)	Integration Range: 1kHz - 76.8MHz		91.6	131.3	fs
		Integration Range: 12kHz - 20MHz		83.3	120.0	fs
Φ_N(10)	Single-side Band Phase Noise	10Hz offset from Carrier		-49		dBc/Hz
Φ_N(100)		100Hz offset from Carrier		-82.8		dBc/Hz
Φ_N(1k)		1kHz offset from Carrier		-113.4	-99.9	dBc/Hz
Φ_N(10k)		10kHz offset from Carrier		-115.0	-110.1	dBc/Hz
Φ_N(100k)		100kHz offset from Carrier		-120.1	-116.7	dBc/Hz
Φ_N(800k)		800kHz offset from Carrier		-141.1	-138.2	dBc/Hz
Φ_N(1M)		1MHz offset from Carrier		-143.1	-140.1	dBc/Hz
Φ_N(∞)		Noise Floor		-153		dBc/Hz
	Spurious Attenuation	300Hz - 100kHz		-78		dBc
		>100kHz		-68		dBc
		Phase Detector Spurious		-62		dBc
f = 737.28MHz						
fjit(Ø)	RMS Phase Jitter (Random)	Integration Range: 1kHz - 76.8MHz		103.7	147.3	fs
		Integration Range: 12kHz - 20MHz		91.2	131.5	fs
Φ_N(10)	Single-side Band Phase Noise	10Hz offset from Carrier		-54.9		dBc/Hz
Φ_N(100)		100Hz offset from Carrier		-89.7		dBc/Hz
Φ_N(1k)		1kHz offset from Carrier		-119	-106	dBc/Hz
Φ_N(10k)		10kHz offset from Carrier		-120.2	-115.8	dBc/Hz
Φ_N(100k)		100kHz offset from Carrier		-125.5	-122.0	dBc/Hz
Φ_N(800k)		800kHz offset from Carrier		-146.0	-143.3	dBc/Hz
Φ_N(1M)		1MHz offset from Carrier		-147.9	-145.0	dBc/Hz
Φ_N(∞)		Noise Floor		-155		dBc/Hz
	Spurious Attenuation	300Hz - 100kHz		-80		dBc
		>100kHz		-63		dBc
		Phase Detector Spurious		-70		dBc
f = 368.64MHz						
fjit(Ø)	RMS Phase Jitter (Random)	Integration Range: 1kHz - 76.8MHz		121.6	168.1	fs
		Integration Range: 12kHz - 20MHz		95.2	136.0	fs
Φ_N(10)	Single-side Band Phase Noise	10Hz offset from Carrier		-61.6		dBc/Hz
Φ_N(100)		100Hz offset from Carrier		-95.9		dBc/Hz
Φ_N(1k)		1kHz offset from Carrier		-126.0	-118.2	dBc/Hz
Φ_N(10k)		10kHz offset from Carrier		-126.3	-122.4	dBc/Hz
Φ_N(100k)		100kHz offset from Carrier		-131.6	-128.4	dBc/Hz
Φ_N(800k)		800kHz offset from Carrier		-151.3	-148.5	dBc/Hz
Φ_N(1M)		1MHz offset from Carrier		-152.7	-149.8	dBc/Hz
Φ_N(∞)		Noise Floor		-156		dBc/Hz

Table 6D. VCO-1 QCLK Phase Noise and Jitter Characteristics, V_{DDx} = V_{DDQx} = 3.3V ± 5%, GND = 0V, T_A = -40°C to +85°C[1, 2, 3, 4, 5, 6, 7]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
	Spurious Attenuation	300Hz - 100kHz		-80		dBc
		>100kHz		-67		dBc
		Phase Detector Spurious		-62		dBc

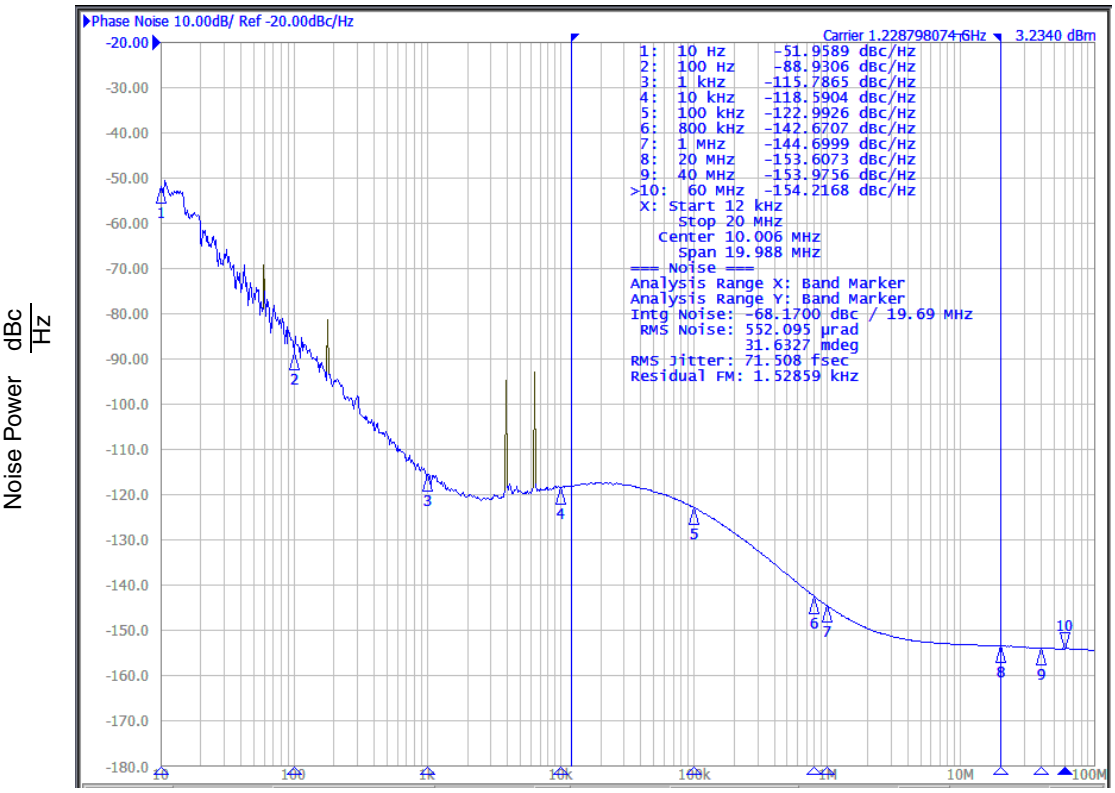
NOTE 1. V_{DDx} denotes V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}, V_{DD5}, V_{DD6} and V_{DD7}.
NOTE 2. V_{DDQx} denotes V_{DDQA}, V_{DDQB} and V_{DDQC}.
NOTE 3. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 4. Phase noise and spurious specifications apply for device operation with QREFn outputs inactive (no SYSREF pulses generated).
NOTE 5. Voltage regulator to supply V_{DDX} was used with a typical power supply rejection ratio of 80dB at 1kHz and ultra low noise generation with a typical value of 3nV/√Hz at 10kHz and 7nV/√Hz at 1kHz.
NOTE 6. A VCXO has been used with Phase Noise and Spurious Attenuation measurements with typical values of 1kHz -131dBc/Hz, 10kHz -155dBc/Hz, 100kHz -160dBc/Hz and 1MHz -162dBc/Hz.
NOTE 7. Outputs configured as LVDS 700MHz.

Table 6E. VCO-1 QREF Phase Noise and Spurious Characteristics, V_{DDx} = V_{DDQx} = 3.3V ± 5%, GND = 0V, T_A = -40°C to +85°C[1, 2, 3, 4, 5, 6, 7]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Φ_N(1k)	Single-side Band Phase Noise (SYSREF = 23.04MHz)	1kz offset from Carrier		-133.4		dBc/Hz
Φ_N(10k)		10kHz offset from Carrier		-144.9		dBc/Hz
Φ_N(100k)		100kHz offset from Carrier		-153.8		dBc/Hz
Φ_N(1M)		1MHz offset from Carrier		-155.4		dBc/Hz
	Spurious Attenuation	300Hz - 100kHz		-80		dBc
		>100kHz		-70		dBc
		Phase Detector Spurious		-80		dBc

NOTE 1. V_{DDx} denotes V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}, V_{DD5}, V_{DD6} and V_{DD7}.
NOTE 2. V_{DDQx} denotes V_{DDQA}, V_{DDQB} and V_{DDQC}.
NOTE 3. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 4. Phase noise and spurious specifications apply for device operation with QREFn outputs inactive.
NOTE 5. Voltage regulator to supply V_{DDX} was used with a typical power supply rejection ratio of 80dB at 1kHz and ultra low noise generation with a typical value of 3nV/√Hz at 10kHz and 7nV/√Hz at 1kHz.
NOTE 6. A VCXO has been used with Phase Noise and Spurious Attenuation measurements with typical values of 1kHz -131dBc/Hz, 10kHz -155dBc/Hz, 100kHz -160dBc/Hz and 1MHz -162dBc/Hz.
NOTE 7. Outputs configured as LVDS 700MHz.

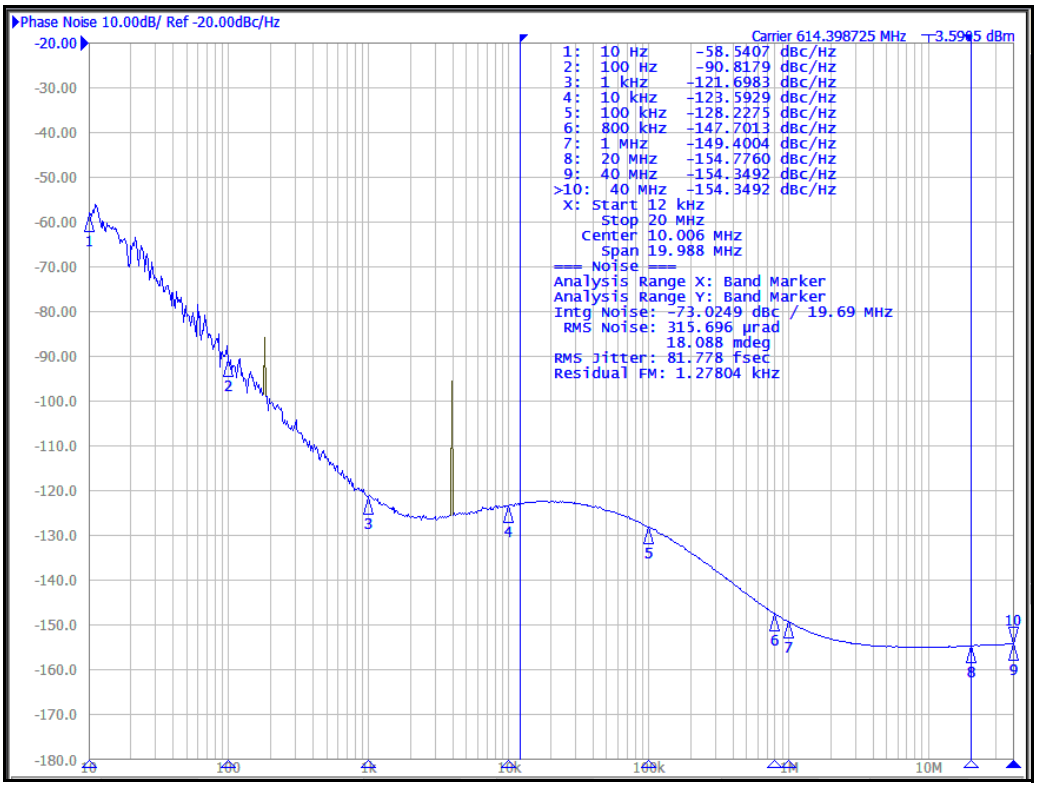
Typical Phase Noise at 1228.8MHz



Noise Power dBc/Hz

Offset Frequency (Hz)

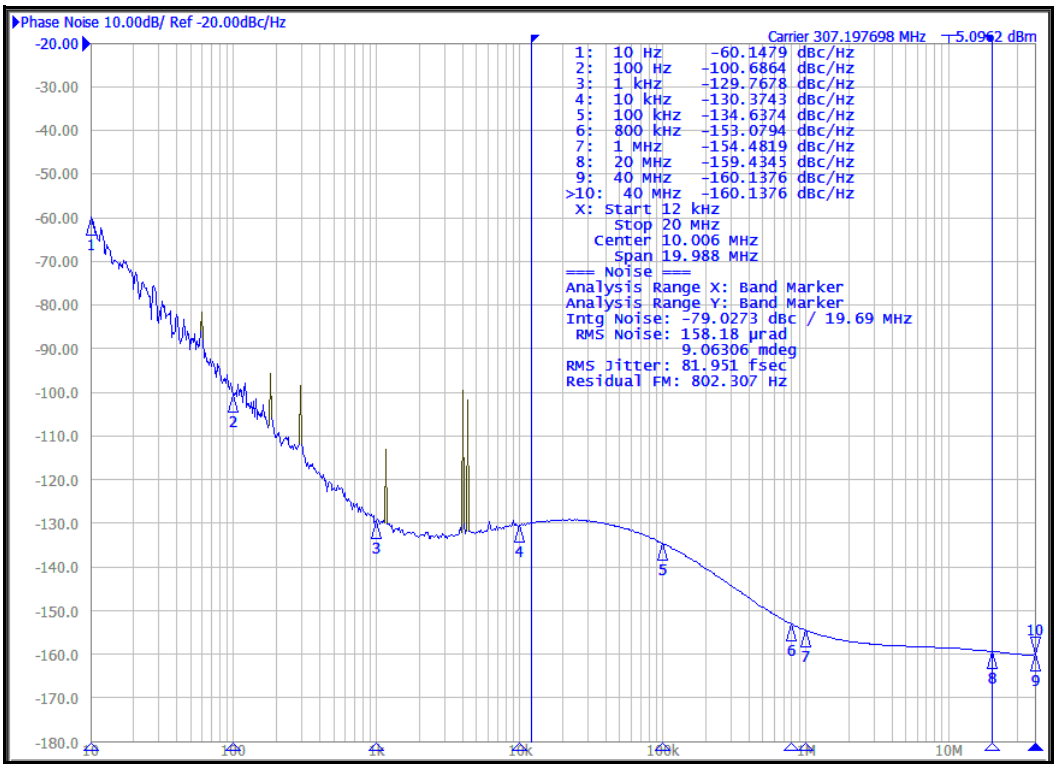
Typical Phase Noise at 614.4MHz



Noise Power dBc/Hz

Offset Frequency (Hz)

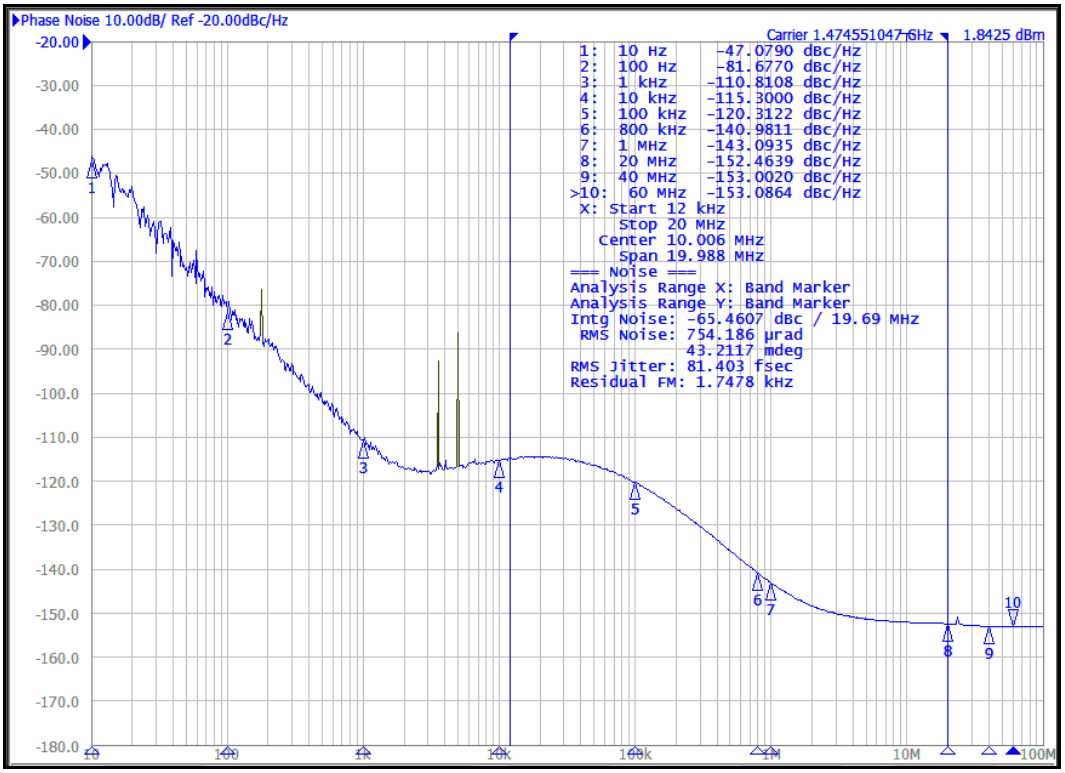
Typical Phase Noise at 307.2MHz



Noise Power dBc/Hz

Offset Frequency (Hz)

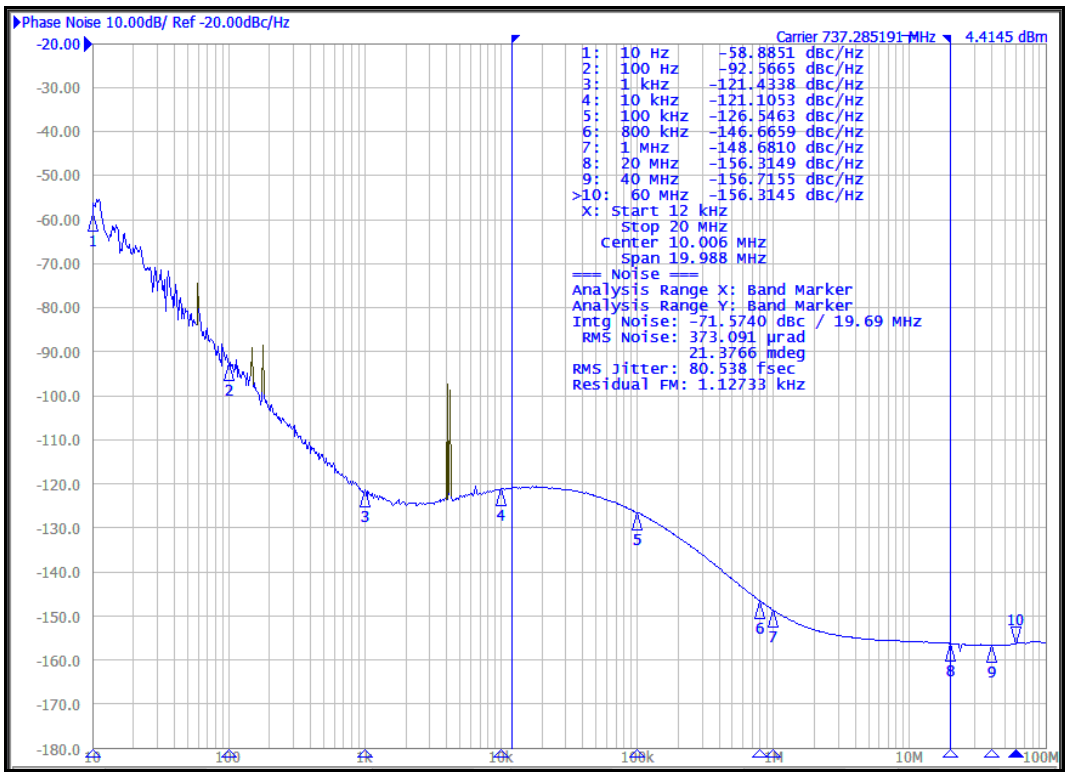
Typical Phase Noise at 1474.56MHz



Noise Power dBc/Hz

Offset Frequency (Hz)

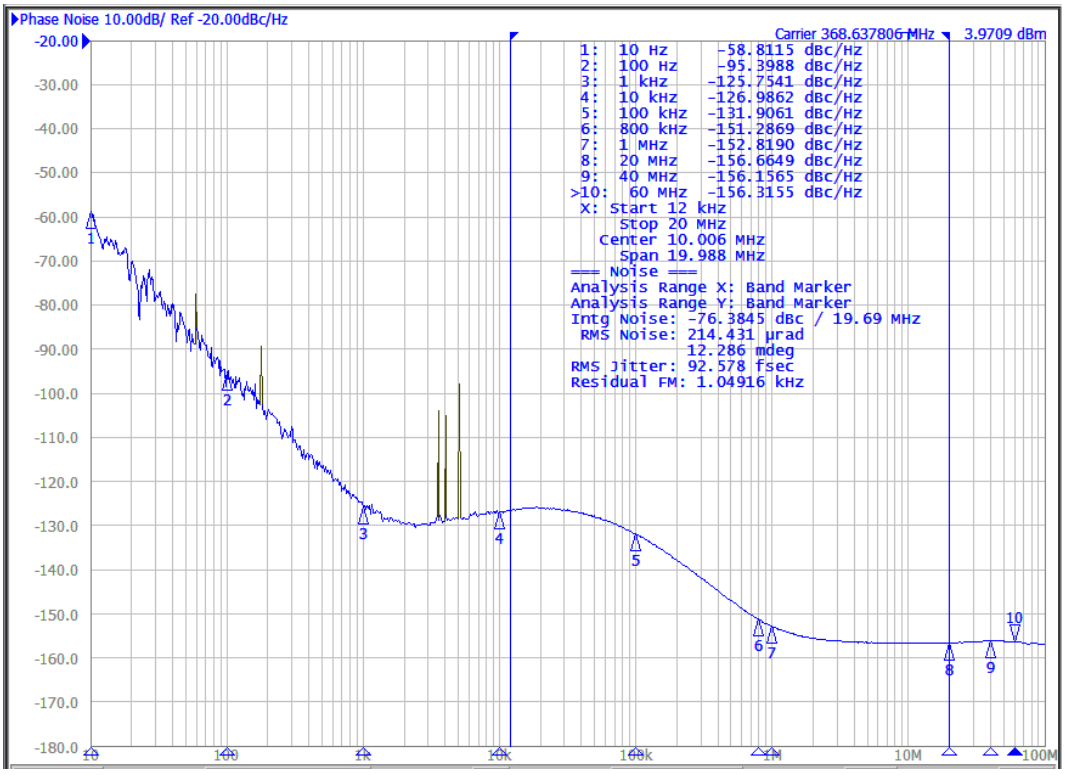
Typical Phase Noise at 737.28MHz



Noise Power dBc/Hz

Offset Frequency (Hz)

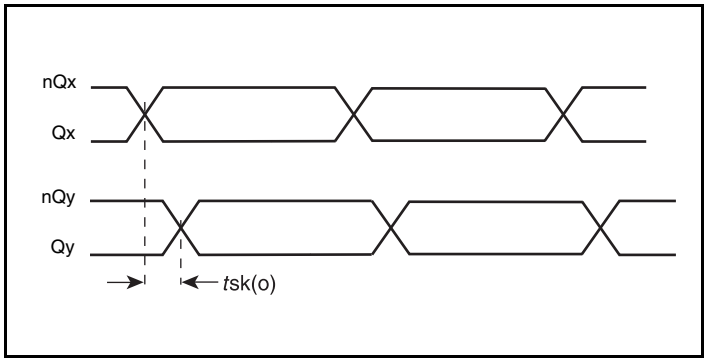
Typical Phase Noise at 368.64MHz



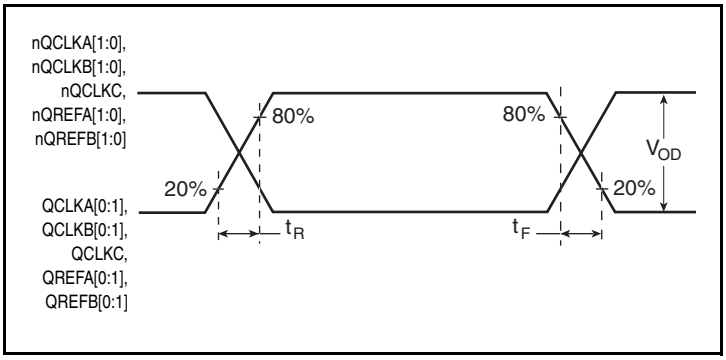
Noise Power dBc/Hz

Offset Frequency (Hz)

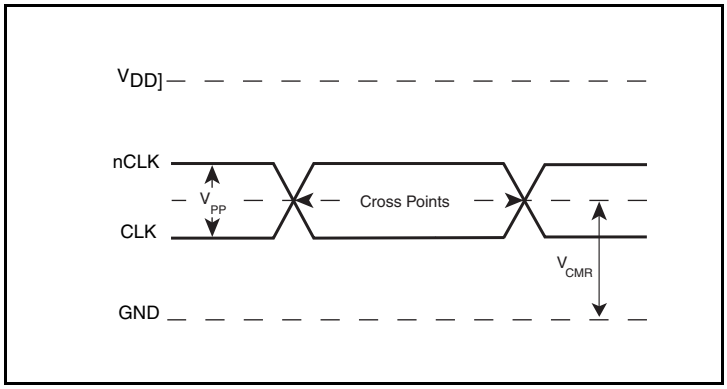
Parameter Measurement Information



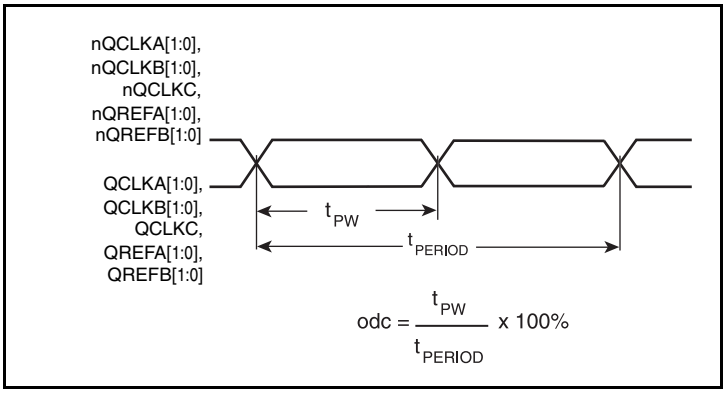
Differential Output Skew



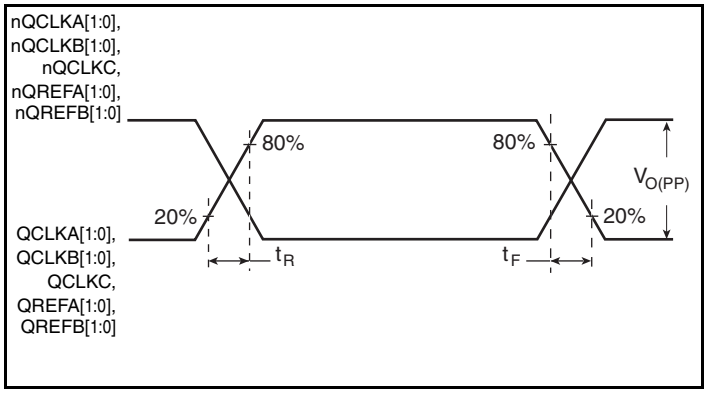
LVDS Output Rise/Fall Time



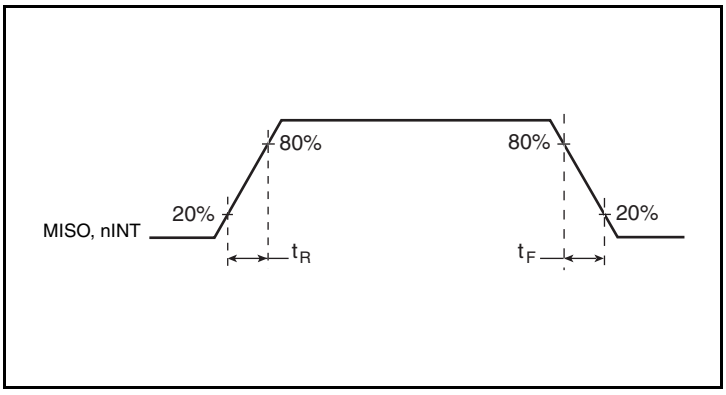
Differential Input Level



Differential Output Duty Cycle/Pulse Width/Period



LVPECL Output Rise/Fall Time



LVCMOS Output Rise/Fall Time

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

Any unused LVPECL output pair can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 4 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced while maintaining an edge rate faster than 1V/ns. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

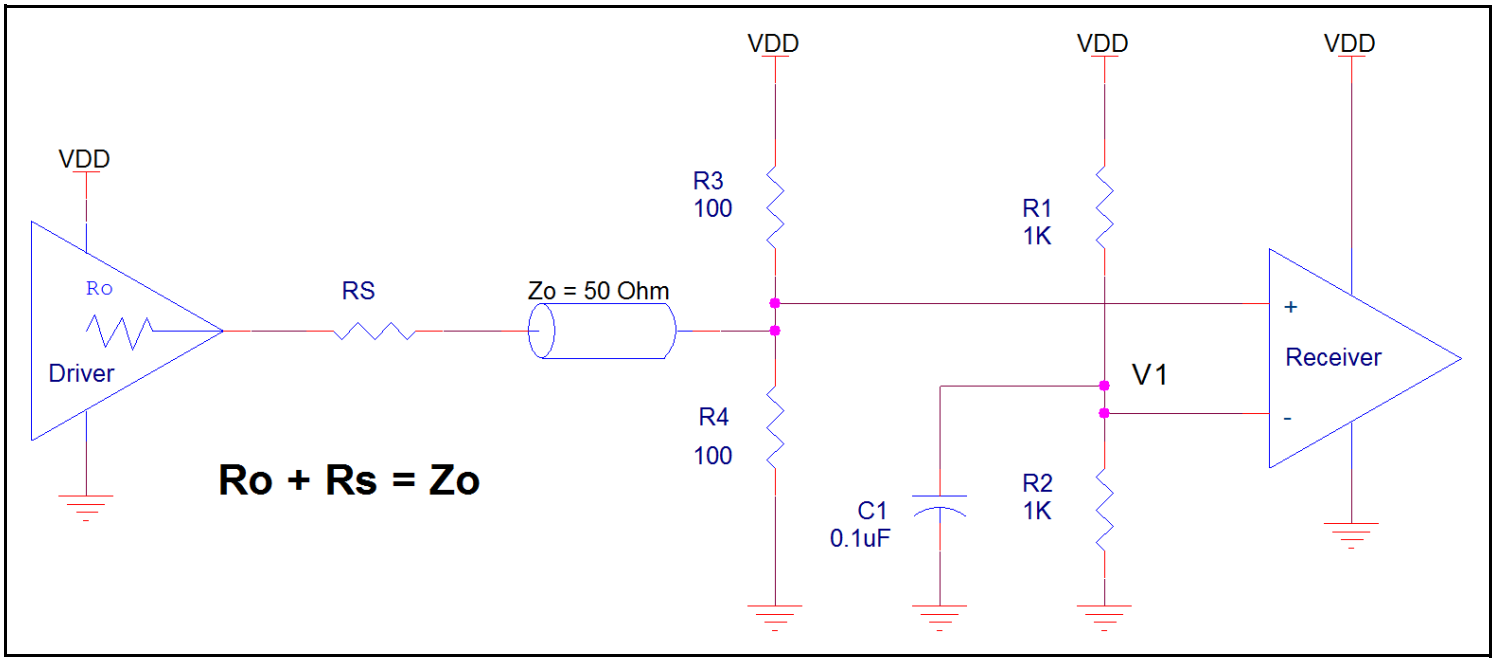


Figure 4. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL and other differential signals. Both differential inputs must meet the V_{PP} and V_{CMR} input requirements. Figure 5A *to* Figure 5C show interface examples for the CLK /nCLK input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

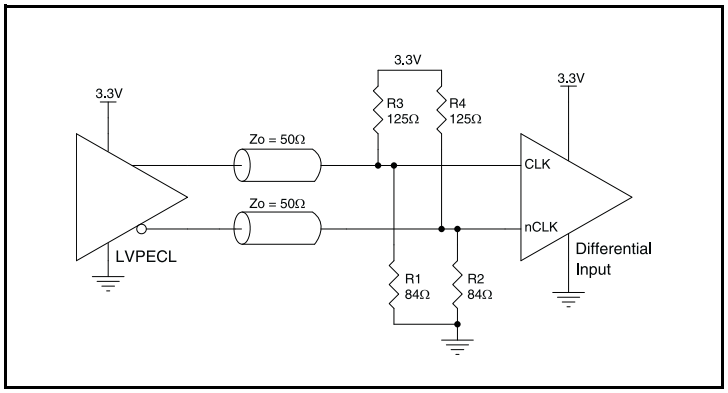


Figure 5A. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

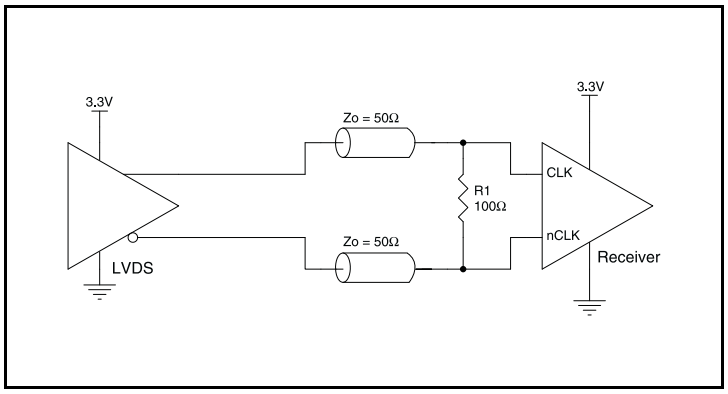


Figure 5C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

Figure 5B. CLK/nCLK Input Driven by a 3.3V LVDS Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 6. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

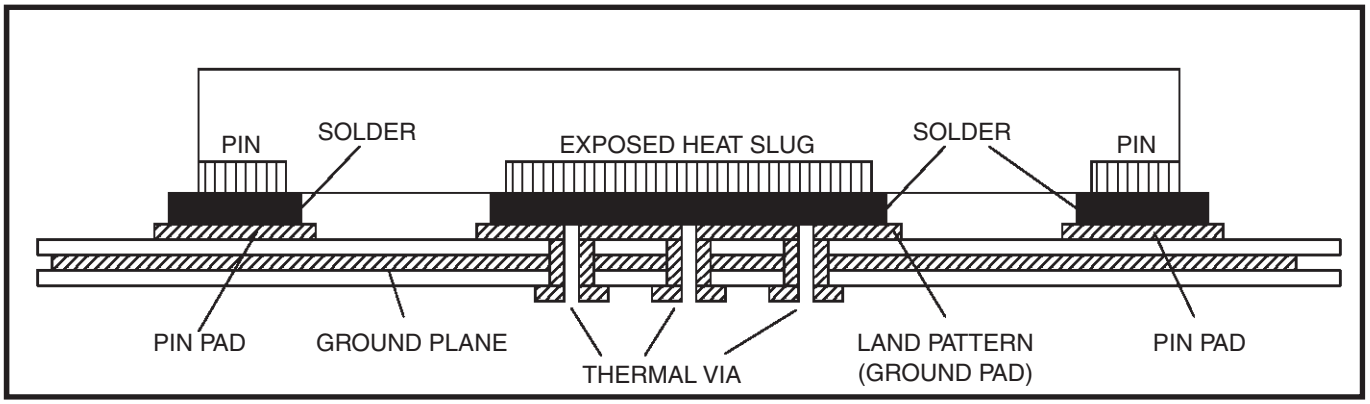


Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Termination Information

Termination for QCLK LVPECL Outputs (EF = 1)

Figure 7 shows an example of the termination for a QCLK LVPECL driver. In this example, the transmission line characteristic impedance is 50Ω. The R1 and R2 50Ω resistors are matched load terminations and are terminated to the voltage V_T. V_T should be set to a voltage according to the output amplitude in Table 2G. The termination resistors must be placed close to the receiver (line end)

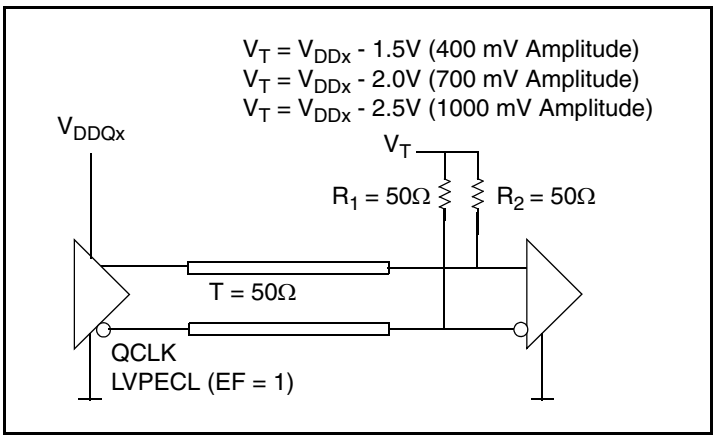


Figure 7. QCLK LVPECL (EF = 1) Output Termination

Termination for QCLK LVDS Outputs (EF = 0)

Figure 8 *and* Figure 9 show examples of the termination for a QCLK and QREF LVDS drivers. In these examples, the transmission line characteristic impedance is 50Ω. The 100Ω resistor R is matched to the line impedance. The output amplitude is configurable, see Table 2G. The termination resistor must be placed close to the receiver (line end) or is internal to the receiver.

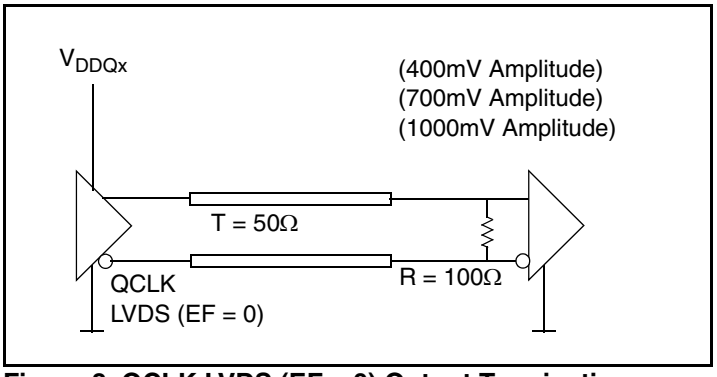


Figure 8. QCLK LVDS (EF = 0) Output Termination

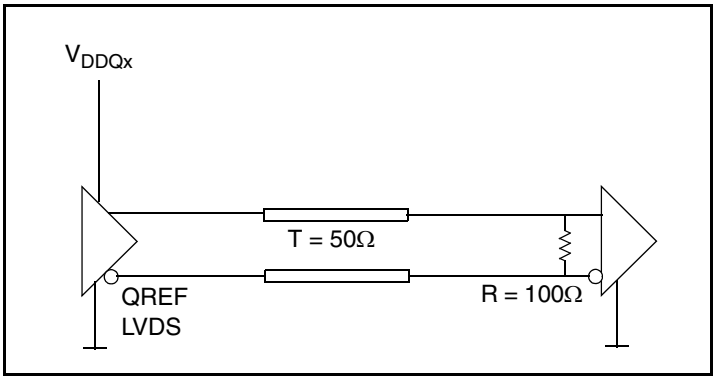


Figure 9. DC Termination for QREF LVDS Outputs

AC Termination for QREF LVDS Outputs

Figure 10 shows an example of the AC termination for the QREF LVDS driver. In this example, the transmission line characteristic impedance is 50Ω. A 100Ω AC-line termination must be placed close to the receiver (line end) or is internal to the receiver. The receiver input should be re-biased according to its common mode range specifications.

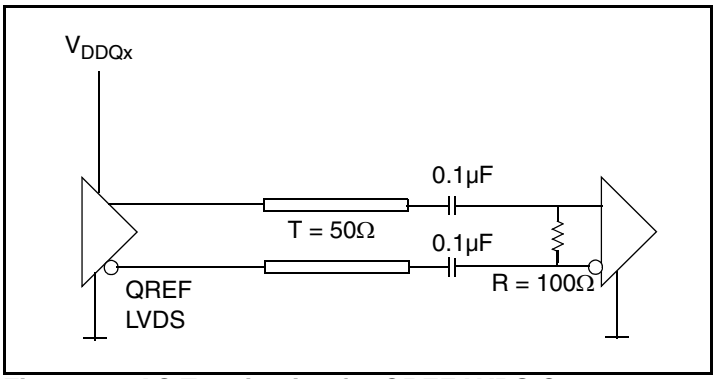


Figure 10. AC Termination for QREF LVDS Outputs

Figure 11 shows an example of the termination for the QREF LVDS driver. In this example, the transmission line characteristic impedance is 50Ω. The 100Ω resistor R is matched to the line impedance. The output amplitude is configurable, see Table 2G. The termination resistor must be placed close to the receiver (line end). A The receiver input should be re-biased according to its common mode range specifications.

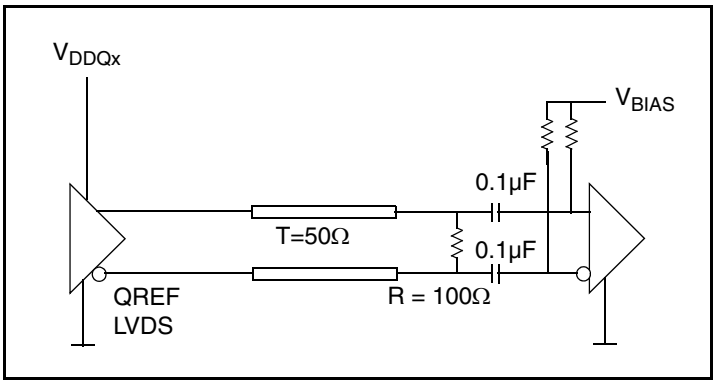


Figure 11. AC Termination for QREF LVDS Outputs

Termination for Single-ended Outputs (nINT)

.

Figure 12 shows an example of the series termination for the nINT LVCMOS driver. In this example, the transmission line characteristic impedance is 50Ω.

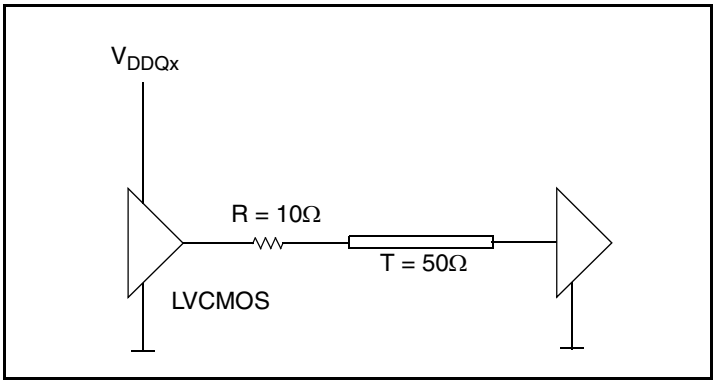


Figure 12. Termination for single-ended Outputs

Schematic Example

Figure 13 and Figure 14 below show an example 8V19N408 application schematic in which the device is operated at V_{DD} = 3.3V.

This example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set for the application.

The required generic VCXO shown requires a separate power filter and a termination for the VCXO output type. Since the type is not specified, neither is a specific termination. The loop filter for the external VCXO is three poles for best out of band rejection. The corresponding loop filters for the internal VCOs are specified as three poles even though only two poles are populated. This leaves the option of increasing the filter order based on system level test.

The output terminations and clock receivers shown in Figure 13 are representative examples. AC coupled LVDS terminations are also permissible as shown in the Termination Information section.

As with any high speed analog circuitry, the power supply pins are vulnerable to board supply or device generated noise. This device requires an external voltage regulator for the V_{DDx} pins for isolation of board supply noise. This regulator is indicated in the schematic by the two different power supplies, VREG_3.3V and 3.3V. Consult the voltage regulator specification for details of the required performance.

To achieve the very low jitter performance the 8V19N408 is capable of, power supply isolation is required to minimize device generated noise on any $V_{DD[1:7]}$ or $V_{DDQ[A:C]}$ power pin from coupling back into any other $V_{DD[1:7]}$ or $V_{DDQ[A:C]}$ power pin. The number of power pins supplied on the part was determined by the number of most significant coupling paths between the V_{DDs} of internal functions. Since the effective number of mixing products is a combinatorial function of the number of coupling frequencies and their amplitude, the separate filtering of the power pins minimizes the number and amplitude of the mixing products that can propagate to each output as spurs. These power filters, shown in Figure 14, also have the added benefit of reducing the switching currents that are injected back into the board power supply.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited the 0.1uf capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB. Pull up and pull down resistors to set configuration pins can all be placed on the PCB side opposite the device side to free up device side area if necessary.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

For additional layout recommendations and guidelines, contact clocks@idt.com.

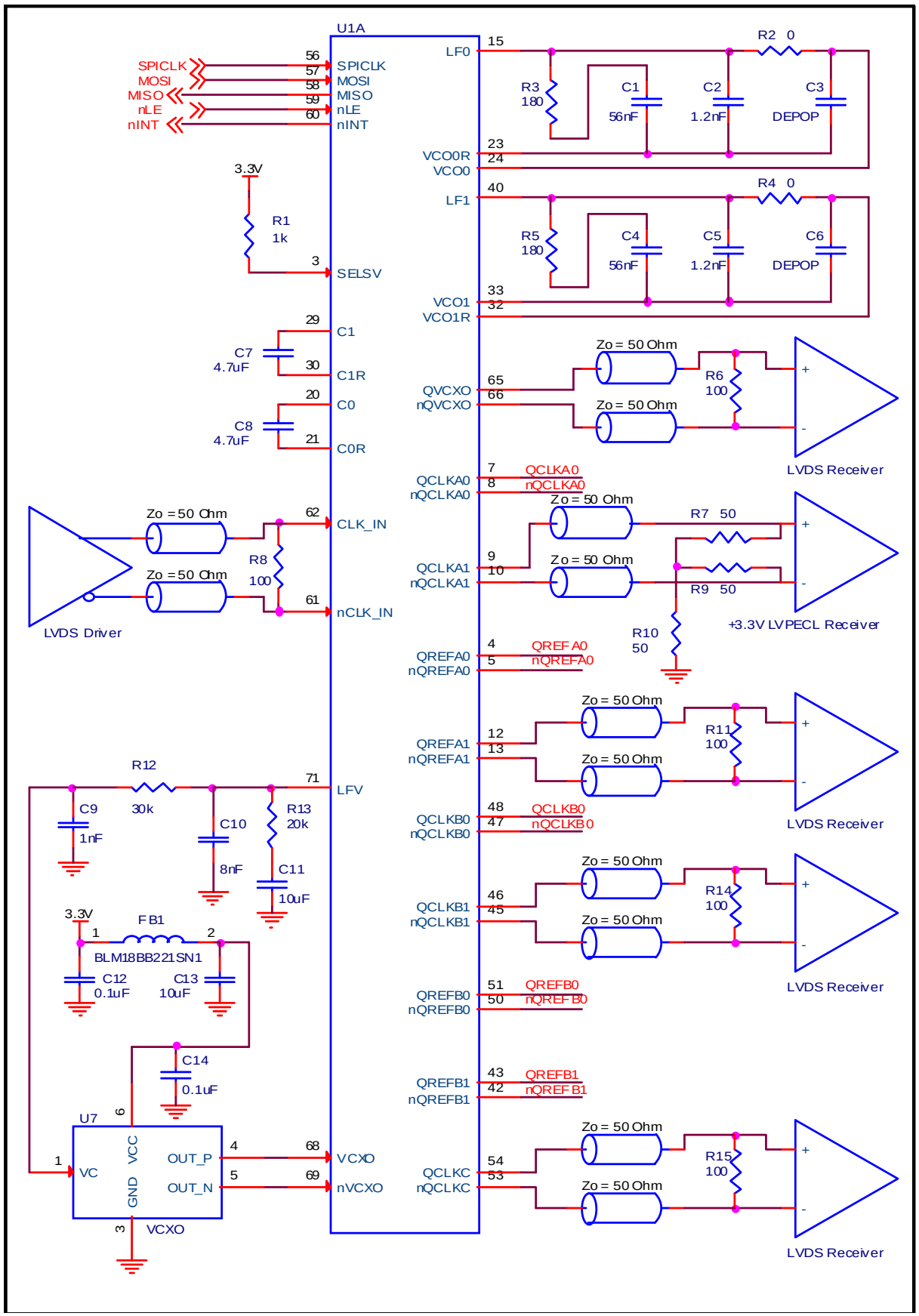


Figure 13. Signal I/O, External VCXO and Loop Filters

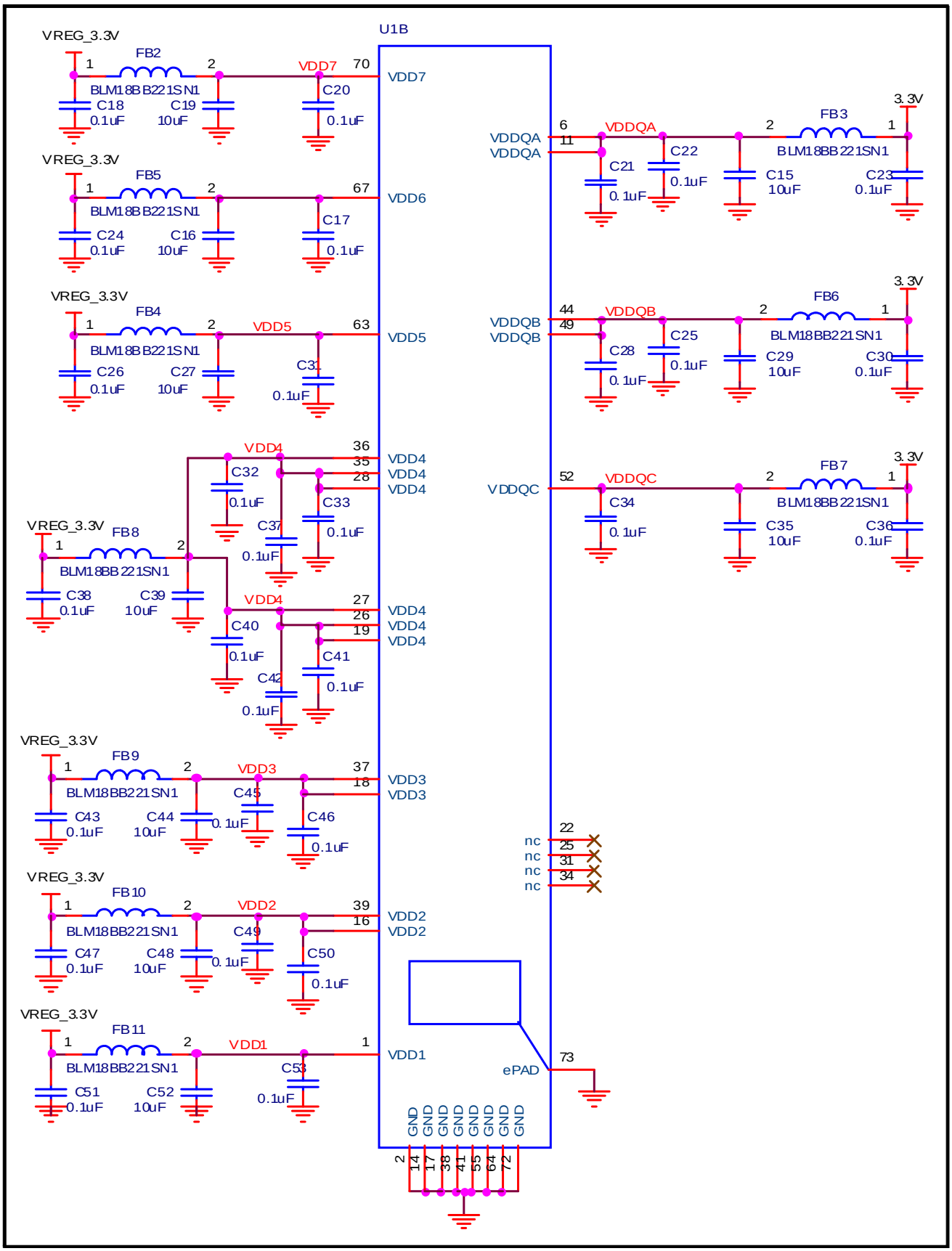


Figure 14. Power Filters

Power Considerations

The 8V19N408 device was designed and characterized to operate within the ambient extended temperature range of -40°C to 85°C.The ambient temperature represents the temperature around the device, not the junction temperature. Extreme care must be taken to avoid exceeding the 125°C junction temperature, potentially damaging the device.

Equations and example calculations are also provided below.

1. Power Dissipation.

The power dissipation for the 8V19N408 is the product of supply voltage and total I_{DD}.
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V at ambient temperature of 85°C.

Maximum current at 85°C, $I_{DD\_TOTAL\_MAX} = I_{DD\_MAX} + I_{DDQ\_MAX}$ (All QCLKx and QVCXO are running with 700mV amplitude in LVDS mode and Continuous SYSREF clocks are running with 400mV amplitude in LVDS mode)

- Total Power Dissipation: $P_D = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.465V * (370mA +620mA) = **3.430W**

2. Junction Temperature.

Junction temperature, Tj, signifies the hottest point on the device and exceeding the specified limit could cause device reliability issues. The maximum recommended junction temperature is 125°C.

For devices like this and in systems where most heat escapes from the bottom exposed pad of the package, θ_{JB} is the primary thermal resistance of interest.

The equation to calculate Tj using θ_{JB} is: $Tj = \theta_{JB} * P_D + T_B$

Tj = Junction Temperature

θ_{JB} = Junction-to-Board Thermal Resistance

P_D = Device Power Dissipation (example calculation is in section 1 above)

T_B = Board Temperature

In order to calculate junction temperature, the appropriate junction-to-board thermal resistance θ_{JB} must be used. Assuming a 2-ground plane board, the appropriate value of θ_{JB} is 0.713°C/W per Table 7 below.

Therefore, Tj for a PCB maintained at 115C° with the outputs switching is:

115°C + 3.413W * 0.713°C/W = 117.4°C which is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, heat transfer method, the type of board (multi-layer) and the actual maintained board temperature. The below table is for two ground planes. The thermal resistance will change as the number of layers in the board changes or if the board size change and other changes in other factors impacts heat dissipation in the system.

Table 7. Thermal Resistances for 72-Lead VFQFN Package

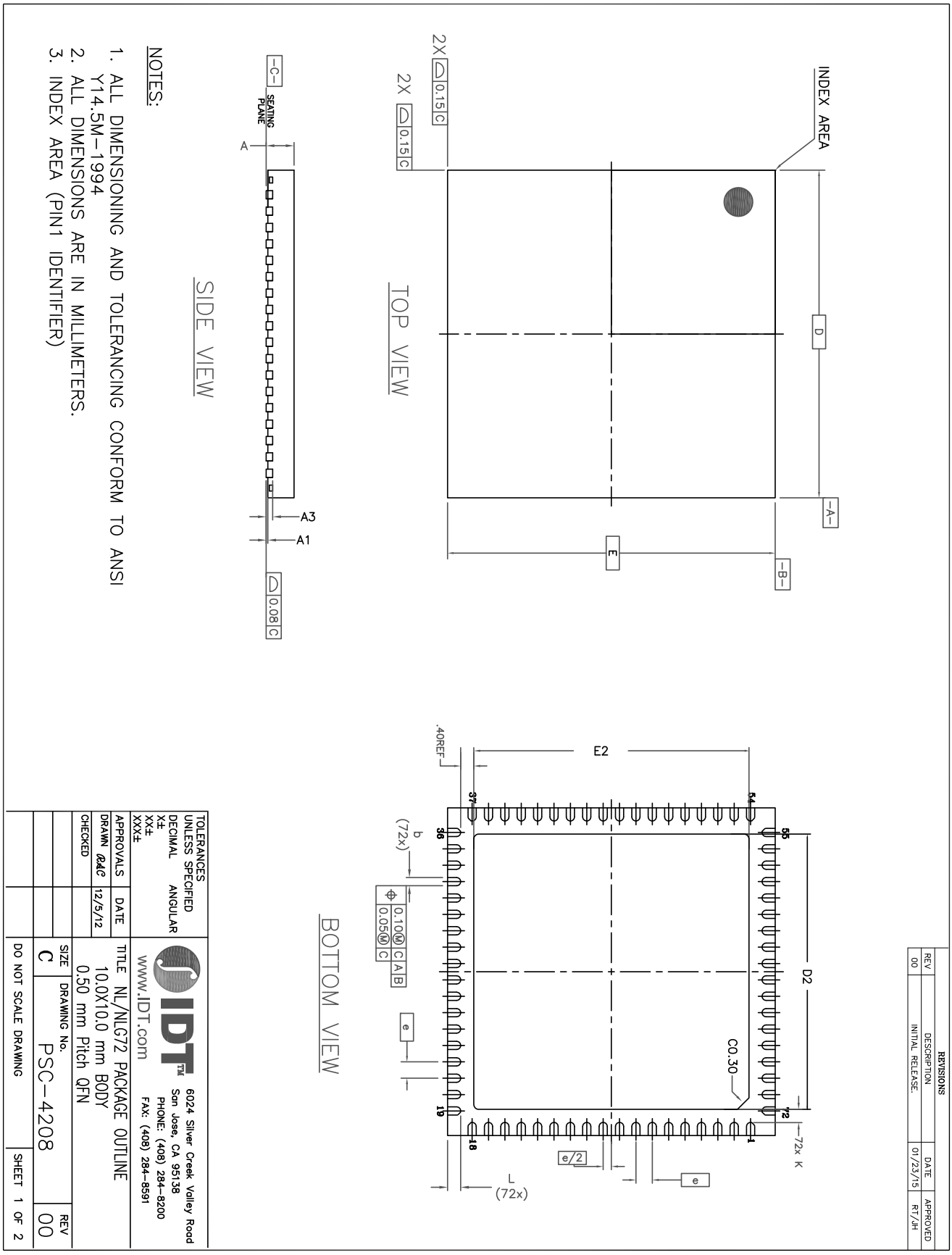
Air Flow (m/s)	0	1	2
θ_{JB}	0.713°C/W	0.713°C/W	0.713°C/W
θ_{JA}	19.16°C/W	15.49°C/W	14.14°C/W

NOTE: Applicable to PCBs with two ground planes.
NOTE: ePAD size is 8.4mm x 8.4mm and connected to ground plane in PCB through 8 x 8 Thermal Via Array.
NOTE: In devices where most of the heat exits through the bottom ePAD, θ_{JB} is commonly used for thermal calculations.

Transistor Count

The transistor count for 8V19N408 is: 52.619

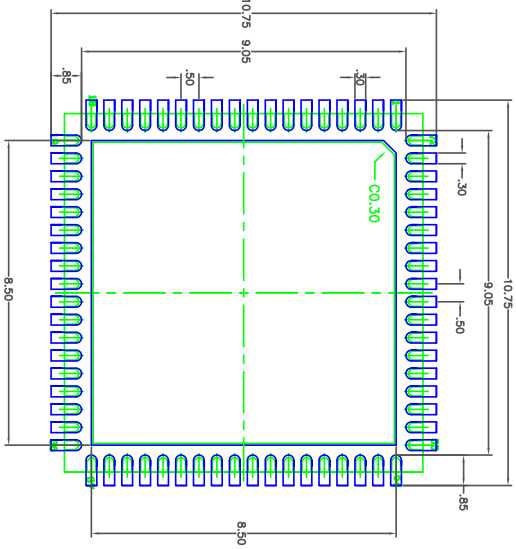
72 VFQFN Package Information



72 VFQFN Package Information, Continued

SYMBOL	DIMENSION			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0	0.02	0.05	
A3	REF	0.20 ref		
b	0.18	0.25	0.30	
e		0.50 BSC		
D2	8.30	8.40	8.50	
E2	8.30	8.40	8.50	
D		10.00 BSC		
E		10.00 BSC		
K	0.20	—	—	
L	0.30	0.40	0.50	

RECOMMENDED LAND PATTERN



EPAD 8.4 mm SQ

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE.	01/23/15	RT/JH

TOLERANCES UNLESS SPECIFIED DECIMAL XX± XXX± XXXX± ANGULAR ±	IDT™ www.IDT.com	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572	
APPROVALS DRAWN RJC 12/5/12 CHECKED	TITLE NL/NLG72 PACKAGE OUTLINE 10.0 X 10.0 mm BODY 0.50 mm Pitch QFN		
	SIZE C	DRAWING No. PSC-4208	REV 00
DO NOT SCALE DRAWING			SHEET 2 OF 2

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8V19N408ZNLGI	IDT8V9N408ZNLGI	72 Lead VFQFN, Lead-Free	Tray	-40°C to 85°C
8V19N408ZNLGI8	IDT8V9N408ZNLGI	72 Lead VFQFN, Lead-Free	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
2	Table 6A	29	AC Characteristics Table - typographical spec errors for $VO_{(pp)}$: **LVPECL Output Voltage Swing** (400mV Amplitude Setting) minimum and maximum specs; **LVPECL Differential Output Voltage Swing** (400mV Amplitude Setting) minimum, typical and maximum specs (1000mV Amplitude Setting) typical spec	10/1/15

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com

Tech Support
email: clocks@idt.com