Control Integrated POwer System (CIPOS™)

IFCM30U65GD

Datasheet

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CIPOS™

Control Integrated POwer System

Dual In-Line Intelligent Power Module
Three Phase Interleaved PFC 650V / 30A

Features

Dual In-Line molded module

- TRENCHSTOP™ 5 IGBTs
- Rapid switching emitter controlled diode
- Rugged SOI gate driver technology with stability against transient
- Over current shutdown
- Under-voltage lockout
- All of 3 switches turn off during protection
- Temperature monitor
- Emitter pins accessible for all phase current monitoring (open emitter)
- Lead-free terminal plating; RoHS compliant
- Very low thermal resistance due to DCB

Target Applications

- 3-Phase Interleaved PFC

Description

The CIPOS™ module family offers the chance for integrating various power and control components to increase reliability, optimize PCB size and system costs.

It is designed to enhance the system efficiency by improvement of power factor. The package concept is specially adapted to power applications, which need good thermal conduction and electrical isolation, but also EMI-save control and overload protection.

TRENCHSTOP™ 5 IGBTs are combined with an optimized SOI gate driver for excellent electrical performance.

System Configuration

- 3-Phase Interleaved PFC with TRENCHSTOP™ 5 IGBTs and Rapid switching emitter controlled diode
- SOI gate driver
- Thermistor
- Pin-to-heatsink clearance distance typ. 1.6mm

Pin Configuration

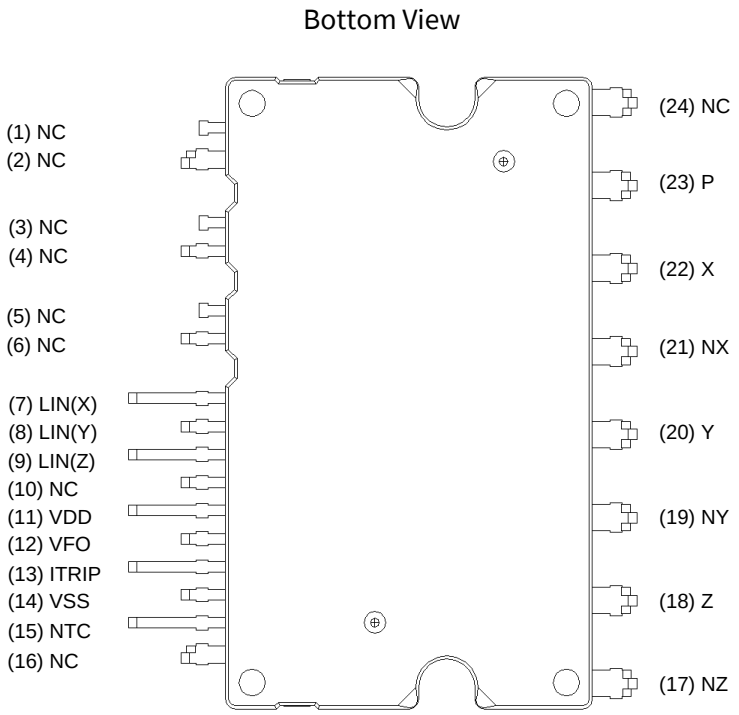


Figure 1 Pin configuration

Internal Electrical Schematic

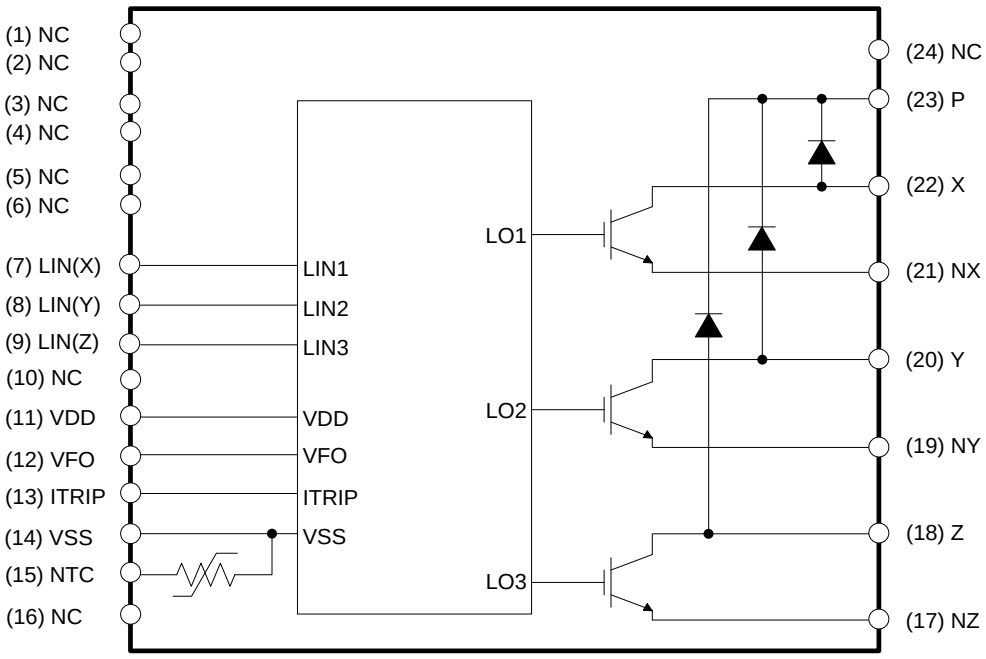


Figure 2 Internal schematic

Pin Assignment

Pin Number	Pin Name	Pin Description
1	NC	No Connection
2	NC	No Connection
3	NC	No Connection
4	NC	No Connection
5	NC	No Connection
6	NC	No Connection
7	LIN(X)	X phase IGBT gate driver input
8	LIN(Y)	Y phase IGBT gate driver input
9	LIN(Z)	Z phase IGBT gate driver input
10	NC	No Connection
11	VDD	Control supply
12	VFO	Fault output
13	ITRIP	Over current shutdown input
14	VSS	Control negative supply
15	NTC	Thermistor
16	NC	No Connection
17	NZ	Z phase IGBT emitter
18	Z	Z phase IGBT collector
19	NY	Y phase IGBT emitter
20	Y	Y phase IGBT collector
21	NX	X phase IGBT emitter
22	X	X phase IGBT collector
23	P	Positive output voltage
24	NC	No Connection

Pin Description

LIN(X, Y, Z) (IGBT control pins, Pin 7, 8, 9)

These pins are positive logic and they are responsible for the control of the integrated IGBT. The Schmitt-trigger input thresholds of them are such to guarantee LSTTL and CMOS compatibility down to 3.3V controller outputs. Pull-down resistor of about 5kΩ is internally provided to pre-bias inputs during supply start-up and a zener clamp is provided for pin protection purposes. Input Schmitt-trigger and noise filter provide beneficial noise rejection to short input pulses.

The noise filter suppresses control pulses which are below the filter time t_{FILIN}. The filter acts according to Figure 4.

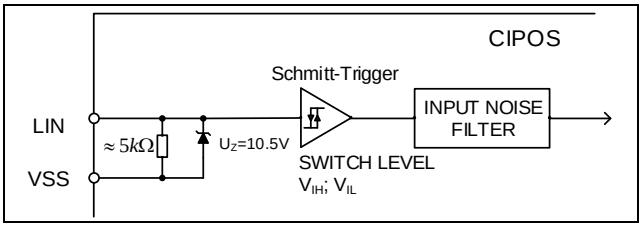


Figure 3 Input pin structure

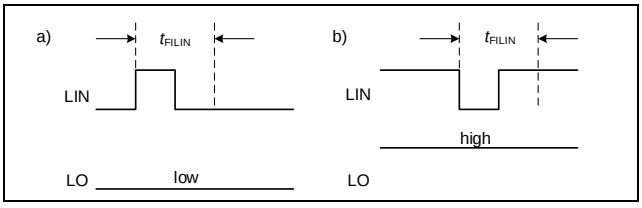


Figure 4 Input filter timing diagram

It is recommended for proper work of this product not to provide input pulse-width lower than 0.5us.

VFO (Fault-output, Pin 12)

The VFO pin indicates a module failure in case of under voltage at pin VDD or in case of triggered over current detection at ITRIP.

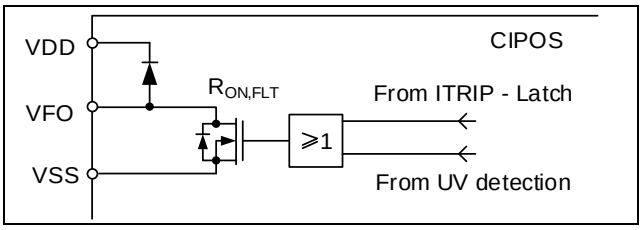


Figure 5 Internal circuit at pin VFO

NTC (Thermistor, Pin 15)

The NTC pin provides direct access to thermistor, which is referenced to VSS. An external pull-up resistor connected to +5V ensures that the resulting voltage can be directly connected to the microcontroller.

ITRIP (Over current detection function, Pin 13)

CIPOS™ provides an over current detection function by connecting the ITRIP input with the IGBT collector current feedback. The ITRIP comparator threshold (typ. 0.47V) is referenced to VSS ground. An input noise filter (typ.: $t_{ITRIPMIN}$ = 530ns) prevents the driver to detect false over-current events.

Over current detection generates a shutdown of all outputs of the gate driver after the shutdown propagation delay of typically 1000ns.

VDD, VSS (Control supply and reference, Pin 11, 14)

VDD is the control supply and it provides power both to input logic and to output power stage. Input logic is referenced to VSS ground.

The under-voltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of VDD_{UV+} = 12.1V is present.

The IC shuts down all the gate drivers power outputs, when the VDD supply voltage is below VDD_{UV-} = 10.4V. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

NX, NY, NZ (IGBT emitter, Pin 17, 19, 21)

The IGBT emitters are available for current measurements of each phase. It is recommended to keep the connection to pin VSS as short as possible in order to avoid unnecessary inductive voltage drops.

X, Y, Z (IGBT collector, Pin 18, 20, 22)

These pins are IGBT collector. It is mandatory to connect anti-parallel diode between IGBT collector and emitter.

P (Positive output voltage, Pin 23)

The diode cathodes are connected to the output voltage. It is noted that the voltage does not exceed 450 V.

Absolute Maximum Ratings

(V_{DD} = 15V and T_j = 25°C, if not stated otherwise)

Module Section

Description	Condition	Symbol	Value		Unit
			min	max	
Storage temperature range		T_{stg}	-40	125	°C
Isolation test voltage	RMS, f=60Hz, t=1min	V_{ISOL}	2000	-	V
Operating case temperature range	Refer to Figure 6	T_C	-40	100	°C

Power Section

Description	Condition	Symbol	Value		Unit
			min	max	
DC link output voltage of P-N	Applied between P-N	V_{PN}	-	450	V
DC link output voltage (surge) of P-N	Applied between P-N	$V_{PN(surge)}$	-	500	V
Max. blocking voltage	I_C = 250µA	V_{CES}	650	-	V
Repetitive peak reverse voltage	I_R = 250µA	V_{RRM}	650	-	V
Input RMS current of each phase	$T_J \leq 150°C$, $T_C = 25°C$ $T_C = 80°C$	I_i	- -	30 20	A
Maximum peak input current of each phase	$T_J \leq 150°C$, $T_C = 25°C$ less than 1ms, non-repetitive	$I_{i(peak)}$	-	80	A
Power dissipation of each IGBT		P_{tot}	-	60.4	W
Operating junction temperature range		T_J	-40	150	°C
Single IGBT thermal resistance, junction-case		R_{thJC}	-	2.07	K/W
Single diode thermal resistance, junction-case		R_{thJCD}	-	2.77	K/W

Control Section

Description	Condition	Symbol	Value		Unit
			min	max	
Module supply voltage		V_{DD}	-1	20	V
Input voltage	LIN, ITRIP	V_{IN} V_{ITRIP}	-1 -1	10	V
Switching frequency		f_{PWM}	-	60	kHz

Recommended Operation Conditions

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified.

Description	Symbol	Value			Unit
		min	typ	max	
DC link output voltage of P-N	V_{PN}	0	-	450	V
Control supply voltage	V_{DD}	13.5	15	16.5	V
Control supply variation	ΔV_{DD}	-1	-	1	V/µs
Logic input voltages LIN,ITRIP	V_{IN} V_{ITRIP}	0 0	-	5 5	V
Between VSS - N (including surge)	V_{SS}	-5	-	5	V

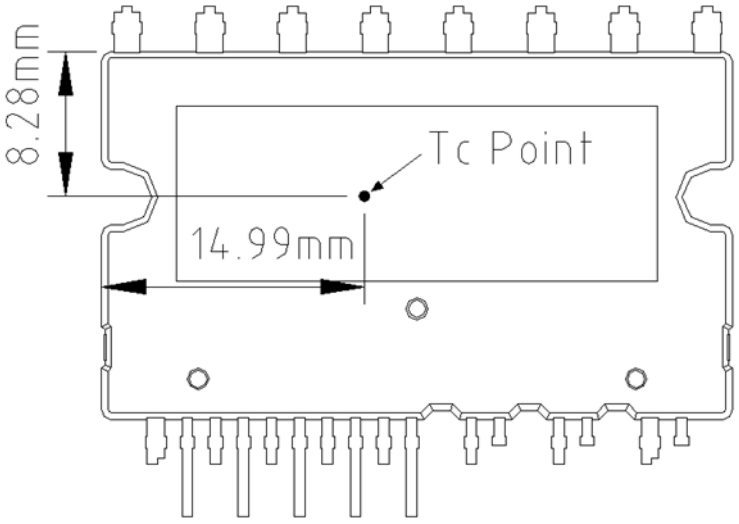


Figure 6 T_C measurement point[1]

[1]Any measurement except for the specified point in figure 6 is not relevant for the temperature verification and brings wrong or different information.

Static Parameters

(V_{DD} = 15V and T_j = 25°C, if not stated otherwise)

Description	Condition	Symbol	Value			Unit
			min	typ	max	
Collector-Emitter saturation voltage	I_C = 20A T_J = 25°C 150°C	$V_{CE(sat)}$	- -	1.75 1.95	2.3 -	V
Diode forward voltage	I_F = 20A T_J = 25°C 150°C	V_F	- -	1.45 1.4	2.0 -	V
Collector-Emitter leakage current	V_{CE} = 650V	I_{CES}	-	-	1	mA
Diode reverse leakage current	V_R = 650V	I_R	-	-	1	mA
Logic "1" input voltage (LIN)		V_{IH}	-	2.1	2.5	V
Logic "0" input voltage (LIN)		V_{IL}	0.7	0.9	-	V
ITRIP positive going threshold		$V_{IT,TH+}$	400	470	540	mV
ITRIP input hysteresis		$V_{IT,HYS}$	40	70	-	mV
VDD supply under voltage positive going threshold		VDD_{UV+}	10.8	12.1	13.0	V
VDD supply under voltage negative going threshold		VDD_{UV-}	9.5	10.4	11.2	V
VDD supply under voltage lockout hysteresis		VDD_{UVH}	1.0	1.7	-	V
Quiescent VDD supply current	L_{IN} = 0V	I_{QDD}	-	370	900	µA
Input bias current	V_{IN} = 5V	I_{IN+}	-	1	1.5	mA
Input bias current	V_{IN} = 0V	I_{IN-}	-	2	-	µA
ITRIP input bias current	V_{ITRIP} = 5V	I_{ITRIP+}	-	65	150	µA
VFO input bias current	VFO = 5V, V_{ITRIP} = 0V	I_{FO}	-	2	-	nA
VFO output voltage	I_{FO} = 10mA, V_{ITRIP} = 1V	V_{FO}	-	0.5	-	V

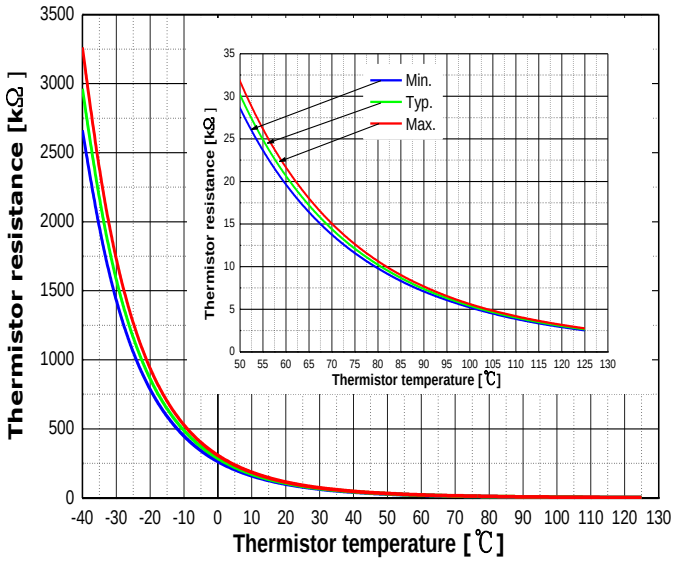
Dynamic Parameters

(V_{DD} = 15V and T_j = 25°C, if not stated otherwise)

Description	Condition	Symbol	Value			Unit
			min	typ	max	
Turn-on propagation delay time	V_{LIN} = 5V, I_C = 20A, V_{DC} = 400V	t_{on}	-	610	-	ns
Turn-on rise time		t_r	-	25	-	ns
Turn-on switching time		$t_{c(on)}$	-	115	-	ns
Reverse recovery time		t_{rr}	-	90	-	ns
Turn-off propagation delay time	V_{LIN} = 0V, I_C = 20A, V_{DC} = 400V	t_{off}	-	700	-	ns
Turn-off fall time		t_f	-	15	-	ns
Turn-off switching time		$t_{c(off)}$	-	30	-	ns
Input filter time ITRIP	V_{ITRIP} = 1V	$t_{ITRIPmin}$	-	530	-	ns
Input filter time at LIN for turn on and off	V_{LIN} = 0V & 5V	t_{FILIN}	-	290	-	ns
Fault clear time after ITRIP-fault	V_{ITRIP} = 1V	t_{FLTCLR}	40	-	-	µs
IGBT turn-on energy (includes reverse recovery of diode)	V_{DC} = 400V, I_C = 20A T_J = 25°C 150°C	E_{on}	- -	550 705	- -	µJ
IGBT turn-off energy	V_{DC} = 400V, I_C = 20A T_J = 25°C 150°C	E_{off}	- -	95 125	- -	µJ
Diode recovery energy	V_{DC} = 400V, I_C = 20A T_J = 25°C 150°C	E_{rec}	- -	80 120	- -	µJ

Thermistor

Description	Condition	Symbol	Value			Unit
			min	typ	max	
Resistor	T_{NTC} = 25°C	R_{NTC}	-	85	-	kΩ
B-constant of NTC (Negative Temperature Coefficient)		B(25/100)	-	4092	-	K



T [°C]	Rmin. [kΩ]	Rtyp. [kΩ]	Rmax. [kΩ]
50	28.400	29.972	31.545
60	19.517	20.515	21.514
70	13.670	14.315	14.960
80	9.745	10.169	10.593
90	7.062	7.345	7.628
100	5.199	5.388	5.576
110	3.856	4.009	4.163
120	2.900	3.024	3.149
125	2.527	2.639	2.751

Figure 7 Thermistor resistance – temperature curve and table

(For more information, please refer to the application note 'AN CIPOS™-Mini 1 Technical description')

Mechanical Characteristics and Ratings

Description	Condition	Value			Unit
		min	typ	max	
Mounting torque	M3 screw and washer	0.49	-	0.78	Nm
Flatness	Refer to Figure 8	-50	-	100	µm
Weight		-	6.58	-	g

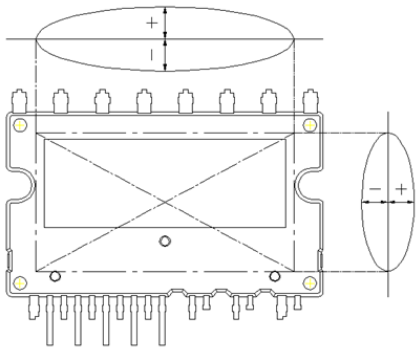


Figure 8 Flatness measurement position

Circuit of a Typical Application

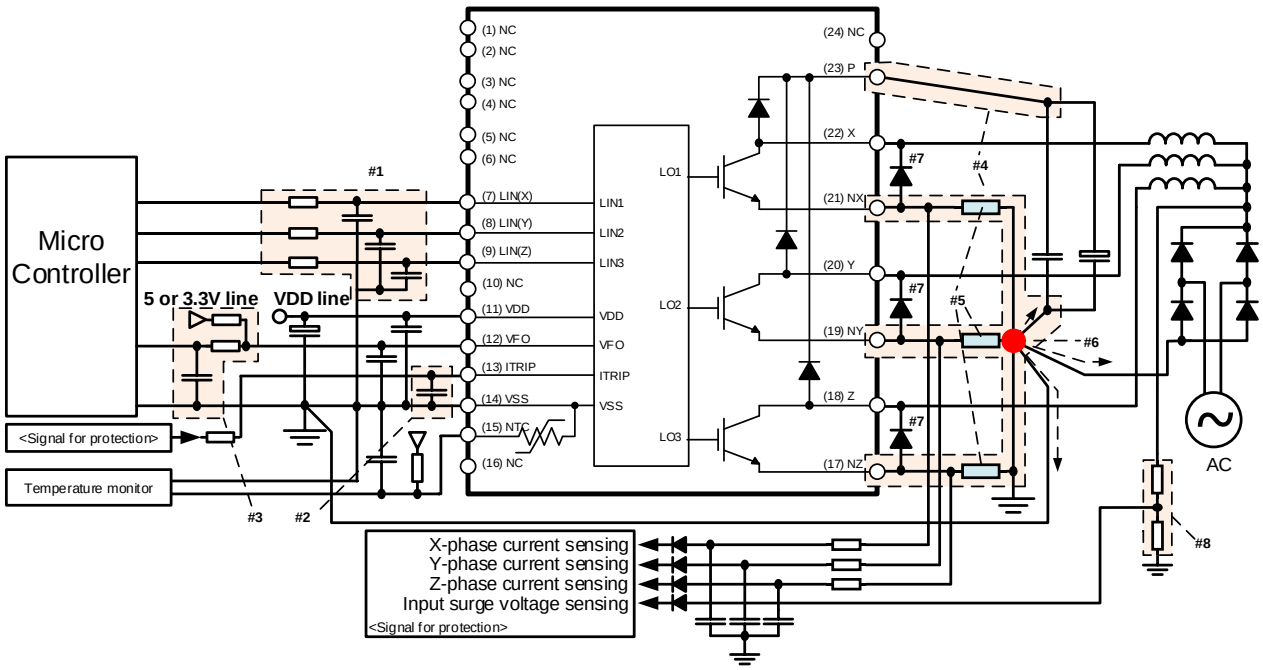


Figure 9 Typical application circuit

Because CIPOS™ Mini PFC has very high speed switching characteristics, considerable large surge voltage between P and N terminals and switching noise on signaling path are generated easily. Please pay attention to the below items for optimized application circuit design.

1. Input circuit

- To reduce input signal noise by high speed switching, the R_{IN} and C_{IN} filter circuit should be mounted. (100Ω, 1nF)

- C_{IN} should be placed as close to V_{SS} pin as possible.

2. Itrip circuit

- To prevent protection function errors, C_{ITRIP} should be placed as close to Itrip and V_{SS} pins as possible.

3. VFO circuit

- VFO output is an open drain output. This signal line should be pulled up to the positive side of the 5V/3.3V logic power supply with a proper resistor R_{PU}. It is recommended that RC filter be placed as close to the controller as possible.

4. Snubber capacitor

- The wiring between CIPOS™ Mini PFC and snubber capacitor including shunt resistor should be as short as possible.

5. Shunt resistor

- The shunt resistor of SMD type should be used for reducing its stray inductance.

6. Ground pattern

- Ground pattern should be separated at only one point of shunt resistor as short as possible.

7. It is mandatory to connect anti-parallel diode (2A, voltage rating higher than 650V) to PFC IGBT.

8. Input surge voltage protection circuit

- This protection circuit is necessary for PFC IGBT to be protected from excessive surge voltage.

Switching Times Definition

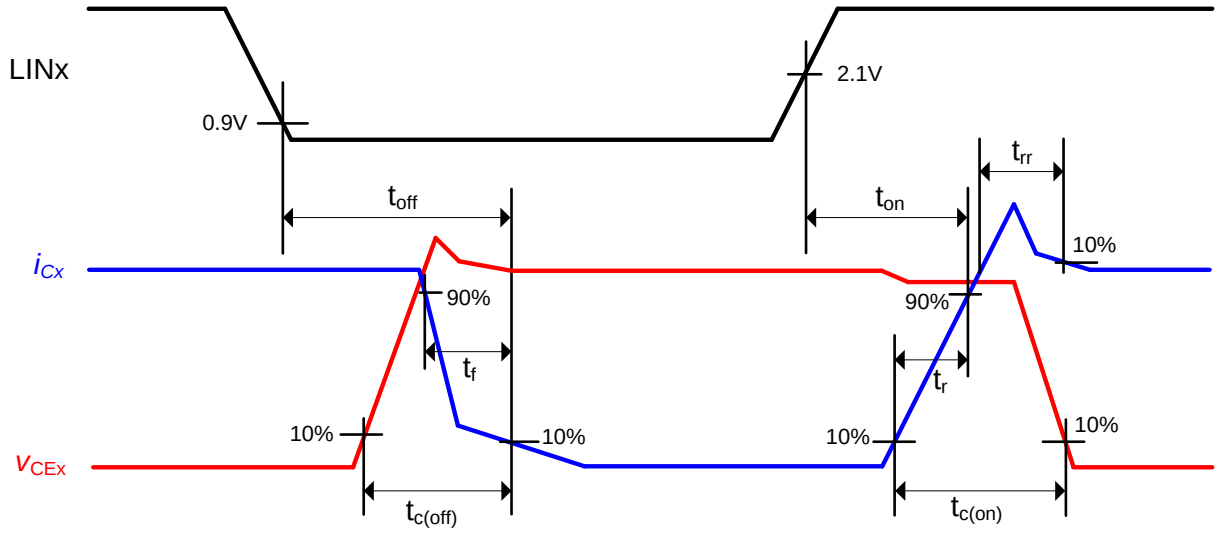
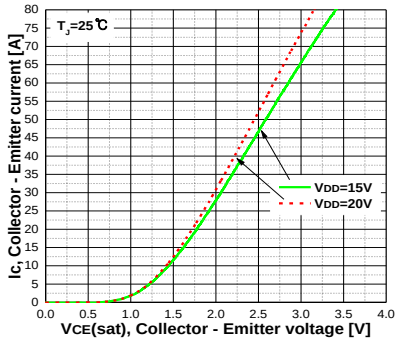
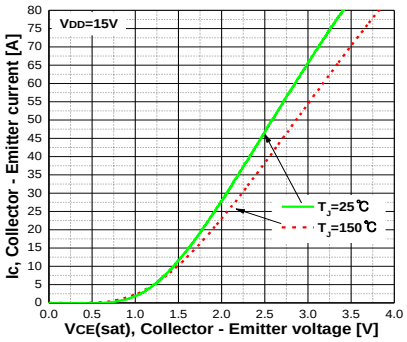


Figure 10 Switching times definition

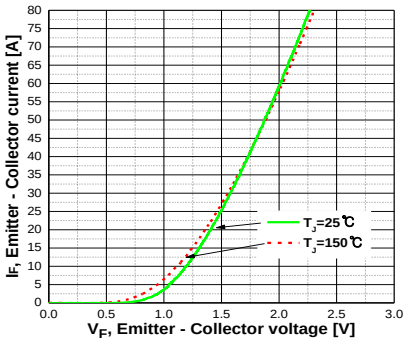
Electrical characteristic



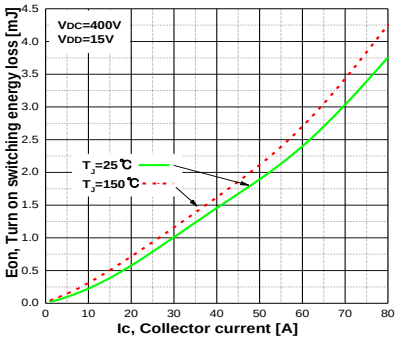
Typ. Collector – Emitter saturation voltage



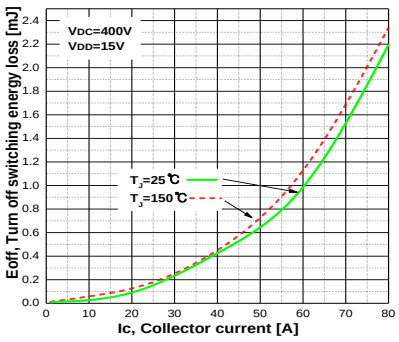
Typ. Collector – Emitter saturation voltage



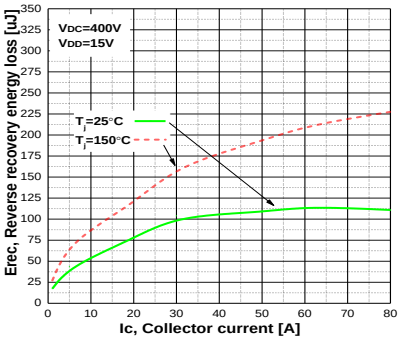
Typ. Emitter – Collector forward voltage



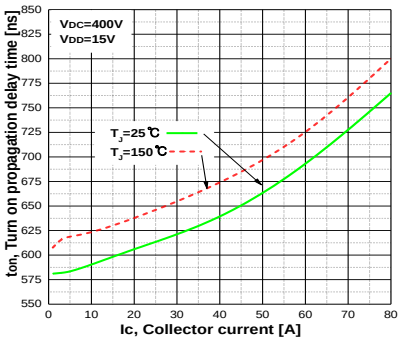
Typ. Turn on switching energy loss



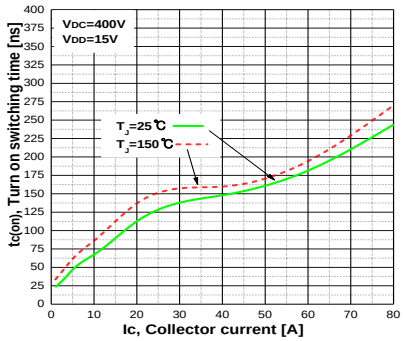
Typ. Turn off switching energy loss



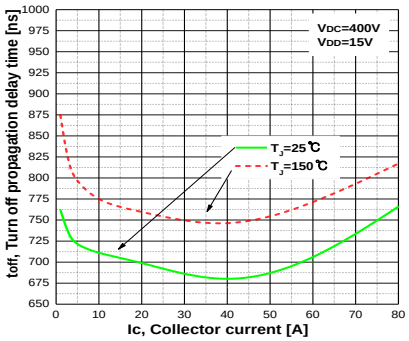
Typ. Reverse recovery energy loss



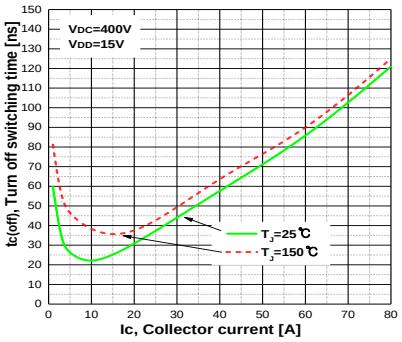
Typ. Turn on propagation delay time



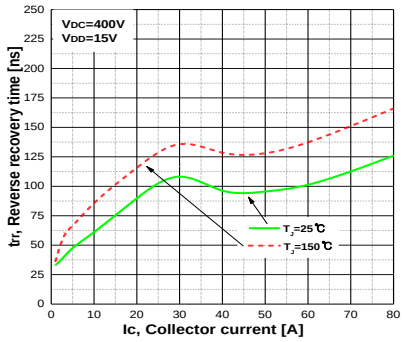
Typ. Turn on switching time



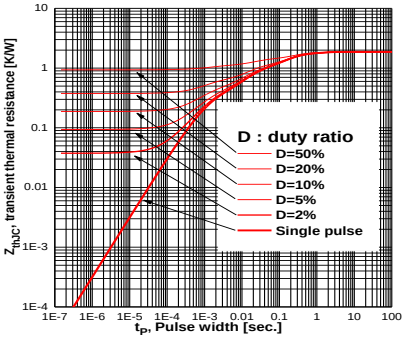
Typ. Turn off propagation delay time



Typ. Turn off switching time

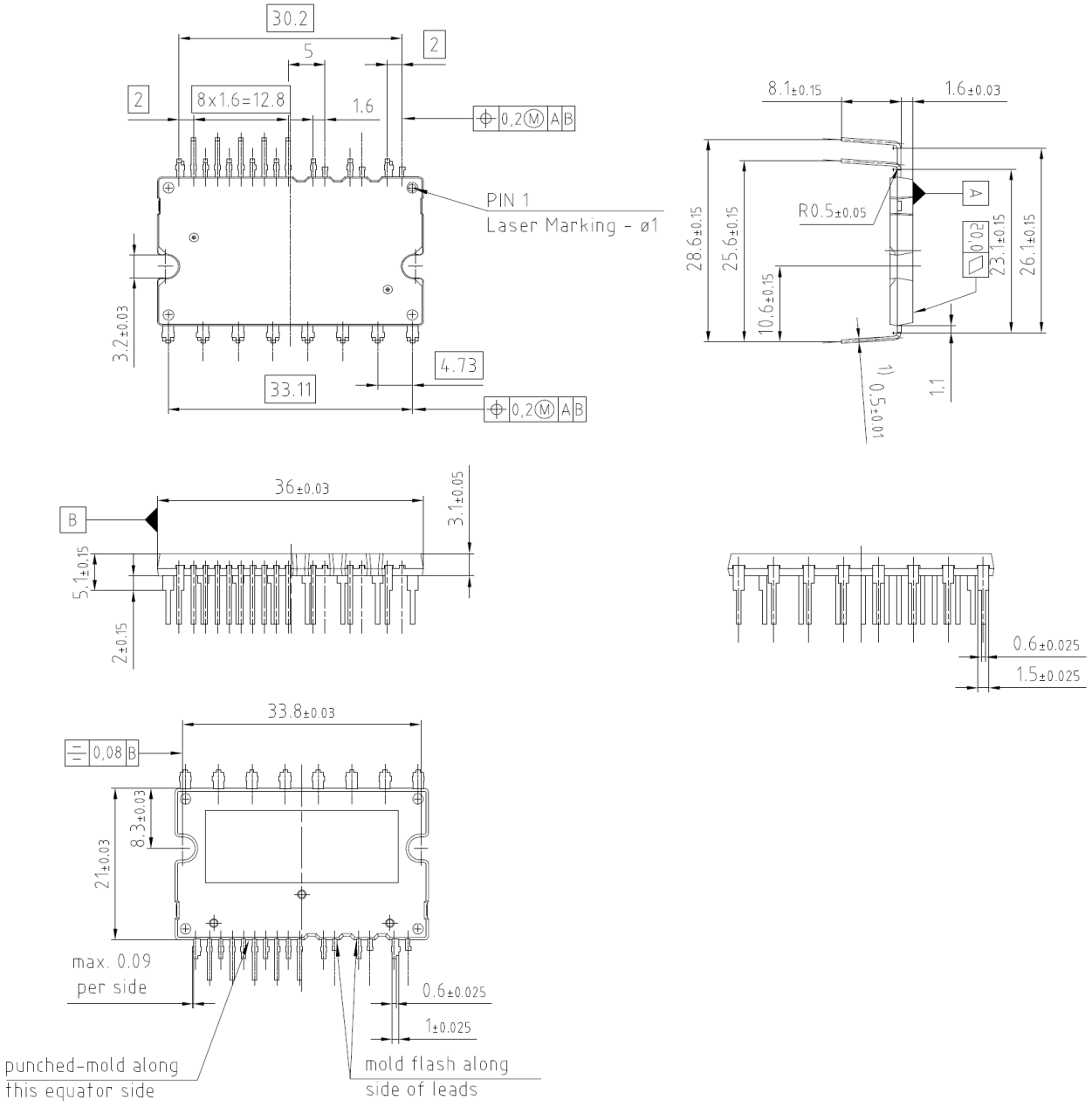


Typ. Reverse recovery time



IGBT transient thermal resistance
at all IGBTs operation

Package Outline



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