

Evaluation Board for the **AD5273** Digital Potentiometer

FEATURES

- Full-featured in conjunction with low voltage digiPOT motherboard (EVAL-MB-LV-SDZ)
- Various test circuits
- Various ac/dc input signals
- PC control via a separately purchased system demonstration platform (SDP-B or SDP-S)
- PC software for control

PACKAGE CONTENTS

- EVAL-AD5273DBZ** board
- EVAL-MB-LV-SDZ motherboard
- CD that includes
 - Self-installing software that allows users to control the board and exercise all functions of the device
 - Electronic version of the **AD5273** data sheet
 - Electronic version of the UG-395 user guide

GENERAL DESCRIPTION

This user guide describes the evaluation board for evaluating the **AD5273**, a single channel, 64-position, one-time programmable (OTP) memory digital potentiometer that employ fuse link technology to achieve memory retention of resistance settings. The on-board socket allows the user to easily replace the device for reprogramming of the OTP memory. The **AD5273** supports single-supply 2.7 V to 5.5 V operation, making the device suited for battery-powered applications and many other applications with superior low temperature coefficient performance. In addition, the **AD5273** uses a versatile I²C serial interface that operates in fast mode, allowing speeds of up to 400 kHz. The EVAL-MB-LV-SDZ can operate in single-supply mode and incorporates an internal power supply from the USB. Complete specifications for the **AD5273** part can be found in the **AD5273** data sheet, which is available from Analog Devices, Inc., and should be consulted in conjunction with this user guide when using the evaluation board.

EVAL-AD5273DBZ WITH MOTHERBOARD AND SDP-B



Figure 1. Digital Picture of Evaluation Board with Low Voltage DigiPOT Motherboard and System Demonstration Platform

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REVISION HISTORY

5/12—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The EVAL-MB-LV-SDZ supports using single power supplies.

The evaluation board can be powered either from the SDP port or externally by the J1 and J2 connectors, as described in Table 1.

All supplies are decoupled to ground using 10 μ F tantalum and 0.1 μ F ceramic capacitors.

Table 1. Maximum and Minimum Voltages of the Connectors

Connector No.	Label	Voltage
J1-1	EXT VDD	Analog positive power supply, V_{DD} ; from 2.7 V to 5.5 V
J1-2	GND	Analog ground
J2-1	VLOGIC	Digital supply, from 2.7 V to V_{DD}
J2-2	DGND	Digital ground

Table 3. Link Functions

Link No.	Power Supply	Options
A11	V_{DD}	This link selects one of the following as the positive power supply: 5 V (from SDP). 3.3 V (from SDP). EXT VDD (external supply from the J1 connector).
A5	V_{LOGIC}	This link selects one of the following as the digital supply: 3.3 V (from SDP). VLOGIC (external supply from the J2 connector).
A12	GND	AGND.

Link Options

Several link and switch options are incorporated in the EVAL-MB-LV-SDZ board and should be set up before using the board. Table 2 describes the positions of the links to control the evaluation board by a PC, via the SDP board. The functions of these link options are described in detail in Table 3 through Table 6.

Table 2. Link Options Setup for SDP Control (Default)

Link No.	Option
A11	3.3 V
A12	AGND
A5	3.3 V

TEST CIRCUITS

The EVAL-AD5273DBZ and EVAL-MB-LV-SDZ incorporate several test circuits to evaluate the performance of the AD5273.

DAC

The RDAC can be operated as a digital-to-analog converter (DAC), as shown in Figure 2.

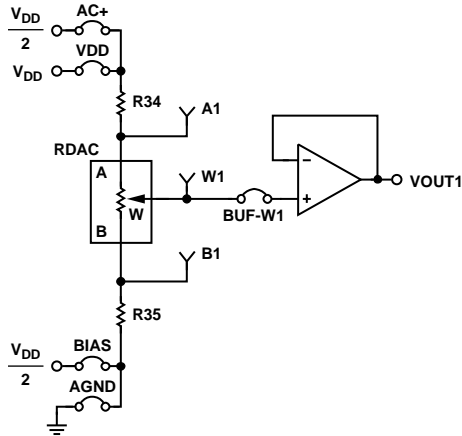


Figure 2. DAC

Table 5 shows the options available for the voltage references. The output voltage is defined in Equation 1.

$$V_{OUT} = (V_A - V_B) \times \frac{RDAC}{64} \tag{1}$$

where:

RDAC is the code loaded in the RDAC register.
 V_A is the voltage applied to the A terminal (A9 link).
 V_B is the voltage applied to the B terminal (A10 link).

However, by using the R34 and R35 external resistors, the user can reduce the voltage of the voltage references. In this case, use the A1 and B1 test points to measure the voltage applied to the A and B terminals and recalculate V_A and V_B in Equation 1.

AC Signal Attenuation

The RDAC can be used to attenuate an ac signal, which must be provided externally using the AC_INPUT connector, as shown in Figure 3.

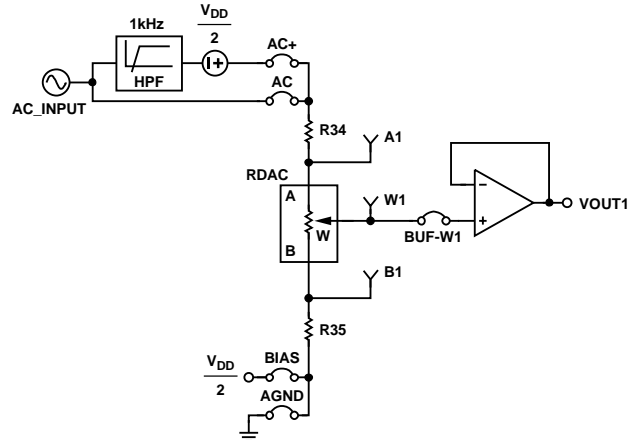


Figure 3. AC Signal Attenuator

Depending on the voltage supply rails and the dc offset voltage of the ac signal, various configurations can be used as described in Table 4.

Table 4. AC Signal Attenuation Link Options

Link	Options	Conditions
A9	AC+	No dc offset voltage. AC signal is outside the voltage supply rails due to the dc offset voltage. DC offset voltage ≠ V _{DD} /2 ¹ .
	AC	All other conditions.
A10	BIAS AGND	Use in conjunction with AC+ link ¹ . All other conditions.

¹ Recommended to ensure optimal total harmonic distortion (THD) performance.

The signal attenuation is defined in Equation 2.

$$Attenuation \text{ (dB)} = 20 \times \log \left(\frac{R_{WB} + R_W}{R_{END-TO-END}} \right) \tag{2}$$

where:

R_{WB} is the resistor between the W and B terminals.
 R_W is the wiper resistance.
 R_{END-TO-END} is the end-to-end resistance value.

Table 5. DAC Voltage References

Terminal	Link (Daughter Board)	Link (Motherboard)	Options	Description
A1	Switch B of A4	A9	AC+ VDD	Connects Terminal A1 to V _{DD} /2 Connects Terminal A1 to V _{DD}
W1	Switch B of A3	BUF-W1		Connects Terminal W1 to an output buffer
B1	Switch B of A2	A10	BIAS AGND	Connects Terminal B1 to V _{DD} /2 Connects Terminal B1 to analog ground
	A1 inserted			Closes feedback loop of second op amp in AD8618

Signal Amplifier

The RDAC can be operated as an inverting or noninverting signal amplifier supporting linear or pseudologarithmic gains. Table 6 shows the available configurations.

The noninverting amplifier with linear gain is shown in Figure 4, and the gain is defined in Equation 3.

$$G = 1 + \frac{R_{WB}}{R_{38}} \tag{3}$$

where R_{WB} is the resistor between the W and B terminals.

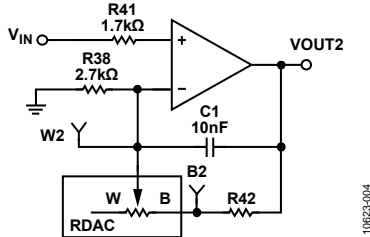


Figure 4. Linear Noninverting Amplifier

The noninverting amplifier with pseudologarithmic gain is shown in Figure 5, and the gain is defined in Equation 4.

$$G = 1 + \frac{R_{WB}}{R_{AW}} \tag{4}$$

where:

R_{WB} is the resistor between the W and B terminals.

R_{AW} is the resistor between the A and W terminals.

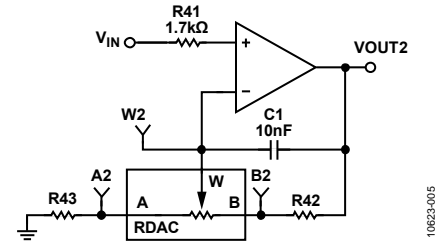


Figure 5. Pseudologarithmic Noninverting Amplifier

R_{43} and R_{42} can be used to set the maximum and minimum gain limits.

The inverting amplifier with linear gain is shown in Figure 6, and the gain is defined in Equation 5.

Note that the input signal, V_{IN} , must be negative.

$$G = -\frac{R_{WB}}{R_{38}} \tag{5}$$

where R_{WB} is the resistor between the W and B terminals.

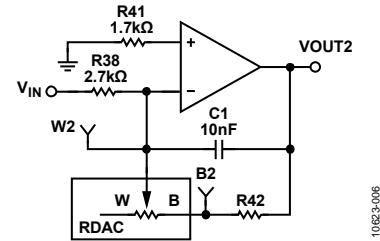


Figure 6. Linear Inverting Amplifier

Table 6. Amplifier Selection Link Options

Amplifier	Gain	Link (Daughter Board)	Link (Motherboard)	Label	V_{IN} Range	
Noninverting	Linear	Switch A of A2, A3, and A4	A7	LIN	0 V to V_{DD}	
		A1 not inserted	A6 A8	N-INV N-INV		
	Pseudologarithmic	Switch A of A2, A3, and A4	A7	LOC		0 V to V_{DD}
		A1 not inserted	A6 A8	N-INV N-INV		
Inverting	Linear	Switch A of A2, A3, and A4	A7	LIN	$-V_{DD}$ to 0 V	
		A1 not inserted	A6	INV		
			A8	INV		

EVALUATION BOARD SOFTWARE

INSTALLING THE SOFTWARE

The [EVAL-AD5273DBZ](#) kit includes evaluation board software provided on a CD. The software is compatible with Windows® XP, Windows Vista, and Windows 7 (both 32 bits and 64 bits).

Install the software before connecting the [SDP board](#) to the USB port of the PC to ensure that the SDP board is recognized when it is connected to the PC.

1. Start the Windows operating system and insert the CD.
2. The installation software opens automatically. If it does not, run the **setup.exe** file from the CD.
3. After installation is completed, power up the evaluation board as described in the Power Supplies section.
4. Connect the [EVAL-AD5273DBZ](#) and EVAL-MB-LV-SDZ to the SDP board and the SDP board to the PC using the USB cable included in the evaluation kit.
5. When the software detects the evaluation board, follow the instructions that appear to finalize the installation.

RUNNING THE SOFTWARE

To run the program, do the following:

1. Click **Start > All Programs > Analog Devices > AD5273 > AD5273 Eval Board**. To uninstall the program, click **Start > Control Panel > Add or Remove Programs > AD5273 Eval Board**.

2. If the SDP board is not connected to the USB port when the software is launched, a connectivity error displays (see Figure 7). Simply connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and follow the instructions.

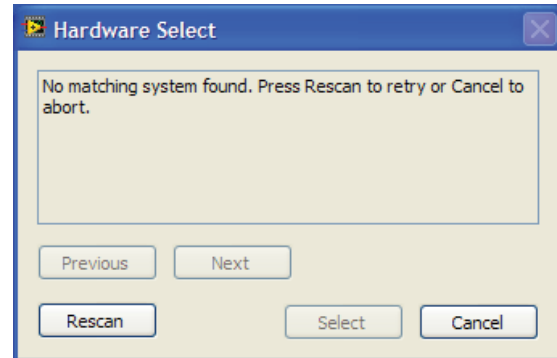


Figure 7. Pop-Up Window Error

The main window of the [EVAL-AD5273DBZ](#) software then opens, as shown in Figure 8.

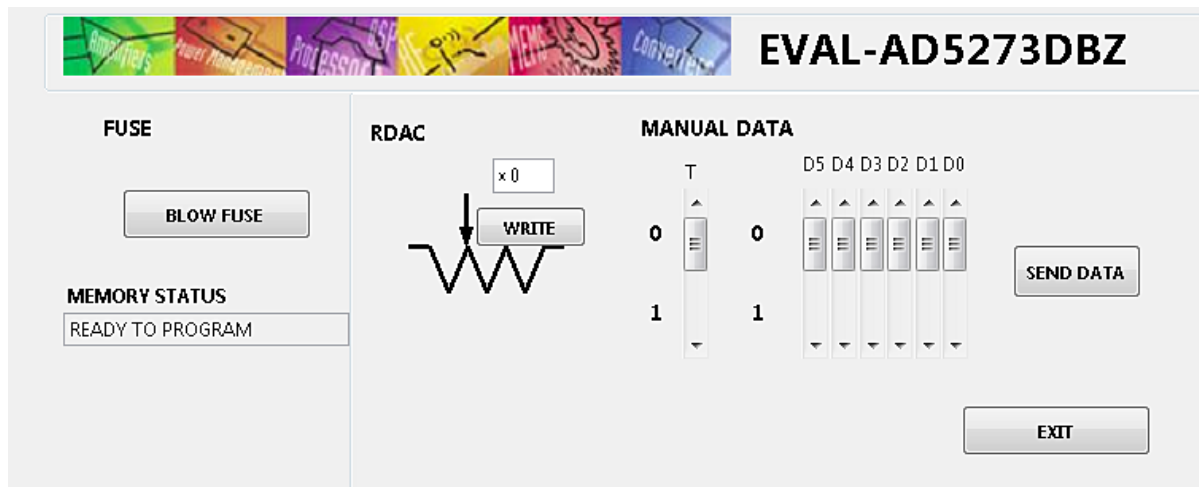


Figure 8. EVAL-AD5273DBZ Software Main Window

SOFTWARE OPERATION

The main window of the [EVAL-AD5273DBZ](#) software is divided into the following sections: **FUSE**, **RDAC**, and **MANUAL DATA**.

FUSE has the following options:

- **BLOW FUSE** allows you to program the fuses. The A11 link must be connected to 5 V. If the board is operated at a different supply, close the program, change the link, and rerun the software. Due to the supply voltage limitations of the SDP board, the logic digital levels operate below a recommended value (2.5 V), and proper communication is not guaranteed.
- **MEMORY STATUS** shows the fuse status.

RDAC has the following option:

- Enter a desired value into the text box to update the RDAC registers and click **WRITE**. When **WRITE** is clicked, a write/read operation is performed, and the value displayed in this section is updated with the actual RDAC register value. This function can be used to verify whether the write operation was completed successfully.

MANUAL DATA has the following option:

- A customized I²C data-word can be sent by manually switching the scroll bars from 0 to 1 or from 1 to 0 as desired and then clicking **SEND DATA**.

EXIT closes the program.

EVALUATION BOARD SCHEMATICS AND ARTWORK

MOTHERBOARD

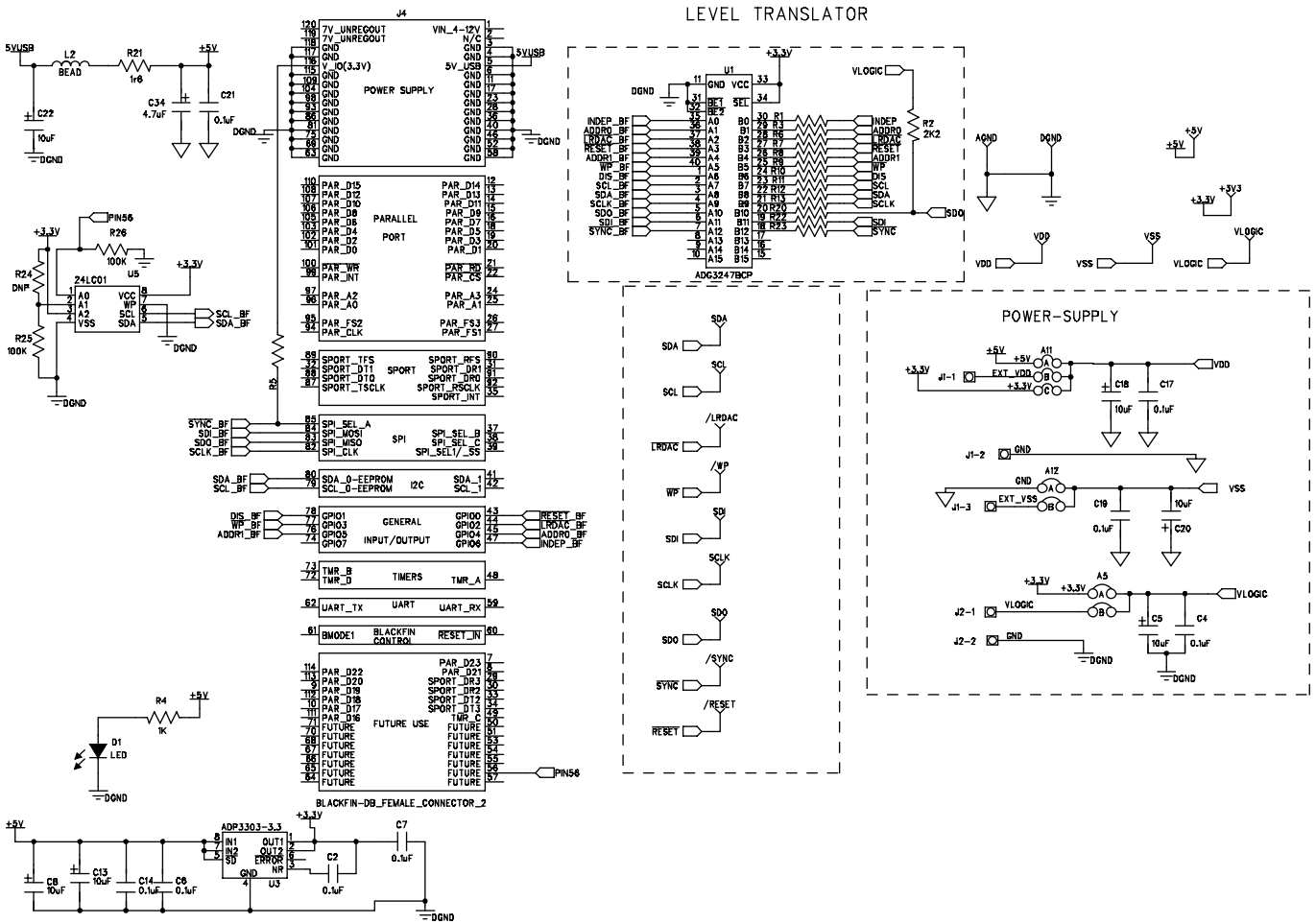
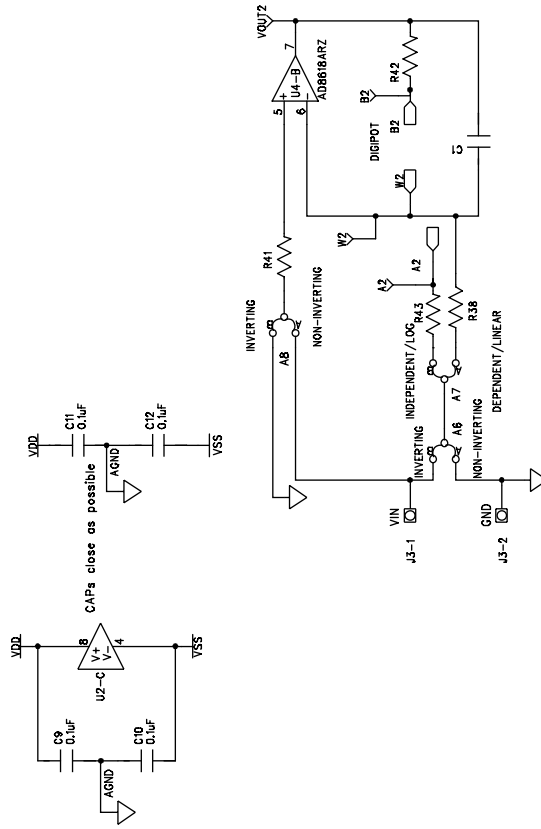
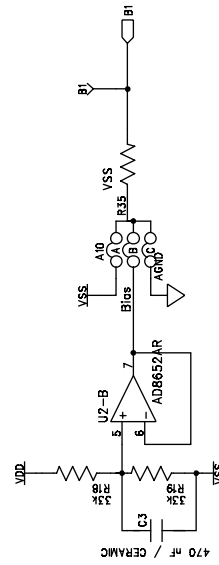
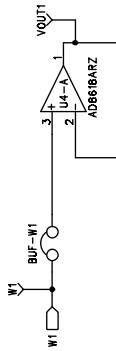
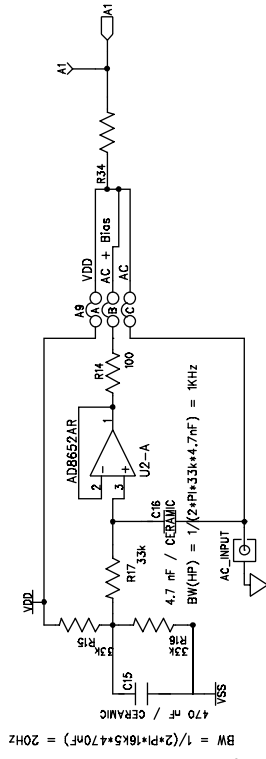


Figure 9. SDP Connector and Power Supply

DAC + FLOATING DAC + BW



INVERTING AND NON-INVERTING WITH LINEAR AND PSEUDO-LOG GAIN

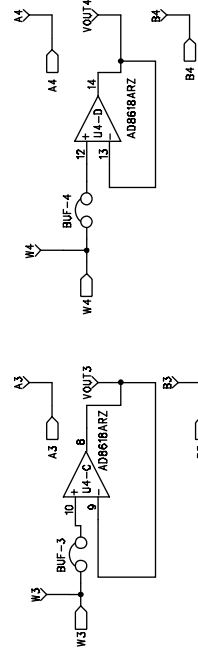


Figure 10. Schematic of Test Circuits

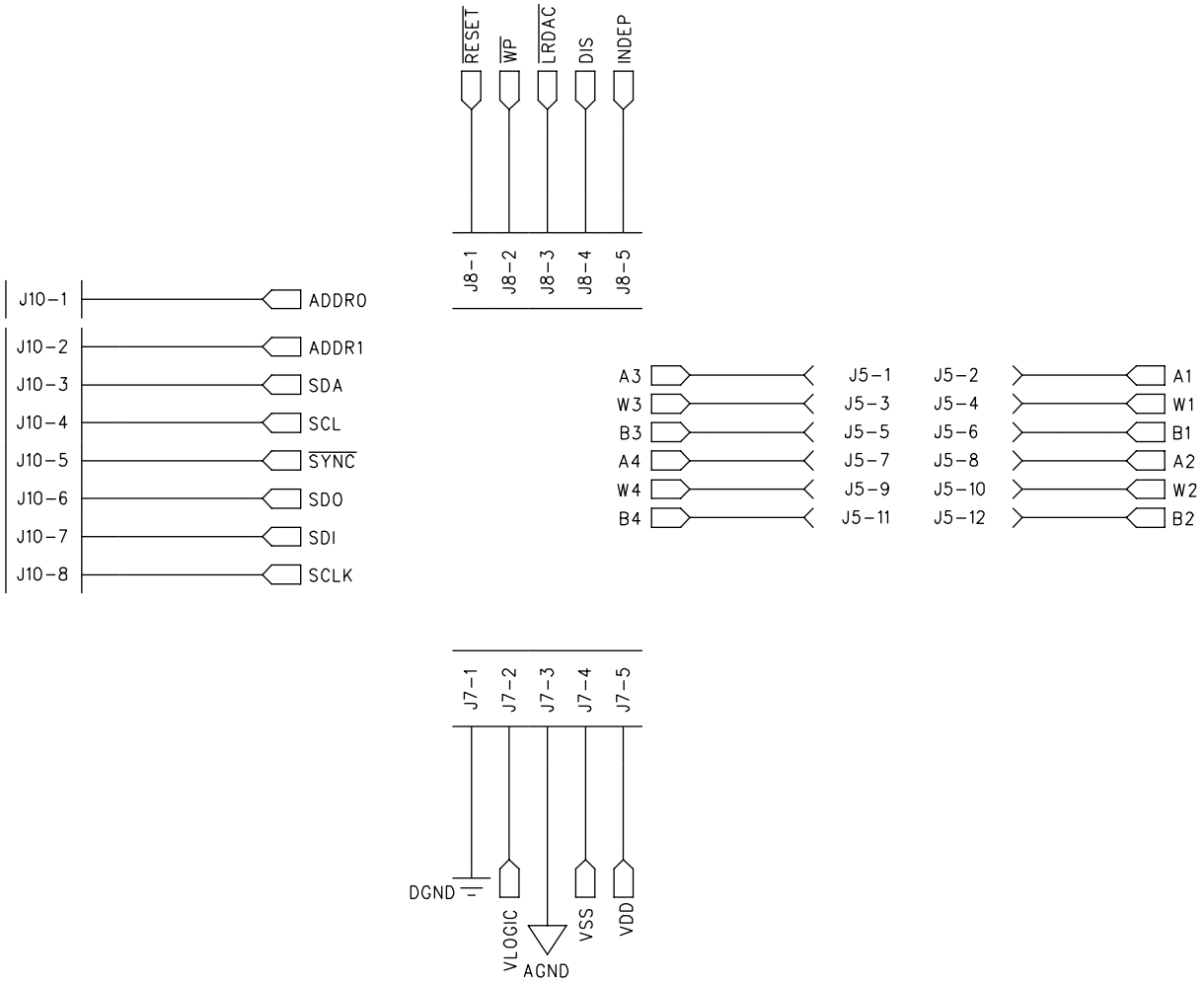


Figure 11. Schematic of Connectors to Daughter Board

10623-011

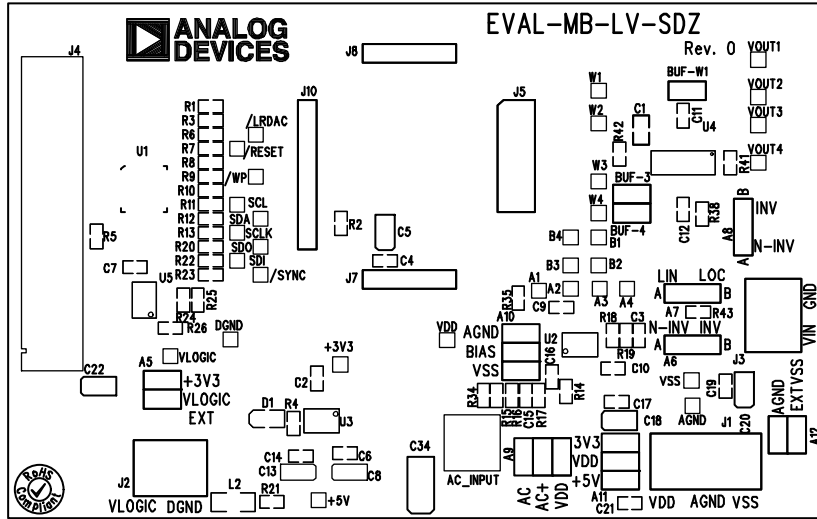


Figure 12. Component Side View

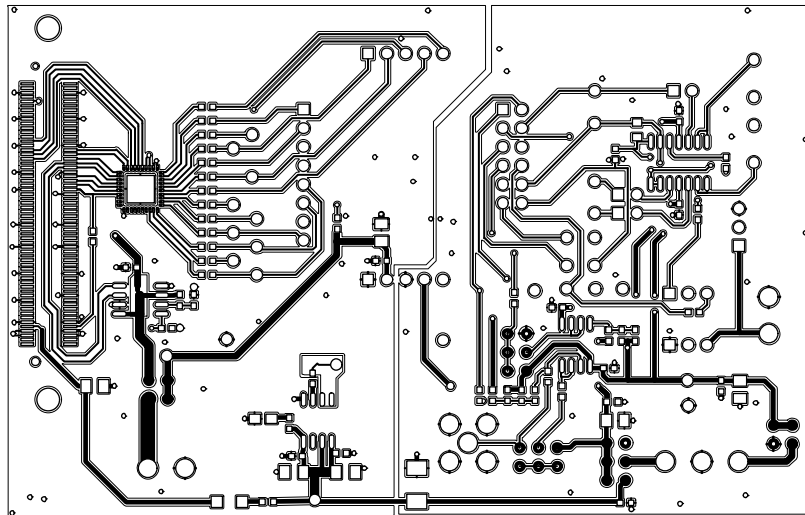


Figure 13. Component Placement Drawing

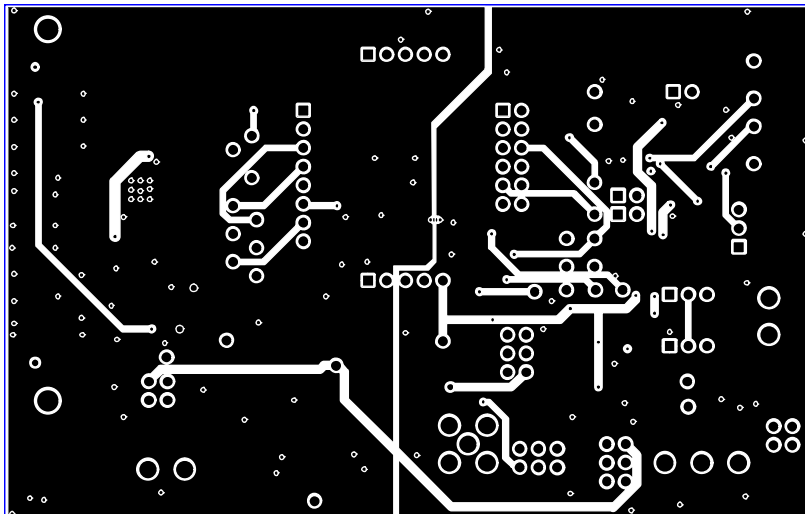
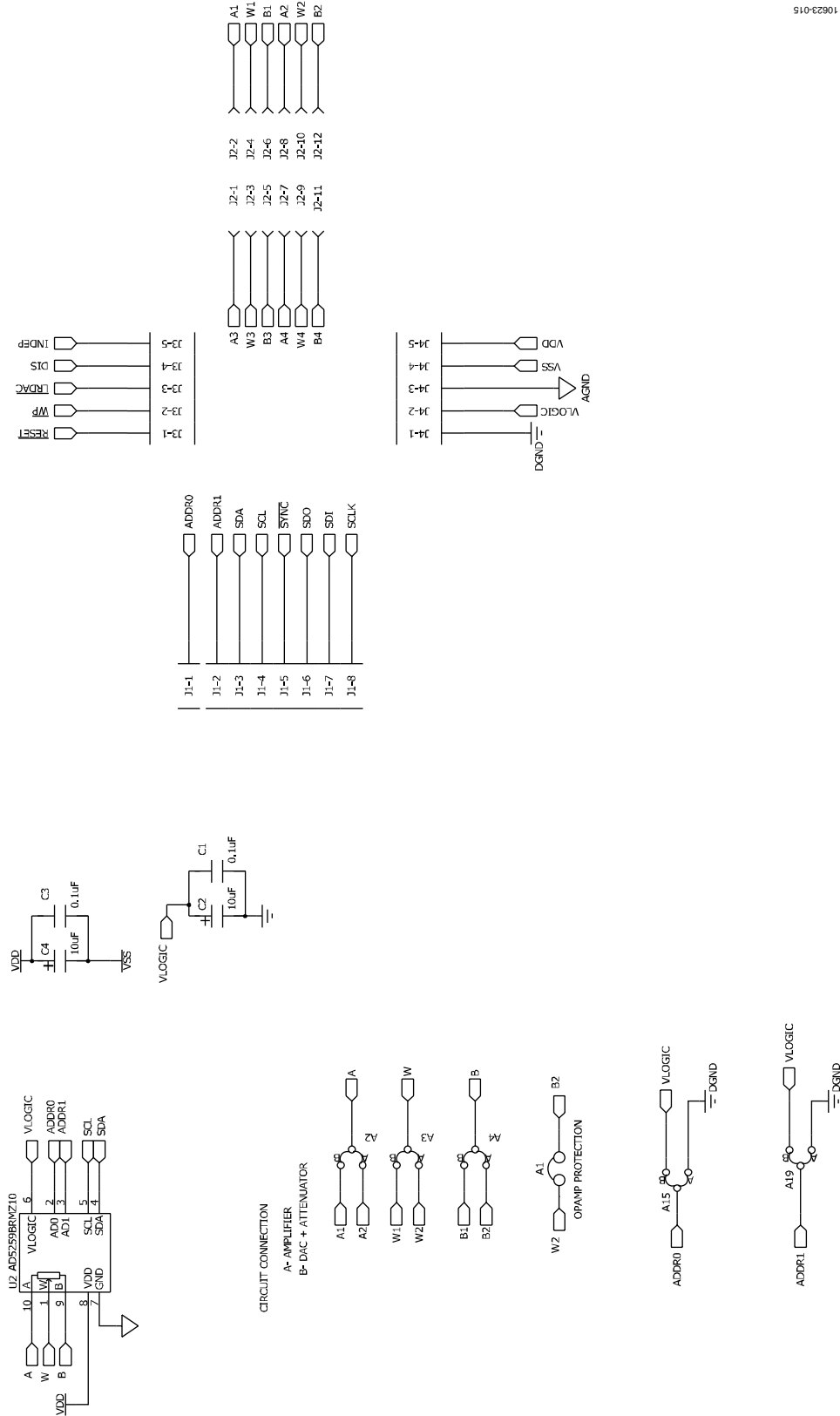


Figure 14. Layer 2 Side PCB Drawing

DAUGHTER BOARD



10623-015

Figure 15. Schematic of Daughter Board

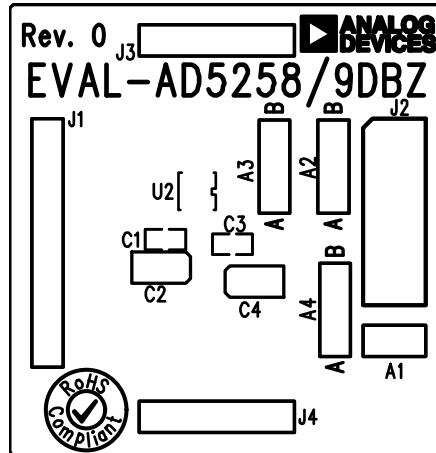


Figure 16. Component Side View

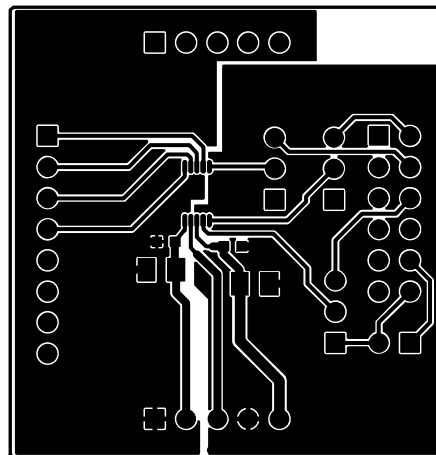


Figure 17. Component Placement Drawing

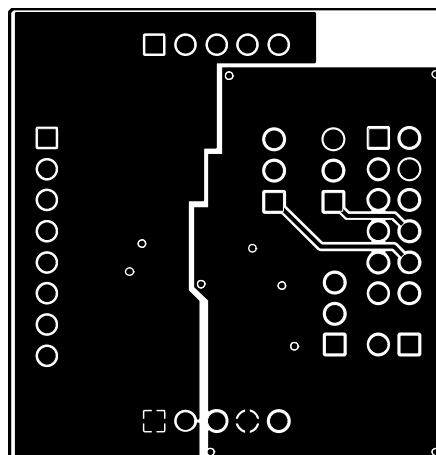


Figure 18. Layer 2 Side PCB Drawing

ORDERING INFORMATION

BILL OF MATERIALS

Table 7. Motherboard

Qty	Reference Designator	Description	Supplier ¹ /Part Number
3	BUF-3, BUF-4, BUF-W1	2-pin (0.1" pitch) header and shorting shunt	FEC 1022247 and 150-411
3	A6, A7, A8	3-pin SIL header and shorting link	FEC 1022248 and 150410
5	A5, A9, A10, A11, A12	6-pin (3 × 2), 0.1" header and shorting block	FEC 148-535 and 150-411 (36-pin strip)
1	J1	3-pin terminal block (5 mm pitch)	FEC 151790
2	J7, J8	4-pin SIL header	FEC 1098035
1	J4	Receptacle, 0.6 mm, 120-way	Digi-Key H1219-ND
1	J10	8-pin inline header; 100 mil centers	FEC 1098038
1	J5	12-pin (2 × 6), 0.1" pitch header	FEC 1098051
2	J2, J3	2-pin terminal block (5 mm pitch)	FEC 151789
17	R1, R3, R6, R7, R8, R9, R10, R11, R12, R13, R20, R22, R23, R34, R35, R42, R43	SMD resistor, 0 Ω, 0.01, 0603	FEC 9331662
1	R2	SMD resistor, 2.2 kΩ, 0.01, 0603	FEC 1750676
1	R41	SMD resistor, 1.7 kΩ, 1%, 0603	FEC 1170811
1	R21	Resistor, surge, 1.6 Ω, 1%, 0603	FEC 1627674
1	R38	SMD resistor, 2.7 kΩ, 1%, 0603	FEC 1750678
1	R14	SMD resistor, 100 Ω, 1%, 0603	FEC 9330364
1	R4	SMD resistor, 1 kΩ, 0.01, 0603	FEC 9330380
3	R5, R25, R26	SMD resistor, 100 kΩ, 1%, 0603	FEC 9330402
5	R15, R16, R17, R18, R19	SMD resistor, 33 kΩ, 1%, 0603	FEC 9331034
1	C1	SMD capacitor, 100 nF, 10%, 0805	FEC 165-0863
8	C4, C9, C10, C11, C12, C17, C19, C21	SMD capacitor, 0.1 μF, ±10%, 0603	FEC 1759122
4	C2, C6, C7, C14	SMD capacitor, 0.1 μF, ±10%, 0603	FEC 301-9482
2	C8, C13	SMD capacitor, 10 μF, ±10%	FEC 197-130
4	C18, C20, C22, C5	Capacitor, 10 μF, ±20%	FEC 1190107
2	C3, C15	Capacitor, 470 nF, ±10%, 0603	FEC 1414037
1	C16	Capacitor, 4.7 nF, ±10%, 0603	FEC 1414642
1	C34	Capacitor, 4.7 nF, ±20%	FEC 1432350
1	L2	Inductor, SMD, 600Z	FEC 9526862
1	D1	Green SMD LED	FEC 5790852
1	U1	Two-port level translating bus switch	ADG3247BCPZ
1	U2	Dual op amp	AD8652ARZ
1	U3	Precision low dropout voltage regulator	ADP3303ARZ-3.3
1	U4	Operational amplifier	AD8618ARZ
1	U5	I ² C serial EEPROM, 64k, 2.5 V, MSOP-8	FEC 1331335
27	LRDAC, RESET, SYNC, WP, A1, A2, A3, A4, AGND, B1, VOUT_C1, VOUT_C2, VOUT3, VOUT4, W1, W2, W3, W4	Terminal, PCB, black, PK100, test point	FEC 8731128
5	+3.3V, +5V, EXT_VDD, VLOGIC, EXT_VSS	Terminal, PCB, red, PK100	FEC 8731144

¹ FEC refers to Farnell Electronic Component Distributors; Digi-Key refers to Digi-Key Corporation.

Table 8. Daughter Board

Qty	Reference Designator	Description	Supplier ¹ /Part Number
1	U1	256-position digital potentiometer	AD5273BRJZ1-REEL7
1	A1	2-pin (0.1" pitch) header and shorting shunt	FEC 1022247 and 150-411
4	A2, A3, A4, A5	3-pin SIL header and shorting link	FEC 1022248 and 150410
1	C6	6.3 V tantalum capacitor (Case A), 10 μ F, \pm 20%	FEC 1190107
1	C3	50 V, X7R ceramic capacitor, 0.1 μ F, \pm 10%, 0603	FEC 1759122
1	J1	Header, 2.54 mm, PCB, 1 \times 8-way	FEC 1766172
1	J2	12-pin (2 \times 6), 0.1" pitch header	FEC 1804099
2	J3, J4	5-pin SIL header	FEC 1929016

¹ FEC refers to Farnell Electronic Component Distributors.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

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