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ON Semiconductor®

June 2017

FAN48618

2.5 MHz, Fixed-Output, Synchronous Tiny Boost® Regulator

Features

- Input Voltage Range: 2.7 V to 4.8 V
- Output Voltage: 5.25 V
- Internal Synchronous Rectification
- True Load Disconnect
- Short-Circuit Protection
- 9-Bump, 1.215 mm x 1.215 mm, 0.4 mm Pitch, WLCSP
- Three External Components: 2012 0.47 μ H Inductor, 0402 4.7 μ F Input Capacitor, 0603 22 μ F Output Capacitor

Applications

- Class-D Audio Amplifier and USB OTG Supply
- Boost for Low-Voltage Li-Ion Batteries
- Smart Phones, Tablets, Portable Devices, and Wearables

Description

The FAN48618 is a low-power boost regulator designed to provide a minimum voltage regulated rail from a standard single-cell Li-Ion battery and advanced battery chemistries. Even below the minimum system battery voltage, the device maintains output voltage regulation. The combination of built-in power transistors, synchronous rectification, and low supply current suit the FAN48618 for battery-powered applications.

The FAN48618 is available in a 9-bump, 0.4 mm pitch, Wafer-Level Chip-Scale Package (WLCSP).

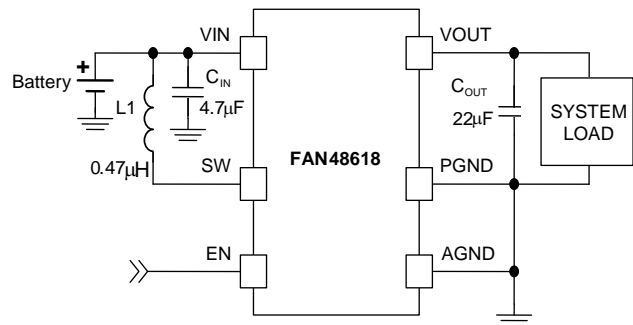


Figure 1. Typical Application

Ordering Information

| Part Number | V _{OUT} | Operating Temperature Range | Package | Packing Method | Device Marking |
|----------------|------------------|-----------------------------|--|------------------------------|----------------|
| FAN48618BUC53X | 5.25 V | -40°C to 85°C | 9-Bump, 0.4 mm Pitch, Wafer-Level Chip-Scale Package (WLCSP) | Tape and Reel ⁽¹⁾ | J9 |

Note:

1. Tape and reel specifications are available on www.onsemi.com.

FAN48618 — 2.5 MHz, Fixed-Output Synchronous Tiny Boost® Regulator

Block Diagram

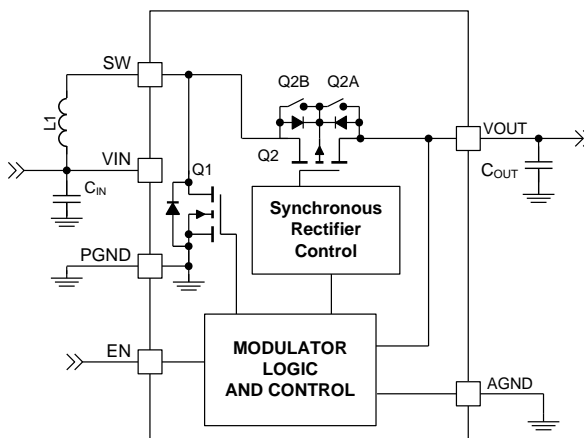


Figure 2. IC Block Diagram

Table 1. Recommended Components

| Component | Description | Vendor | Parameter | Typ. | Unit |
|------------------|---------------------------------|-----------------------------|----------------|------|------|
| L1 | 2012, 4.0 A, 0.8 mm Max. Height | CIGT201208EMR47SNE SEMCO | L | 0.47 | μH |
| | | | DCR (Series R) | 37 | mΩ |
| C _{IN} | 10%, 10 V, X5R, 0402 | CL05A475KP5NRNC SEMCO | C | 4.7 | μF |
| C _{OUT} | 20%, 10 V, X5R, 0603 | CL10A226MP8NUNE SEMCO | C | 22 | μF |

Pin Configuration

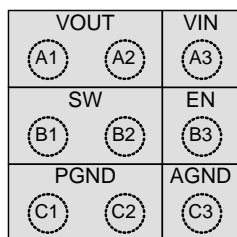


Figure 3. Top View

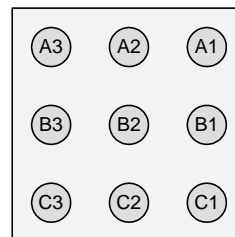


Figure 4. Bottom View

Pin Definitions

| Pin # | Name | Description |
|--------|------|--|
| A1, A2 | VOUT | Output Voltage. This pin is the output voltage terminal; connect directly to C _{OUT} . |
| A3 | VIN | Input Voltage. Connect to the Li-Ion battery input power source and the bias supply for the gate drivers. |
| B1, B2 | SW | Switching Node. Connect to inductor. |
| B3 | EN | Enable. When this pin is HIGH, the circuit is enabled. It is recommended to connect and set to a logic voltage of 1.8 V after UVLO has been satisfied. |
| C1, C2 | PGND | Power Ground. This is the power return for the IC. C _{OUT} capacitor should be returned with the shortest path possible to these pins. |
| C3 | AGND | Analog Ground. This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin. Connect to PGND at a single point. |

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | | Min. | Max. | Unit |
|------------------|--|---|------|--------------------|------|
| V _{IN} | Voltage on VIN Pin | | -0.3 | 6.0 | V |
| V _{OUT} | Voltage on VOUT Pin | | | 6.0 | V |
| V _{SW} | Voltage on SW Node | DC | -0.3 | 6.0 | V |
| | | Transient: 10 ns, 3 MHz | -1.0 | 8.0 | |
| V _{CC} | Voltage on Other Pins | | -0.3 | 6.0 ⁽²⁾ | V |
| ESD | Electrostatic Discharge Protection Level | Human Body Model, ANSI/ESDA/JEDEC JS-001-2012 | 2 | | kV |
| | | Charged Device Model per JESD22-C101 | 1 | | |
| T _J | Junction Temperature | | -40 | +150 | °C |
| T _{STG} | Storage Temperature | | -65 | +150 | °C |
| T _L | Lead Soldering Temperature, 10 Seconds | | | +260 | °C |

Note:

2. Lesser of 6.0 V or V_{IN} + 0.3 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON Semiconductor does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Min. | Max. | Unit |
|------------------|-------------------------------|------|------|------|
| V _{IN} | Supply Voltage | 2.7 | 4.8 | V |
| I _{OUT} | Output Current ⁽⁴⁾ | | 1200 | mA |
| T _A | Ambient Temperature | -40 | +85 | °C |
| T _J | Junction Temperature | -40 | +125 | °C |

Note:

3. Typical 1 A and 1.2A I_{OUT} at V_{IN} = 2.7 V and 3.0 V, respectively.

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards with vias in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature, T_{J(max)}, at a given ambient temperature, T_A.

| Symbol | Parameter | Typical | Unit |
|-----------------|--|---------|------|
| Θ _{JA} | Junction-to-Ambient Thermal Resistance | 50 | °C/W |

Electrical Specifications

Recommended operating conditions, unless otherwise noted, circuit per Figure 1, $V_{OUT}= 5.25\text{ V}$, $V_{IN} = 2.7\text{ V}$ to 4.8 V , and $T_A = -40^\circ\text{C}$ to 85°C . Typical values are given $V_{IN} = 3.6\text{ V}$ and $T_A = 25^\circ\text{C}$.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---------------------|---|---|------|------|------|------------------|
| Power Supply | | | | | | |
| I_Q | V_{IN} Quiescent Current | $V_{IN}=3.6\text{ V}$, $I_{OUT}=0$, $EN=V_{IN}$ | | 90 | 140 | μA |
| | | Shutdown: $EN=0$, $V_{IN}=3.7\text{ V}$, $V_{OUT}=0\text{ V}$ | | 2.7 | 10.0 | |
| V_{UVLO} | Under-Voltage Lockout | V_{IN} Rising | | 2.2 | 2.3 | V |
| V_{UVLO_HYS} | Under-Voltage Lockout Hysteresis | | | 150 | | mV |
| Inputs | | | | | | |
| V_{IH} | Enable HIGH Voltage | | 1.2 | | | V |
| V_{IL} | Enable LOW Voltage | | | | 0.4 | V |
| I_{PD} | Current Sink Pull-Down | EN Pin, Logic HIGH | | 100 | | nA |
| R_{LOW} | Low-State Active Pull-Down | EN Pin, Logic LOW | 200 | 300 | 400 | k Ω |
| Outputs | | | | | | |
| V_{REG} | Output Voltage Accuracy DC ⁽⁴⁾ | Referred to V_{OUT} , $V_{IN}=3.0$ to 4.5 V | -2 | | 4 | % |
| I_{LK_OUT} | V_{IN} -to- V_{OUT} Leakage Current | $V_{OUT}=0$, $EN=0$, $V_{IN}=2.7\text{ V}$ | | | 1 | μA |
| I_{LK} | V_{OUT} -to- V_{IN} Reverse Leakage Current | $V_{OUT}=5.25\text{ V}$, $EN=0$, $V_{IN}=2.7\text{ V}$ | | | 3.5 | μA |
| V_{RIPPLE} | Output Ripple ⁽⁵⁾ | 0 mA to 1 A | | 25 | | mV |
| Timing | | | | | | |
| f_{SW} | Switching Frequency | $V_{IN}=3.6\text{ V}$, $V_{OUT}=5.25\text{ V}$, $I_{LOAD}=500\text{ mA}$ | 2.0 | 2.5 | 3.0 | MHz |
| t_{SS} | Soft-Start EN HIGH to Regulation ⁽⁵⁾ | $V_{IN}=3.0\text{ V}$, $V_{OUT}=5.25\text{ V}$, $I_{LOAD}=0\text{ mA}$, $C_{OUT}=22\text{ }\mu\text{F}$ (0603) | | 1000 | | μs |
| I_{SS} | Input Peak Current | | | 90 | 200 | mA |
| t_{RST} | FAULT Restart Timer ⁽⁵⁾ | | | 20 | | ms |
| Power Stage | | | | | | |
| $R_{DS(ON)N}$ | N-Channel Boost Switch $R_{DS(ON)}$ | $V_{IN}=3.6\text{ V}$, $V_{OUT}=5.25\text{ V}$ | | 80 | 130 | m Ω |
| $R_{DS(ON)P}$ | P-Channel Sync. Rectifier $R_{DS(ON)}$ | $V_{IN}=3.6\text{ V}$, $V_{OUT}=5.25\text{ V}$ | | 65 | 115 | m Ω |
| I_{V_LIM} | Boost Valley Current Limit | $V_{OUT}=5.25\text{ V}$ | | 2.3 | | A |
| $I_{V_LIM_SS}$ | Boost Soft-Start Valley Current Limit | $V_{IN}<V_{OUT}<V_{OUT_TARGET}$ | | 1.3 | | A |
| T_{150T} | Over-Temperature Protection (OTP) | | | 150 | | $^\circ\text{C}$ |
| T_{150H} | OTP Hysteresis | | | 20 | | $^\circ\text{C}$ |

Notes:

- DC I_{LOAD} from 0 to 1 A. V_{OUT} measured from mid-point of output voltage ripple. Effective capacitance of $C_{OUT} \geq 5\text{ }\mu\text{F}$.
- Guaranteed by design and characterization; not tested in production.

Typical Performance Characteristics

Unless otherwise specified; $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 5.25\text{ V}$, $T_A = 25^\circ\text{C}$, and circuit and components according to Figure 1.

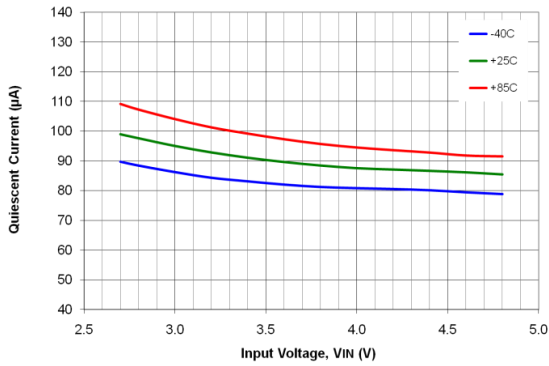


Figure 5. Quiescent Current vs. Input Voltage and Temperature

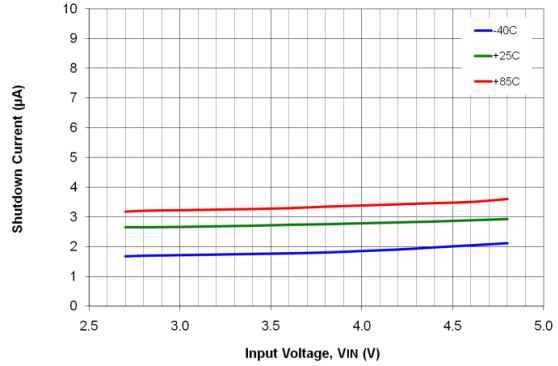


Figure 6. Shutdown Current vs. Load Current and Temperature

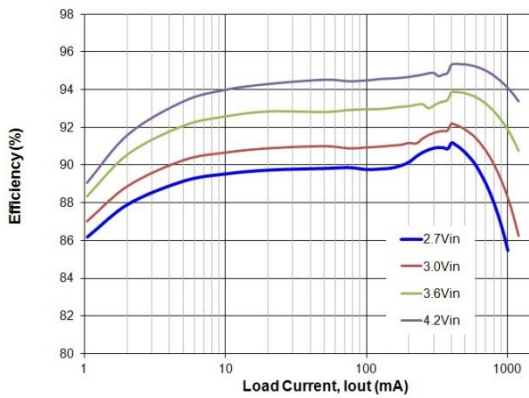


Figure 7. Efficiency vs. Load Current and Input Voltage

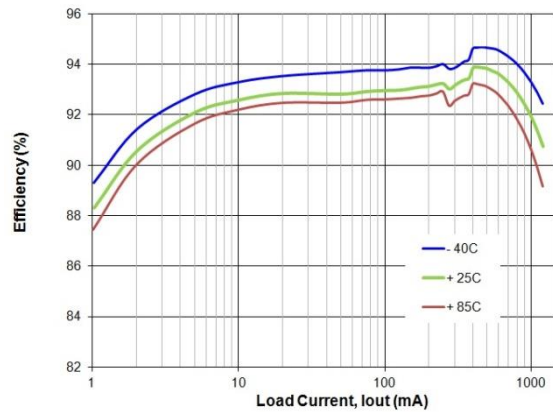


Figure 8. Efficiency vs. Load Current and Temperature

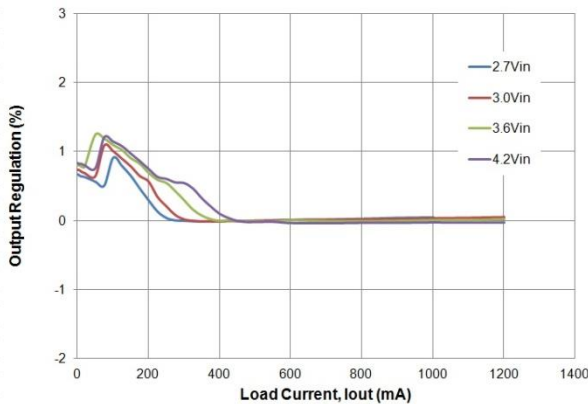


Figure 9. Output Regulation vs. Load Current and Input Voltage

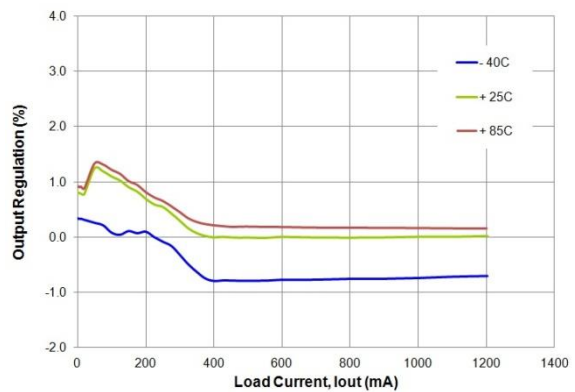


Figure 10. Output Regulation vs. Load Current and Temperature

Typical Performance Characteristics

Unless otherwise specified; $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 5.25\text{ V}$, $T_A = 25^\circ\text{C}$, and circuit and components according to Figure 1.

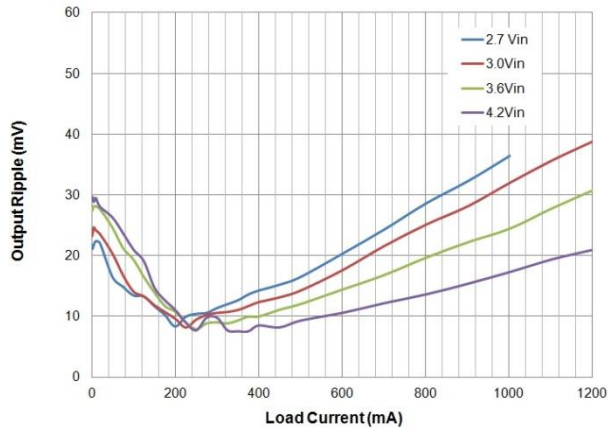


Figure 11. Output Ripple vs. Load Current and Input Voltage

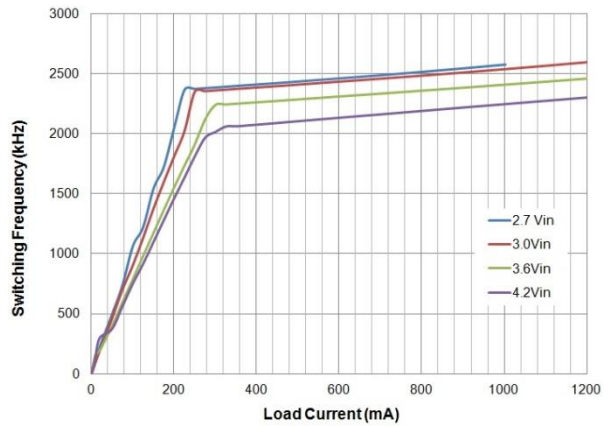


Figure 12. Switching Frequency vs. Load Current and Temperature

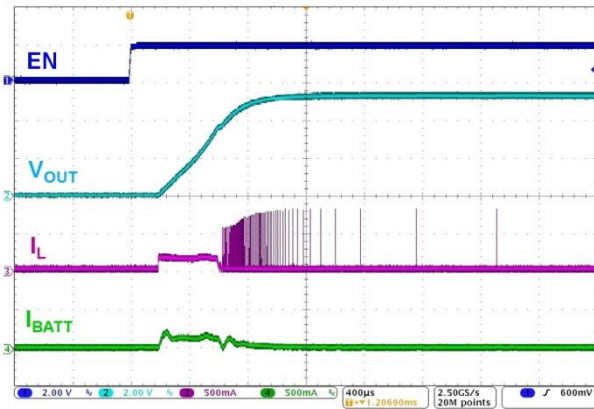


Figure 13. Startup, No Load

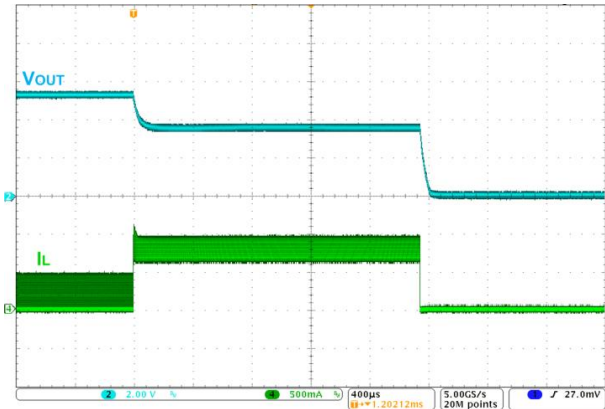


Figure 14. Overload Protection

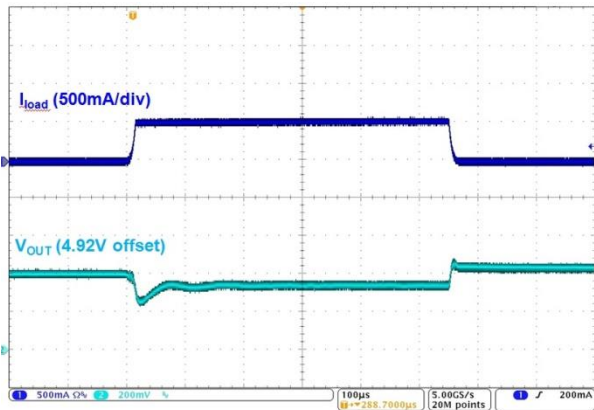


Figure 15. Load Transient, 3.8 V_{IN} , $0 \leftrightarrow 500\text{ mA}$, $8\ \mu\text{s}$ Edge

Functional Description

FAN48618 is a synchronous boost regulator, typically operating at 2.5 MHz in Continuous Conduction Mode (CCM), which occurs at moderate to heavy load current and low V_{IN} voltage. Typically, 1 A and 1.2 A output currents can be obtained at input voltages ≥ 2.7 V and ≥ 3.0 V, respectively. Passive component derating must be taken into consideration, as well as, thermal properties of the regulator.

Table 2. Operating Modes

| Mode | Description | Invoked When: |
|------|------------------|--------------------------------------|
| LIN | Linear Startup | $V_{IN} > V_{OUT}$ |
| SS | Boost Soft-Start | $V_{IN} < V_{OUT} < V_{OUT(TARGET)}$ |
| BST | Boost Mode | $V_{OUT} = V_{OUT(TARGET)}$ |

Boost Mode Regulation

The current-mode modulator achieves excellent transient response and smooth transitions between CCM and DCM operation. During CCM operation, the device maintains a switching frequency of about 2.5 MHz. In light-load operation (DCM), frequency is naturally reduced to maintain high efficiency.

Startup and Shutdown

When EN is LOW, all bias circuits are off and the regulator enters Shutdown Mode. During shutdown, current flow is prevented from V_{IN} to V_{OUT} , as well as reverse flow from V_{OUT} to V_{IN} . It is recommended to keep load current draw below 50 mA until the device successfully executes startup. Table 3 describes the startup sequence.

Table 3. Boost Startup Sequence

| Start Mode | Entry | Exit | End Mode | Timeout (μ s) |
|------------|----------------------------|-----------------------------|----------|--------------------|
| LIN1 | $V_{IN} > V_{UVLO}$, EN=1 | $V_{OUT} > V_{IN} - 300$ mV | SS | |
| | | TIMEOUT | LIN2 | 512 |
| LIN2 | LIN1 Exit | $V_{OUT} > V_{IN} - 300$ mV | SS | |
| | | TIMEOUT | FAULT | 1024 |
| SS | LIN1 or LIN2 Exit | $V_{OUT} = V_{OUT(TARGET)}$ | BST | |
| | | OVERLOAD TIMEOUT | FAULT | 64 |

LIN Mode

When EN is HIGH and $V_{IN} > V_{UVLO}$, the regulator attempts to bring V_{OUT} within 300 mV of V_{IN} using the internal fixed-current source from V_{IN} (Q2). The current is limited to the I_{SS} set point, which is typically 90 mA. The linear charging current is limited to a maximum of 200 mA to prevent any “brownout” situations where the system voltage drops too low.

During LIN1 Mode, if V_{OUT} reaches $V_{IN} - 300$ mV, SS Mode is initiated. Otherwise, LIN1 Mode expires after 512 μ s and LIN2 Mode is entered.

In LIN2 Mode, the current source is equal to LIN1 current source I_{SS} , typically 90 mA. If V_{OUT} fails to reach $V_{IN} - 300$ mV after 1024 μ s, a fault condition is declared and the device waits 20 ms (t_{RST}) to attempt an automatic restart.

Soft-Start (SS) Mode

Upon the successful completion of LIN Mode ($V_{OUT} \geq V_{IN} - 300$ mV), the regulator begins switching with boost pulses current limited to 50% of nominal level.

During SS Mode, if V_{OUT} fails to reach regulation during the SS ramp sequence for more than 64 μ s, a fault is declared. If a large C_{OUT} is used, the reference is automatically stepped slower to avoid excessive input current draw.

Boost (BST) Mode

This is a normal operating mode of the regulator.

Fault State

The regulator enters Fault State under any of the following conditions:

- V_{OUT} fails to achieve the voltage required to advance from LIN Mode to SS Mode.
- V_{OUT} fails to achieve the voltage required to advance from SS Mode to BST Mode.
- Boost current limit triggers for 2 ms during BST Mode.
- $V_{IN} - V_{OUT} > 300$ mV; this fault can occur only after successful completion of the soft-start sequence.
- $V_{IN} < V_{UVLO}$.

Once a fault is triggered, the regulator stops switching and presents a high-impedance path between V_{IN} and V_{OUT} . After 20 ms, automatic restart is attempted.

Over-Temperature

The regulator shuts down if the die temperature exceeds 150°C. Restart occurs when the IC has cooled by approximately 20°C.

Application Information

Output Capacitance (C_{OUT})

The effective capacitance (C_{EFF}⁽⁶⁾) of small, high-value ceramic capacitors decreases as the bias voltage increases, as illustrated in Figure 16.

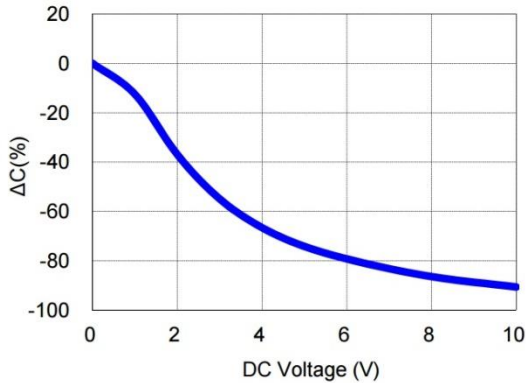


Figure 16. C_{EFF} for 22 μF, 0603, X5R, 10 V-Rated Capacitor (SEMCO CL10A226MP8NUNE)

FAN48618 is guaranteed for stable operation with the typical value of C_{EFF} outlined in Table 4

Table 4. Typical C_{EFF} Required for Stability

| Operating Conditions | | | C _{EFF} (μF) |
|----------------------|---------------------|------------------------|-----------------------|
| V _{OUT} (V) | V _{IN} (V) | I _{LOAD} (mA) | |
| 5.25 | 2.7 to 4.5 | 0 to 1000 | 5 |

Note:

6. C_{EFF} varies by manufacturer, capacitor material, and case size.

Inductor Selection

Recommended nominal inductance value is 0.47 μH.

The FAN48618 employs valley-current limiting, so peak inductor current can reach 3.6 A for a short duration during overload conditions. Saturation causes the inductor current ripple to increase under high loading, as only the valley of the inductor current ripple is controlled.

Startup

Input current limiting is active during soft-start, which limits the current available to charge C_{OUT} and any additional capacitance on the V_{OUT} line. If the output fails to achieve regulation within the limits described in the Soft-Start section above, a fault occurs, causing the circuit to shut down. It waits about 20 ms before attempting a restart. If the total combined output capacitance is very high, the circuit may not start on the first attempt, but eventually achieves regulation if no load is present. If a high current load and high capacitance are both present during soft-start, the circuit may fail to achieve regulation and continually attempt soft-start, only to have the output capacitance discharged by the load when in Fault State.

Output Voltage Ripple

Output voltage ripple is inversely proportional to C_{OUT}. During t_{ON}, when the boost switch is on, all load current is supplied by C_{OUT}.

$$V_{RIPPLE(P-P)} = t_{ON} \cdot \frac{I_{LOAD}}{C_{OUT}} \quad (1)$$

and

$$t_{ON} = t_{SW} \cdot D = t_{SW} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad (2)$$

therefore:

$$V_{RIPPLE(P-P)} = t_{SW} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \cdot \frac{I_{LOAD}}{C_{OUT}} \quad (3)$$

$$t_{SW} = \frac{1}{f_{SW}} \quad (4)$$

The maximum V_{RIPPLE} occurs when V_{IN} is minimum and I_{LOAD} is maximum. For better ripple performance, more output capacitance can be added.

Layout Recommendations

The layout recommendations below highlight various top-copper pours by using different colors.

To minimize spikes at V_{OUT}, C_{OUT} must be placed as close as possible to PGND and V_{OUT}, as shown below.

For best thermal performance, maximize the pour area for all planes other than SW. The ground pour, especially, should fill all available PCB surface area and be tied to internal layers with a cluster of thermal vias.

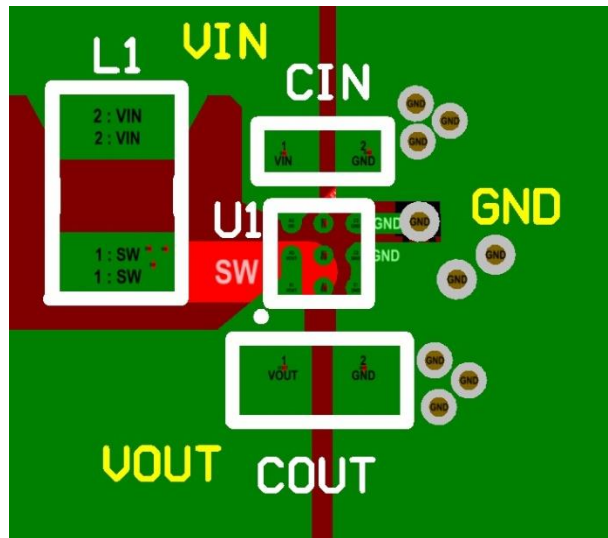


Figure 17. Layout Recommendation

Physical Dimensions

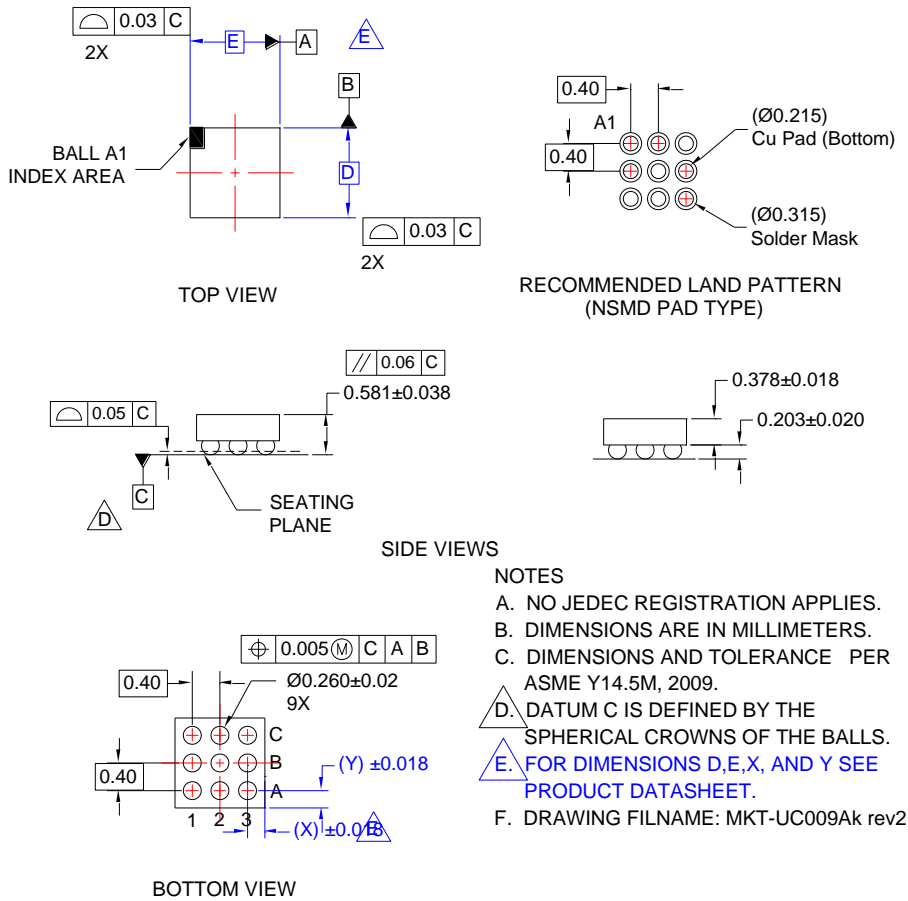


Figure 18. 9-Bump, 0.4 mm Pitch, Wafer-Level Chip-Scale Package (WLCSP)

Table 5. Product-Specific Dimensions

| D | E | X | Y |
|-----------------|-----------------|-----------|-----------|
| 1.215 ±0.030 mm | 1.215 ±0.030 mm | 0.2075 mm | 0.2075 mm |

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