Document Number: KT33905UG
Rev. 2.0, 9/2011

KIT33905 Evaluation Boards

Supports KIT33905D5EKEVBE (5 Volt)/KIT33905BD3EVBE (3.3 Volt)

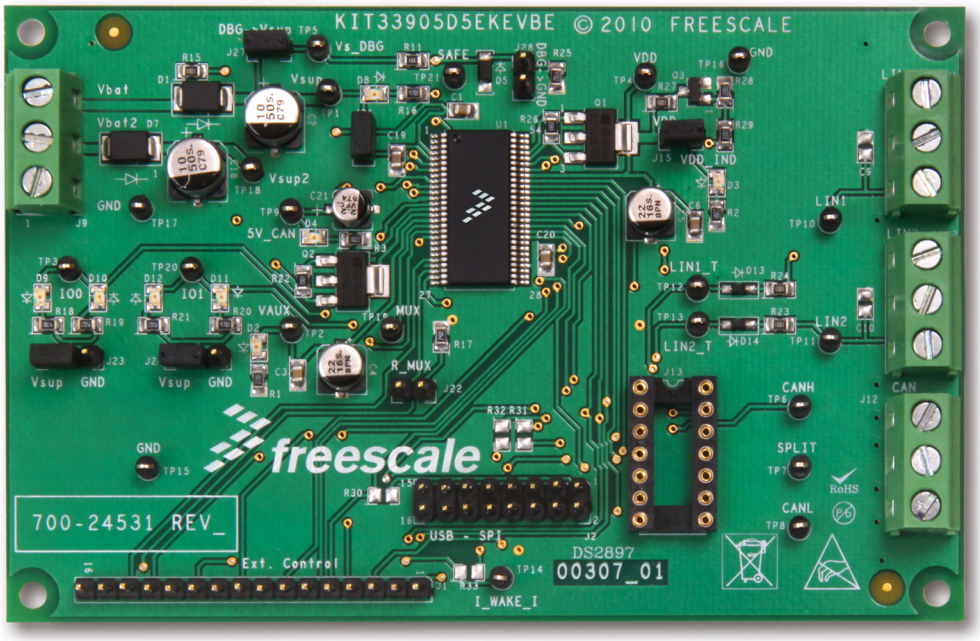

Figure 1. KIT33905D5EKEVBE/KIT33905BD3EVBE Evaluation Boards

Table of Contents

1 Kit Contents / Packing List

- KIT33905D5EKEVBE or KIT33905BD3EVBE Hardware
- CD33905 (includes SPIGen Software)
- CABLE, RIBBON FLAT 16 PIN ASSY, 0.100" PITCH, 6" LENGTH

2 Important Notice

Freescale provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This EVB may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This EVB is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact Freescale sales and technical support services.

Should this evaluation kit not meet the specifications indicated in the kit, it may be returned within 30 days from the date of delivery and will be replaced by a new kit.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typical”, must be validated for each customer application by customer’s technical experts.

Freescale does not convey any license under its patent rights nor the rights of others. Freescale products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale product could create a situation where personal injury or death may occur.

Should the Buyer purchase or use Freescale products for any such unintended or unauthorized application, the Buyer shall indemnify and hold Freescale and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale was negligent regarding the design or manufacture of the part.Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

3 Introduction

This evaluation board allows the user to implement the functionality of the MC33905 product System Basis Chip (SBC).

This EVB includes two I/O test points that can be configured to be pulled up to V_{SUP}, or pulled down to GND through a resistor and indicator LED. These are easily configured via jumper settings. The SBC can also be exercised in debug mode (watchdog re-fresh/monitoring not needed) by simply populating a jumper. Separating the input supply voltage to VSUP1 and VSUP2 is also made simple with a jumper configuration. Specified resistor pull-downs can be implemented on DBG and MUX pins via simple jumper configurations. The status of I/O0, I/O1, VAUX, 5V_CAN, SAFE, and VDD can be visually monitored via on-board LEDs. The CAN and LIN Bus signals are provided through terminal block connectors.

An isolated terminal block connector is implemented to provide power to the evaluation board with an external DC power supply.

The evaluation board is operated through the graphical user interface paired up with the SPI dongle board (KITUSBSPIDGLEVME) through the 2x8 pin ribbon cable. Additionally, for added flexibility, the user can implement a custom board with a microcontroller to talk to the SBC via the 16 pin header.

3.1 EVB Features

- Nominal operating supply voltage range of 5.5 V to 27 V
- Individually routed power supply inputs for VSUP1 and VSUP2
- 5.0/3.3 V regulator for MCU with an external PNP ballast transistor to increase current capability
- Multiple CAN Bus termination options supported via socket
- Two high/low side I/Os (SPI configurable) accessible through test points
- Status of I/O0 and I/O1 indicated by an LED (dependent on jumper configuration)
- Debug mode/watchdog configuration via jumper settings
- MUX output voltage accessible through a test point and external resistor selectable through jumper
- 3.3 V or 5.0 V output voltage test point VAUX (SPI configurable)
- I_WAKE_I test point to enable a FET and load VDD with current to wake-up the SBC
- LIN1_T and LIN2_T test points to monitor I/O voltages (SPI configurable)
- I/O0, I/O1, VAUX, 5V_CAN, SAFE, and VDD status indicated by LED
- 100 mil 2x8 pin standard header connector for SPI communication
- 100 mil 16 pin standard header connector for custom MCU board connections

3.2 Device Description/Features

- Protected 5.0 V or 3.3 V regulators for MCU (part number selectable) and additional ICs (SPI configurable) with optional external PNP usage to increase current capability for MCU
- Fully-protected embedded 5.0 V regulator for the CAN driver
- Extremely low quiescent current in low power modes
- Multiple under-voltage detections to address various MCU specifications and system operation modes (i.e. cranking)
- Multiple wake-up sources in low power modes: CAN or LIN bus, I/O transition, automatic timer, SPI message, and VDD over-current detection
- Voltage, current, and temperature protection with enhanced diagnostics that can be monitored by the system via a MUX output
- ISO11898-5 high speed CAN interface compatibility for baud rates of 40 kb/s to 1.0 Mb/s. LIN 2.1 and J2602 LIN interface compatibility
- Pb-free packaging designated by suffix code EK

4 Required Equipment

4.1 Minimum Required Equipment

- Power supply: minimum 5.5 V and 200 mA current
- Any piece of equipment/board that is capable of producing TXD and/or CAN and LIN messages
- KITUSBSPIDGLEVME (USB-to-SPI Kit)
- USB cable
- CABLE, RIBBON FLAT 16 PIN ASSY, 0.100" PITCH, 6" LENGTH
- USB enabled computer with Windows XP or higher
- SPIGen software (Setup.exe)

5 EVB Setup Configuration

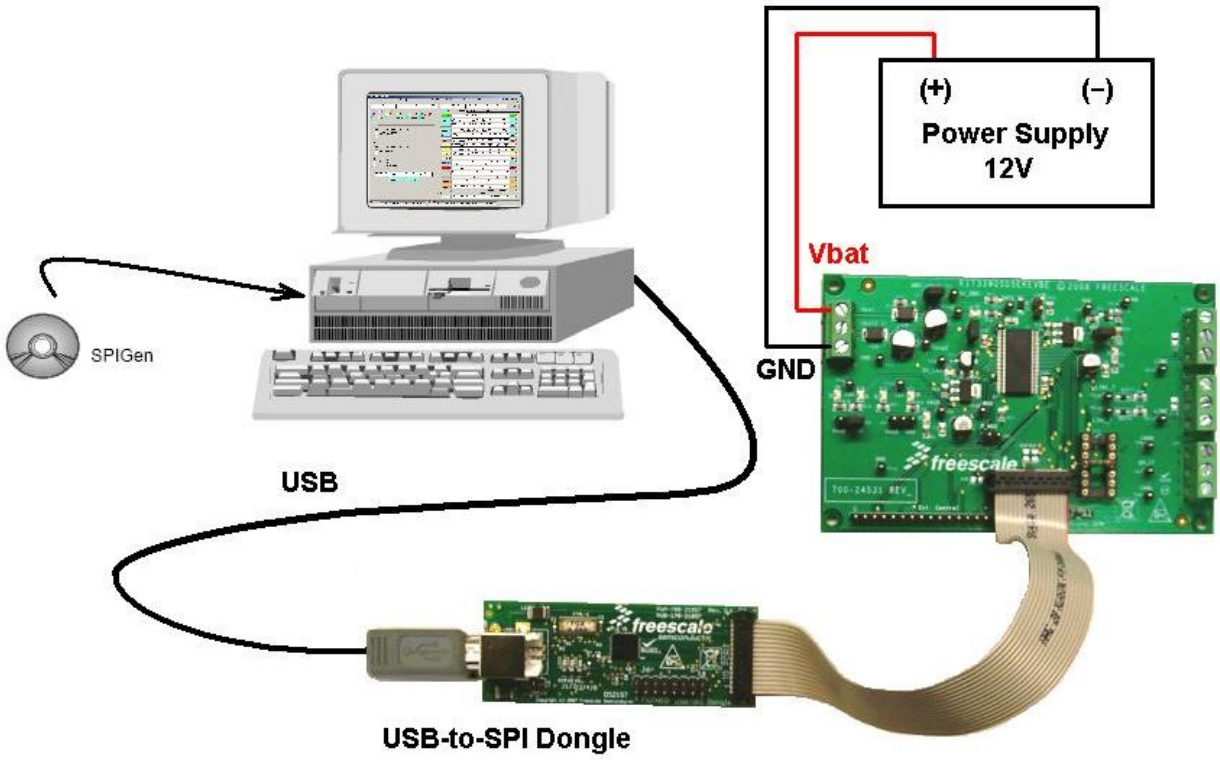

Figure 2. EVB Setup Configuration Diagram

6 Hardware Configuration

KIT33905D5EKEVBE/KIT33905BD3EVBE operates with a single 5.5 V minimum power supply and can be driven with the KITUSBSPIDGLEVME along with its GUI. For added flexibility, it's also possible to develop a custom board to drive this evaluation board via the 16 pin standard header.

6.1 Board Implementation

For Standard EVB configuration, set up the jumpers as shown on Figure 3. If the jumper configuration is in accordance with Jumper Connections, on page 8, The VDD (D3) and the 5V_CAN (D4) LEDs must be ON at startup. If CAN communication will be exercised, populate the CAN termination socket (J13) with the necessary components to implement the chosen CAN Termination as shown on Figure 4.

JUMPER	*POSITION*
J15	1-2
J21	1-2
J22	1-2
J23	OPEN
J24	OPEN
J27	1-2
J28	OPEN

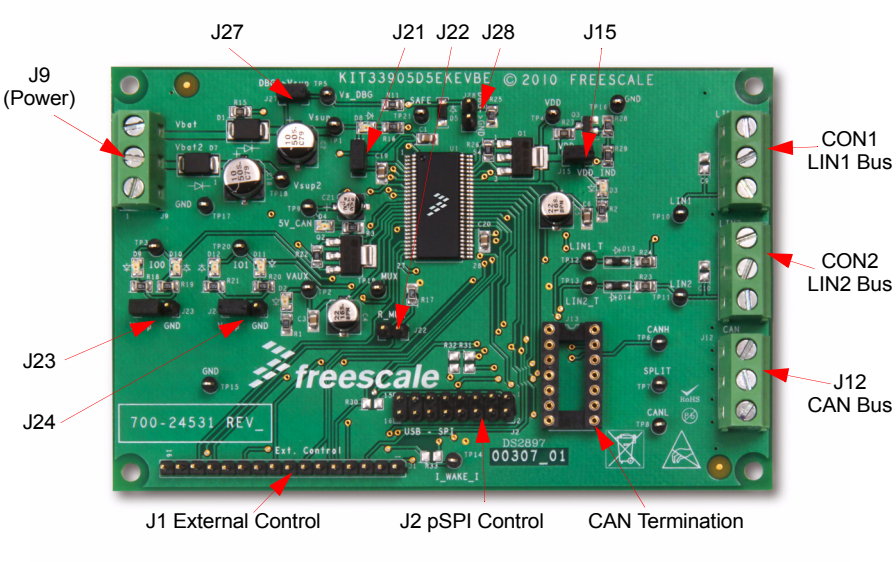

Figure 3. Manual Mode Jumper Settings

6.2 Jumper Connections

Name	Description
J15	VDD Status Jumper closed -> LED indicator enabled
J21	V_{SUP} source connection Jumper closed -> V_{SUP} connected to $V_{SUP}2$
J22	MUX pin output Jumper closed -> external 2.4 kohm resistor pull-down to GND implemented
J23	I/O0 configuration 1-2 closed -> 4.7 kohm pull-down resistor to GND and indicator LED implemented 2-3 closed -> 15 kohm pull-up resistor to V_{SUP} and indicator LED implemented
J24	I/O1 configuration 1-2 closed -> 4.7 kohm pull-down resistor to GND and indicator LED implemented 2-3 closed -> 15 kohm pull-up resistor to V_{SUP} and indicator LED implemented
J27	DBG configuration Jumper closed -> SBC runs in debug mode (no need to refresh/monitor watchdog) J28 MUST be left open
J28	DBG external pull-down resistor configuration Jumper closed -> 47 kohm pull-down resistor to GND implemented J27 MUST be left open

6.3 CAN Termination Configurations

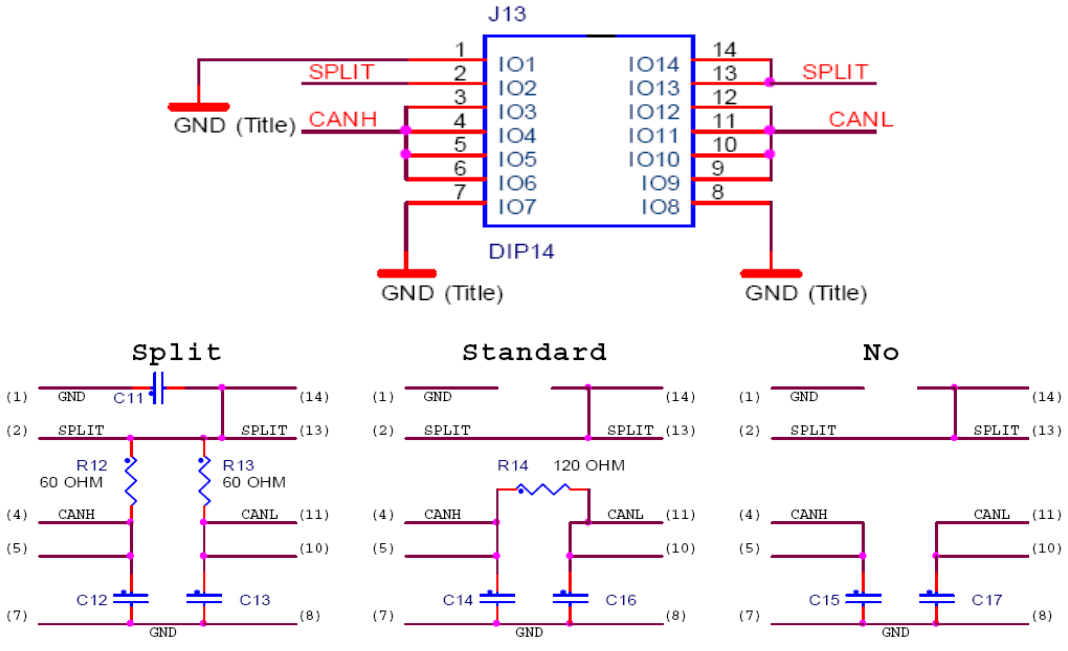

Figure 4. CAN Termination Configurations Via J13 Socket

6.4 Power Supply and Input/Output Connectors

The three pin terminal block (J9) serves as the main power terminal to supply a minimum of 5.5 V to operate KIT33905D5EKEVBE/KIT33905BD3EVBE.

The CAN, LIN1, and LIN2 bus signals are accessible through the three pin terminal blocks J12, CON1, and CON2 respectively.

6.5 Connector J1 – External Control

Pin #	Pin Name	Description
1	MISO	SPI data sent to the MCU. When the CS is high, MISO is high-impedance
2	MOSI	SPI data received by the device
3	SCLK	Clock input for the Serial Peripheral Interface (SPI) of the device
4	CSB	Chip select pin for the SPI. When the CS is low, the device is selected. In Low Power mode with VDD ON, a transition on CS is a wake-up condition
5	TXDC_I	CAN bus transmit data input. Internal pull-up to VDD
6	RXDC	CAN bus receive data output
7	I_WAKE_I	Active high input to enable on-board FET to create a 5.0 mA load on VDD
8	N/C	Not Connected
9	VDD	5.0/3.3 V output of the main regulator for the Microcontroller supply
10	INTB_I	This output is asserted low when an enabled interrupt condition occurs. The output is a push-pull structure
11	RSTB_I	This is the device reset output whose main function is to reset the MCU. It has an internal pull-up to VDD. The reset input voltage is also monitored in order to detect external reset and safe conditions
12	TXDL1	LIN1 bus transmit data input. Includes an internal pull-up resistor to VDD
13	RXDL1	LIN1 bus receive data output
14	TXDL2	LIN bus transmit data input. Includes an internal pull-up resistor to VDD
15	RXDL2	LIN2 bus receive data output
16	GND	Ground termination

6.6 Connector J2 – SPI Control

Pin #	Pin Name	Description
1	TXDC	CAN bus transmit data input. Internal pull-up to VDD
2	CSB	Chip select pin for the SPI. When the CS is low, the device is selected. In Low Power mode with VDD ON, a transition on CS is a wake-up condition
3	INTB	This output is asserted low when an enabled interrupt condition occurs. The output is a push-pull structure.
4	MISO	SPI data sent to the MCU. When the CS is high, MISO is high-impedance
5	RSTB	This is the device reset output whose main function is to reset the MCU. It has an internal pull-up to VDD. The reset input voltage is also monitored in order to detect external reset and safe conditions
6	MOSI	SPI data received by the device
7	NC	No Connect
8	SCLK	Clock input for the Serial Peripheral Interface (SPI) of the device
9	NC	No Connect
10	NC	No Connect
11	I_WAKE	Active high input to enable on-board FET to create a 5.0 mA load on VDD
12	NC	No Connect
13	NC	No Connect
14	NC	No Connect
15	NC	No Connect
16	GND	Ground termination

6.7 EVB – KITUSBSPIDGLEVME Interconnection

KIT33905D5EKEVBE/KIT33905BD3EVBE - J2		USB-to-SPI Dongle Board - I/O PORT	
Pin #	Pin Name	Pin Name	Pin #
1	TXDC	CNTL2	2
2	CSB	CSB	1
3	INTB	CNTL1	4
4	MISO	SO	3
5	RSTB	CNTL0	6
6	MOSI	SI	5
7	NC	DATA4	8
8	SCLK	SCLK	7
9	NC	DATA3	10
10	NC	CNTL3	9
11	I_WAKE	DATA2	12
12	NC	VDD	11
13	NC	DATA1	14
14	NC	REG 3.3V	13
15	NC	DATA0	16
16	GND	GND	15

7 Using the EVB

1. Select Install SPIGen (setup.exe) from the CD33905 Start page and follow the on-screen installation instructions.
2. Connect power supply to the VBAT and GND terminals on the EVB and build the setup as shown on Figure 2.
3. Ensure the voltages provided are in accordance with the device data sheet and that the supply currents are sufficient to supply the device.
4. To use SPIGen, go to the Windows **Start** menu > **Programs** > **SPIGen** and click on the **SPIGen** icon. The **SPIGen Generic SPI Generator** GUI will appear.
5. Go to the **Configure** menu in the upper left hand corner of the GUI and select **Edit Configuration**.
6. Select the **Enable 33905 Tab** in the **Part Specific Tabs** section on the lower right hand corner of the GUI and click **OK** button.
7. Select the **SBC MC3390x Family** tab.

7.1 Using SPIGen with the MC33905 Product

Evaluating all capabilities of the MC33905 product is made easy with the included SPIGen and respective GUI configuration file.

7.1.1 Sending Commands to Read Flags Set on SBC

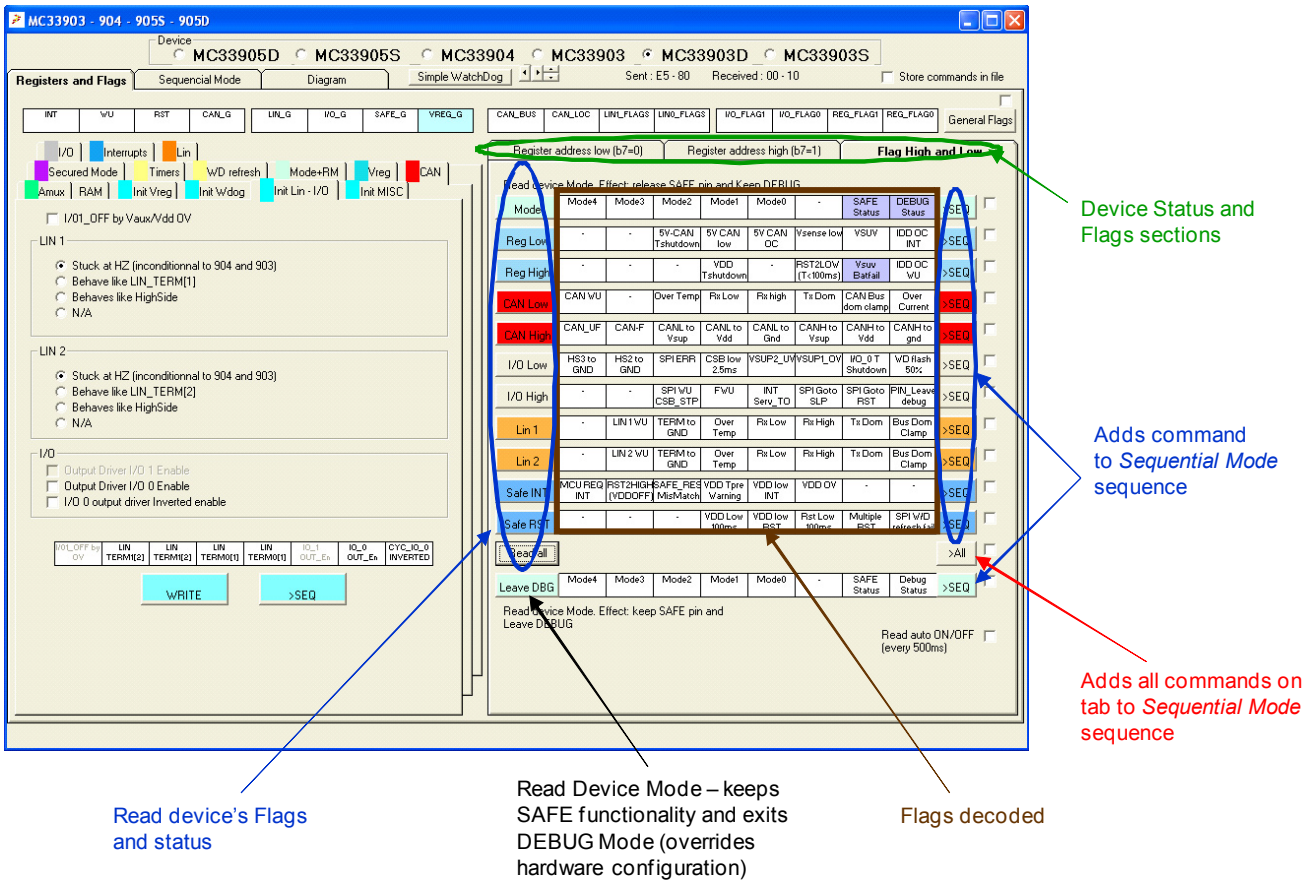

Figure 5. SPIGen Graphical User Interface (Commands and Flags Decoded)

1. In the **Registers and Flags** tab, click **Flag High and Low** sub tab to read the device status and clear flags as shown in Figure 5.
2. Click any of the read device flag status options.
3. Click **SEQ** to add commands to the Sequential Mode window.

7.1.2 Reading and Writing Commands to Exercise SBC and Acquire Its Status

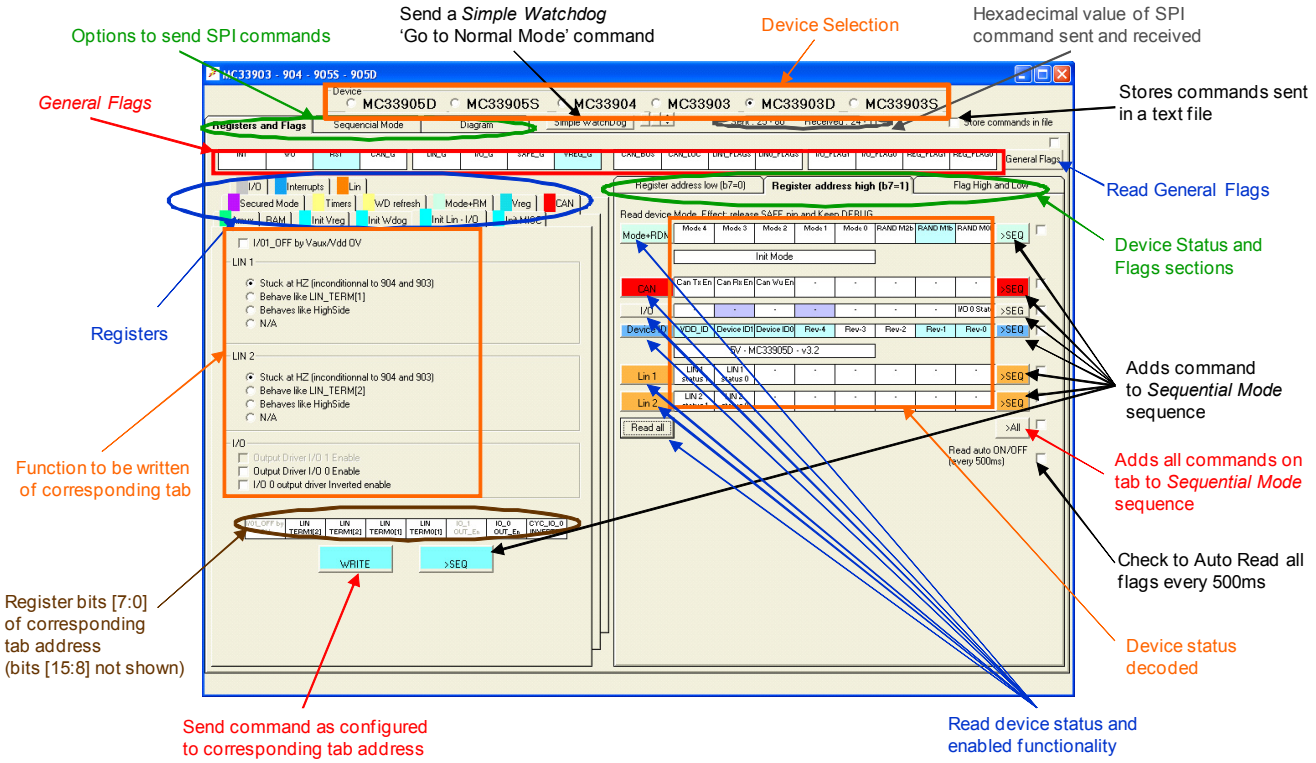

Figure 6. SPIGen Graphical User Interface (Commands and Device Status)

1. In the **Registers and Flags** tab, click **Register address high (b7=1)** sub tab to read device status and enabled functionality as shown in Figure 6.
2. Initialize the registers by clicking one of the options **Init Vreg** / **Init Wdog** / **Init Lin-I/O** / **Init MISC** and then click **WRITE**.
3. Click **WD Refresh** to go to Normal mode and then click **Single WD Write Command**.
4. Click **Mode+RM** to go to low power mode and then click **WRITE**.

7.1.3 Sending Commands to Acquire the Configuration of the SBC

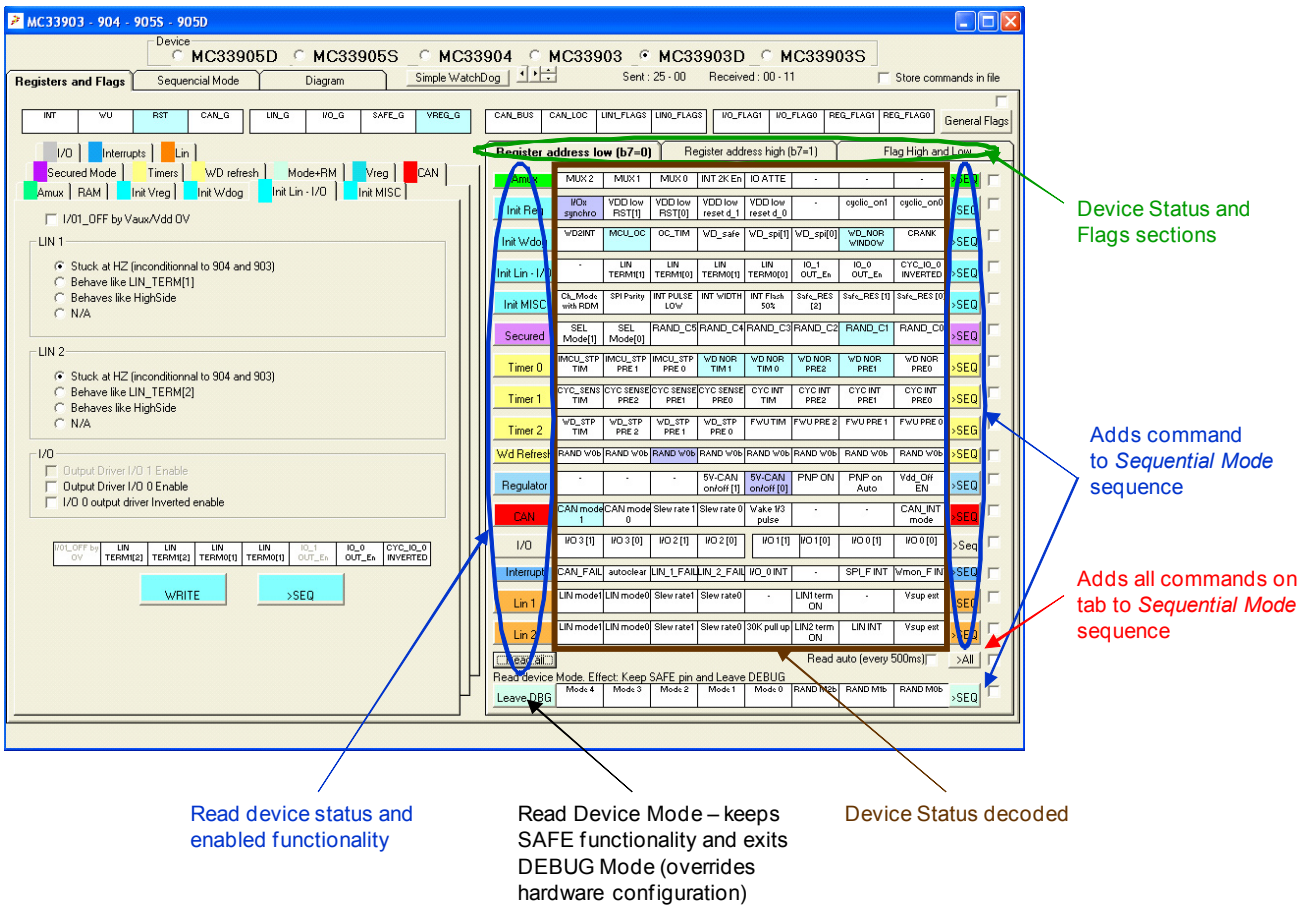

Figure 7. SPIGen Graphical User Interface (Commands and Device Configuration)

1. In the **Registers and Flags** tab, click **Register address low (b7=0)** sub tab as shown in Figure 7.
2. Click any of the read device flag status options.
3. Click **SEQ** to add commands to the Sequential Mode window.

7.1.4 Sequential Mode

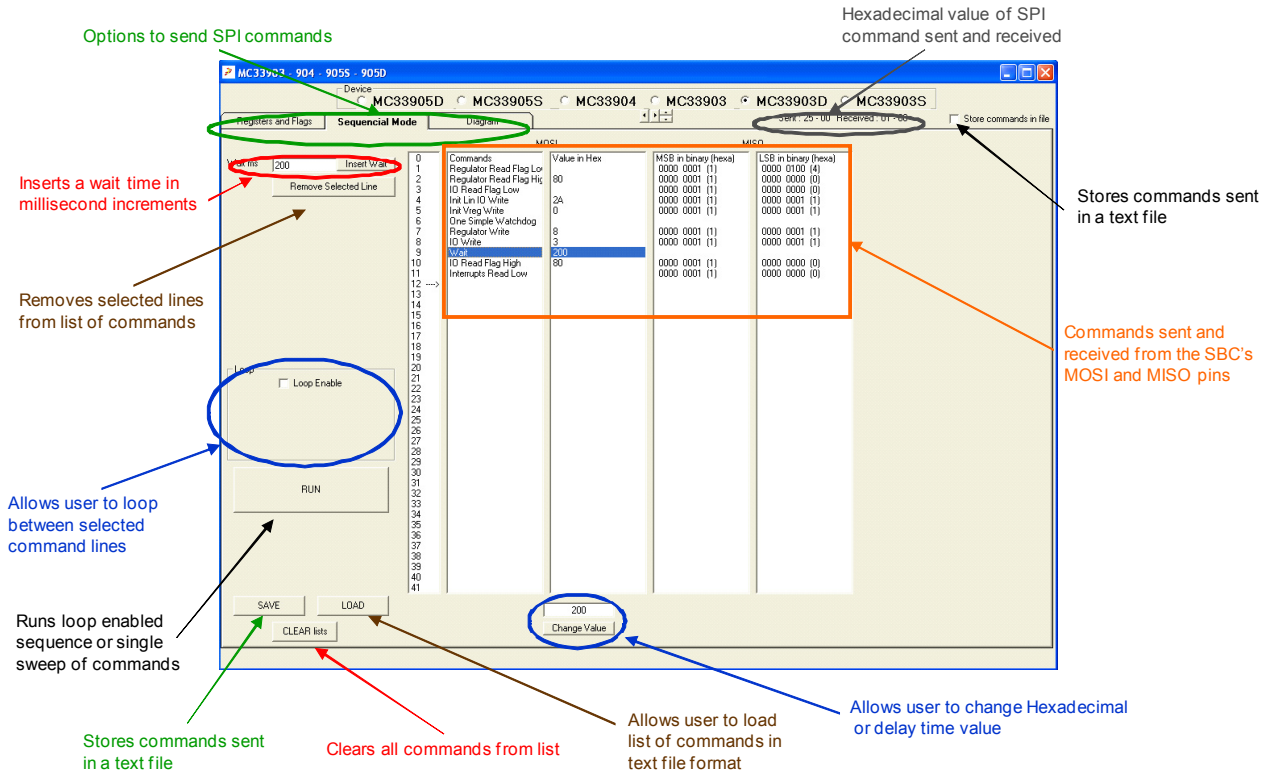

Figure 8. SPIGen Graphical User Interface (Sequential Mode)

1. Click **Sequential Mode** tab. This window displays all commands in the Sequential Mode sequence as shown in Figure 8.
2. In the **Insert Wait** text box, enter a wait time in millisecond increments.
3. Click **Remove Selected Line** to remove selected lines from the list of commnads.
4. Select **Loop Enable** option to allow loop between selected lines.
5. Click **Run** to activate the loop enabled sequence or single sweep of commands.
6. Click **Save** to store commands sent in a text file.
7. Click **Load** to load list of commands in text file format.
8. Click **Clear lists** to clear all commands from the list.
9. Enter a value in the text box and click **Change Value** to change the hexadecimal or the delay time value.

7.1.5 Automated State Diagram Mode

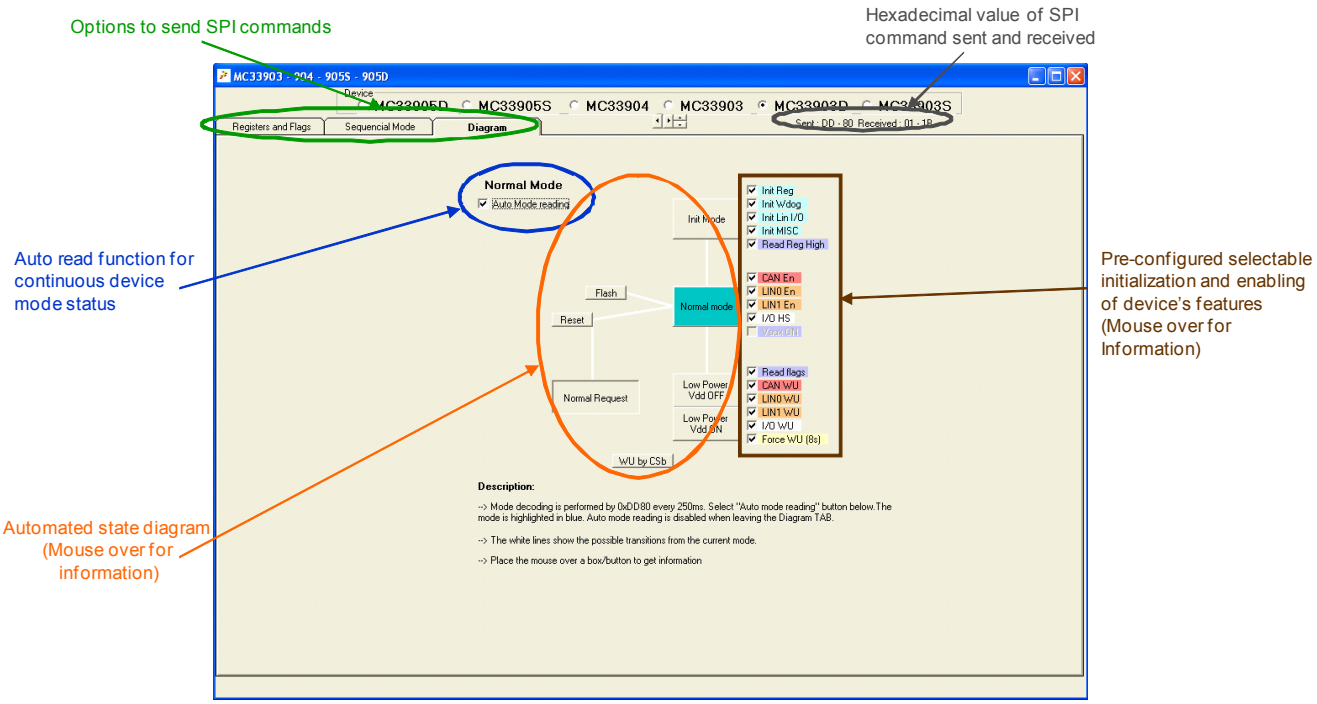

Figure 9. SPIGen Graphical User Interface (Automated State Diagram Mode)

1. Click **Diagram** tab.
2. Select **Normal Mode** option to enable auto read function for continuous device mode status as shown in Figure 9.
3. Click **Init Mode** to initialize selected registers.
4. Click **Normal Mode** to go to normal mode and enable selected registers.
5. Click **Low Power Vdd OFF/ON** to go to low power mode with selected wake ups.

8 Schematic Drawing

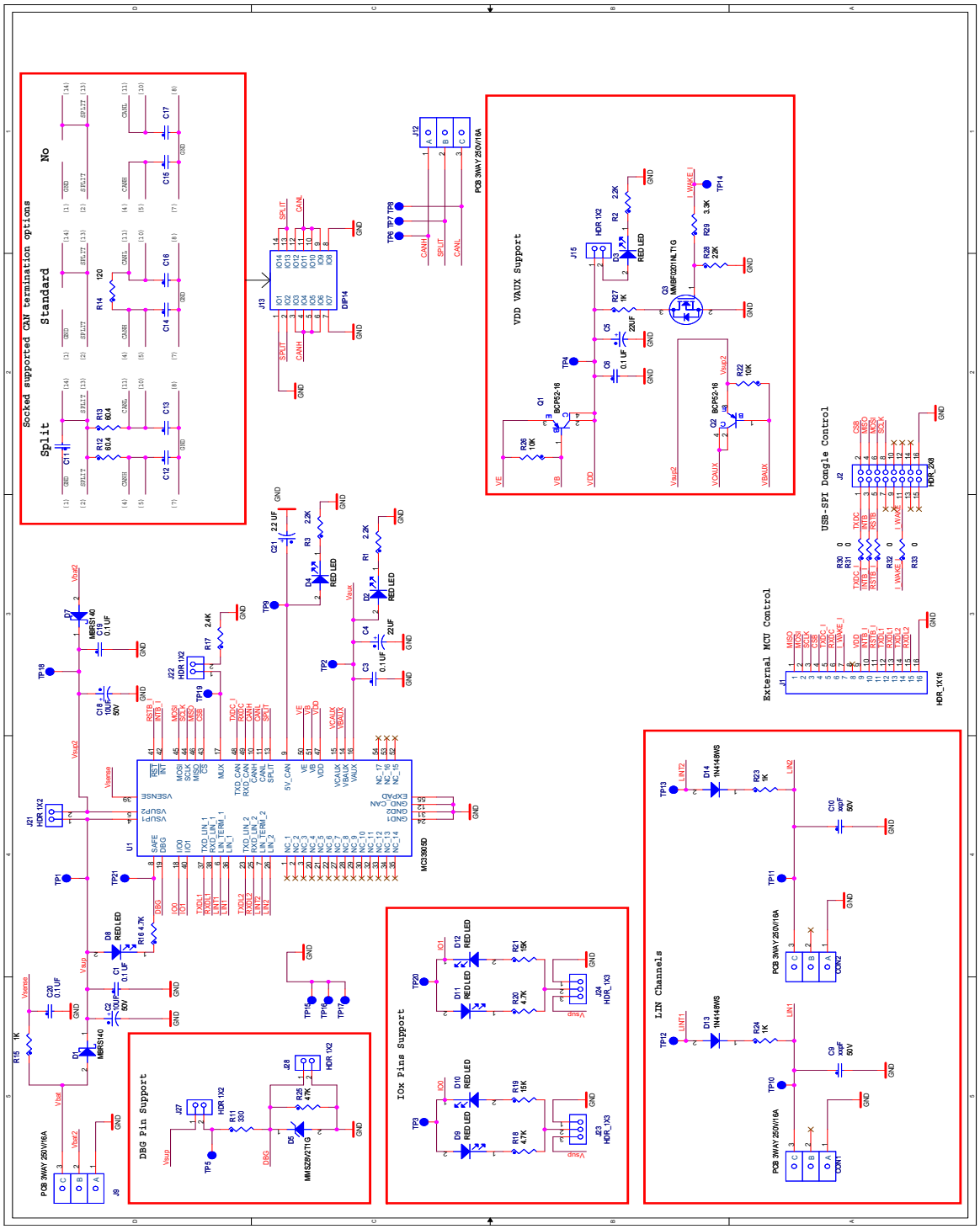

Figure 10. Schematic Drawing

9 Board Layout

9.1 Assembly Drawing

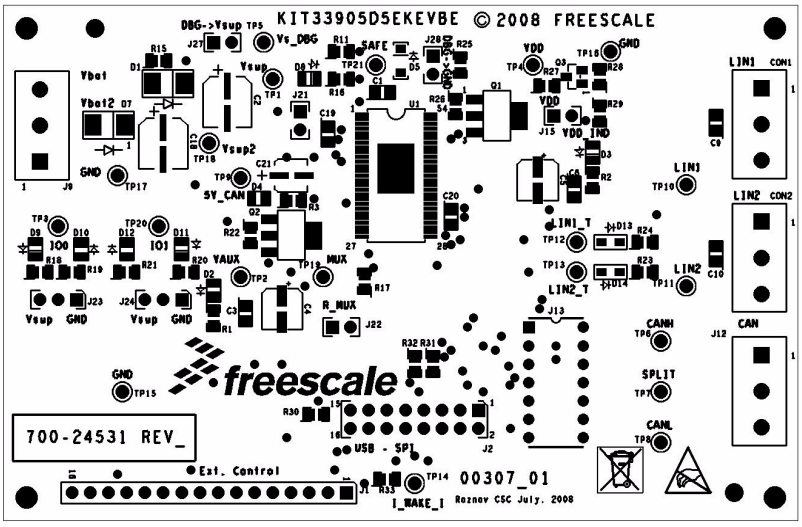

Figure 11. Assembly Drawing

9.2 Top Side Layer

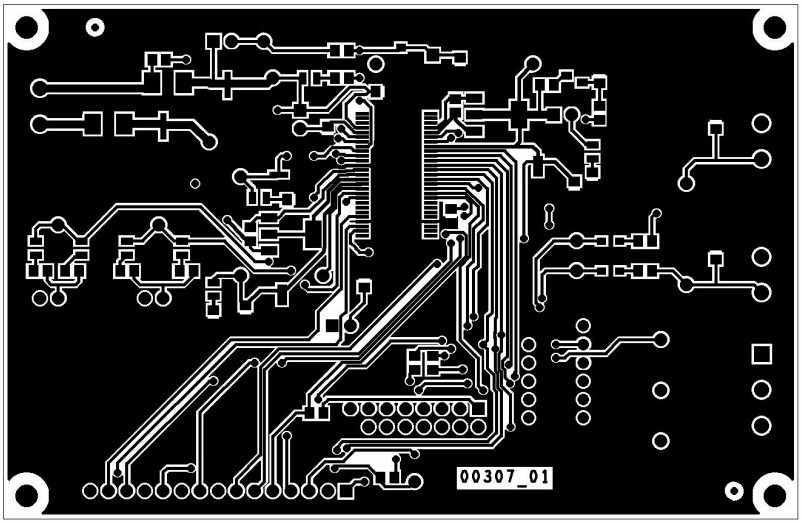

Figure 12. Top Side Layer

9.3 Bottom Side Layer

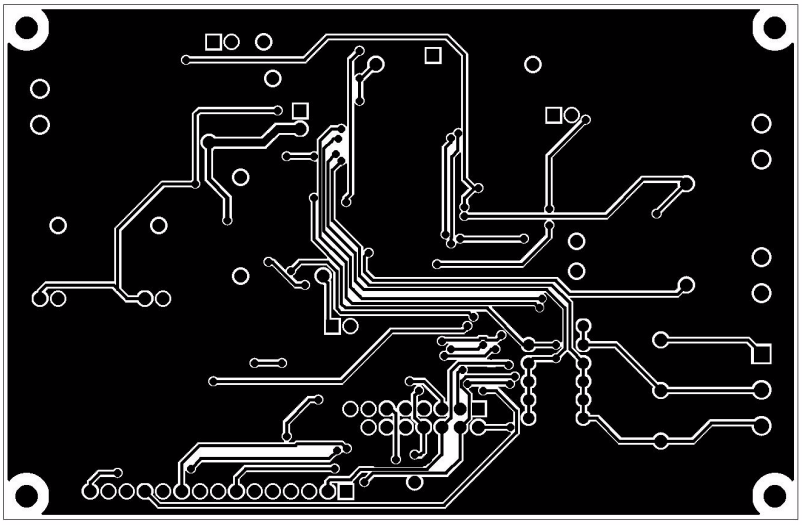

Figure 13. The Bottom Side Layer

10 Evaluation Board Bill of Material

Item	Qty	Schematic Label	Value	Description	Vender	Mfg. PN
1	4	CON1, CON2, J9, J12	PCB 3WAY 250V/16A	CON 3 TB TH 5MM SN	CAMDEN ELEC-TRONICS LTD	CTB5000/3
2	5	C1, C3, C6, C19, C20	0.1 UF	CAP CER 0.1UF 50V 10% X7R 0805	KEMET	C0805C104K5RAC
3	2	C2, C18	10UF	CAP ALEL 10UF 50V 20% SMT (CASE D)	PANASONIC	EEE1HA100SP
4	2	C4, C5	22UF	CAP ALEL 22UF 16V 20% -- CASE C SMT	PANASONIC	EEE1CA220SR
5	2	C9, C10	xxpF			
6	1	C11	1000PF	CAP CER 1000PF 50V 5% C0G 1206	AVX	12065A102JAT2A
7	6	C12, C13, C14, C15, C16, C17	56PF	CAP CER 56PF 50V 5% C0G 1206	KEMET	C1206C560J5GACTU
8	1	C21	2.2 UF	CAP ALEL 2.2UF 35V 20% -- SMT	PANASONIC	EEEFC1V2R2R
9	2	D1, D7	MBRS140	DIODE SCH PWR RECT 1A 40V SMB	ON SEMICONDUC-TOR	MBRS140T3G
10	8	D2, D3, D4, D8, D9, D10, D11, D12	RED LED	LED RED SGL 30MA SMT 0805	LUMEX	SML-LXT0805IW-TR
11	1	D5	MMSZ8V2T1G	DIODE ZNR -- 0.5W 8.2V SOD123	ON SEMICONDUC-TOR	MMSZ8V2T1G
12	2	D13, D14	1N4148WS	DIODE SW 150MA 53V SOD-323	DIODES INC	1N4148WS-7-F
13	1	J1	HDR_1X16	HDR 1X16 TH 100MIL SP 330H AU	SAMTEC	TSW-116-07-S-S
14	1	J2	HDR_2X8	HDR 2X8 TH 100MIL CTR 330H AU	SAMTEC	TSW-108-07-G-D
15	1	J13	DIP14	SKT DIP 14 PINS TH	3M	ICE-143-S-TG30
16	5	J15, J21, J22, J27, J28	HDR 1X2	HDR 1X2 TH 100MIL SP 330H SN	SAMTEC	TSW-102-07-T-S
17	2	J23, J24	HDR_1X3	HDR 1X3 TH 100MIL SP 330H AU	SAMTEC	HTSW-103-07-S-S
18	2	Q1, Q2	BCP52-16	TRAN PNP PWR 1A 60V SOT-223	PHILIPS SEMICON-DUCTOR	BCP52-16
19	1	Q3	MMBF0201NLT1G	TRAN NMOS PWR 0.3A 20V SOT23	ON SEMICONDUC-TOR	MMBF0201NLT1G
20	3	R1, R2, R3	2.2K	RES MF 2.2K 1/8W 5% 0805	BOURNS	CR0805-JW-222ELF
21	1	R11	330	RES MF 330 OHM 1/8W 5% 0805	VISHAY INTER-TECHNOLOGY	CRCW0805330RJNEA
22	2	R12, R13	60.4	RES MF 60.4 1/10W 1% 0603	KOA SPEER	RK73H1JTTD60R4F
23	1	R14	120	RES MF 120 OHM 1/8W 5% 0805	KOA SPEER	RK73B2ATTD121J
24	3	R15, R23, R24	1K	RES TF 1.0K 1/8W 5% RC0805	BOURNS	CR0805JW102E
25	3	R16, R18, R20	4.7K	RES MF 4.7K 1/8W 5% 0805	VENKEL COMPANY	CR0805-8W-472JT
26	1	R17	2.4K	RES MF 2.4K 1/8W 1% 0805	YAGEO AMERICA	232273462402L
27	2	R19, R21	15K	RES MF 15K 1/8W 5% 0805	BOURNS	CR0805JW153ELF
28	2	R22, R26	10K	RES TF 10K 1/8W 5% RC0805	BOURNS	CR0805JW103E
29	1	R25	47K	RES TF 47K 1/8W 5% RC0805	BOURNS	CR0805JW473E
30	1	R27	1K	RES TF 1.00K 1/8W 1% RC0805	BOURNS	CR0805FX1001E
31	1	R28	22K	RES MF 22K 1/8W 5% 0805	BOURNS	CR0805-JW-223ELF
32	1	R29	3.3K	RES MF 3.3K 1/8W 5% 0805	BOURNS	CR0805-JW-332ELF
33	4	R30, R31, R32, R33	0	RES MF ZERO OHM 1/8W -- 0805	BOURNS	CR0805-J/-000ELF
34	21	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21	TEST POINT BLACK	TEST POINT PIN.100 X .45 BLACK TH	COMPONENTS CORPORATION	TP-105-01-00
Freescale IC						
35	**1**	**U1**	**MC33905D**	**IC XCVR CAN DUAL LIN 40-1000KBPS 4.4-40V SOIC54**	**FREESCALE SEMI-CONDUCTOR**	**MCZ33905BD5EK MCZ3905D5EK MCZ33905BD3EK**

Freescale does not assume liability, endorse or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their applications.

11 References

You can obtain information on other Freescale products and application solutions by going to the following URLs:

Description	URL
Data Sheet	www.freescale.com/files/analog/doc/data_sheet/MC33903_4_5.pdf
Fact Sheet	www.freescale.com/files/analog/doc/fact_sheet/MC33903_4_5FS.pdf
Application Note	www.freescale.com/files/analog/doc/app_note/AN3865.pdf
Errata	http://www.freescale.com/files/analog/doc/errata/MC33903_4_5ER.pdf
SPIGen	www.freescale.com/files/soft_dev_tools/software/device_drivers/SPI-Gen.html
Freescale's Web Site	www.freescale.com
Freescale's Analog Web Site	www.freescale.com/analog
Freescale's Power Management Web Site	www.freescale.com/powermanagement
Freescale's Automotive Applications Web Site	www.freescale.com/automotive

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

KT33905UG
Rev. 2.0
9/2011