I2C Bus/SMBus Repeater

Features

- 2 channel, bidirectional buffer
- I^2C-bus and SMBus compatible
- Operating supply voltage range of 2.3 V to 3.6 V
- Active HIGH repeater enable input
- Open-drain input/outputs
- Lock-up free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates Standard-mode and Fast-mode I^2C-bus devices and multiple masters
- Powered-off high-impedance I^2C-bus pins
- 5.5 V tolerant I^2C-bus and enable pins
- 0 Hz to 400 kHz clock frequency (the maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater)
- ESD protection exceeds 4KV HBM per JESD22-A114
- Package: MSOP-8, SOIC-8 and DFN2x3-8L

Description

The PI6ULS5V9515A is a CMOS integrated circuit intended for I^2C bus and SMBus systems applications. The device contains two identical bidirectional open-drain buffer circuits that enable I^2C and similar bus systems to be extended without degradation of system performance.

The PI6ULS5V9515A enables the system designer to isolate two halves of a bus for both voltage and capacitance, accommodating more I^2C devices or longer trace length. It also permits extension of the I^2C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus allowing two buses of 400 pF to be connected in an I^2C application.

The PI6ULS5V9515A has an EN pin to turn the drivers on and off. This can be used to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I^2C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I^2C-bus parts being enabled. The enable pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

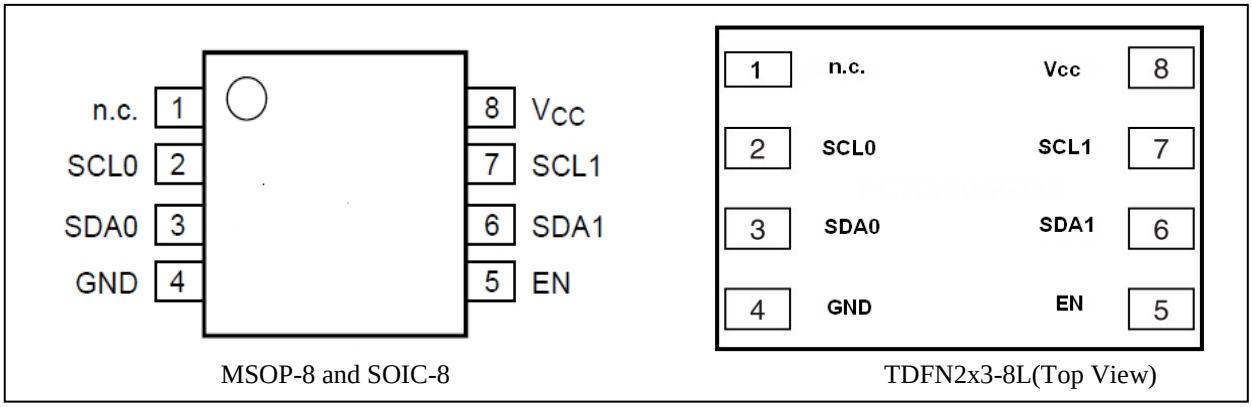
The output low levels for sides are approximately 0.5 V, but the input voltage of each internal buffer must be 70 mV lower (0.43V) or even more lower. When the output internally is driven low the low is not recognized as a low by the input.. This prevents a lockup condition from occurring when the input low condition is released.

Two or more PI6ULS5V9515A devices can't be used in series. The PI6ULS5V9515A design does not allow this configuration. Since there is no direction pin, slightly different valid low-voltage levels are used to avoid lockup conditions between the input and the output of each repeater. A valid low applied at the input of a PI6ULS5V9515A will be propagated as a buffered low with a slightly higher value on the output. When this buffered low is applied to another PI6ULS5V9515A-type device in series, the second device does not recognize it as a valid low and will not propagate it as a buffered low again.

The device contains a power-up control circuit that sets an internal latch to prevent the output circuits from becoming active until Vcc is at a valid level (Vcc = 2.3 V).

As with the standard I^2C system, pull-up resistors are required to provide the logic-high levels on the buffered bus. The PI6ULS5V9515A has standard open-collector configuration of the I^2C bus. The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. The device is designed to work with Standard mode and Fast mode I^2C devices in addition to SMBus devices. Standard mode I^2C devices only specify 3mA in a generic I^2C system, where Standard mode devices and multiple masters are possible. Under certain conditions, higher termination currents can be used.

Pin Configuration



MSOP-8 and SOIC-8 TDFN2x3-8L(Top View)

Pin Description

Pin No	Name	Description
1	n.c.	Not connected
2	SCL0	serial clock port 0 bus
3	SDA0	serial data port 0 bus
4	GND	supply ground (0 V)
5	EN	active HIGH repeater enable input
6	SDA1	serial data port 1 bus
7	SCL1	serial clock port 1 bus
8	V_{CC}	supply voltage (2.3 V to 3.6 V)

Block Diagram

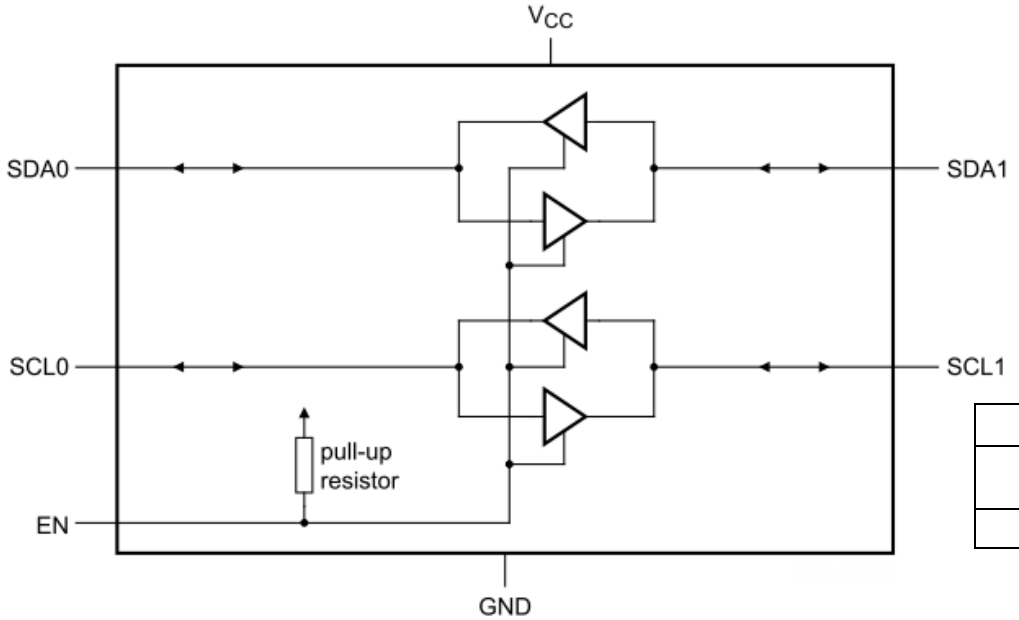


Figure 1:Block Diagram

EN	Function
H	SCL0 = SCL1; SDA0 = SDA1;
L	disabled

Maximum Ratings

Storage Temperature	-55°C to +125°C
DC Input Voltage	-0.5V to +6.0V
Control Input Votage(EN)	-0.5V to+6.0V
Total Power Dissipation	100mA
Input/Output Current (portA&B)	50mA
Input Current (EN, $V_{CC(A)}$, $V_{CC(B)}$, GND)	50mA
ESD: HBM Mode	4000V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

V_{CC} = 2.3 V to 3.6 V; GND = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vcc	supply voltage port	-	2.3	-	3.6	V
I_{CCH}	HIGH-level supply current	both channels HIGH;; SDAn = SCLn = V_{CC} V_{CC} = 2.7 V	-	0.5	5	mA
		both channels HIGH;; SDAn = SCLn = V_{CC} V_{CC} = 3.6 V	-	0.5	5	mA
I_{CCL}	LOW-level supply current	both channels LOW; V_{CC} = 2.7 V; one SDA and one SCL = GND; other SDA and SCL open	-	1.6	5	mA
		both channels LOW; V_{CC} = 3.6 V; one SDA and one SCL = GND; other SDA and SCL open	-	1.7	5	mA
I_{CCLC}	contention port A supply current	V_{CC} = 2.7V or 3.6V; SDAn = SCLn = GND	-	1.6	5	mA

DC Electrical Characteristics

V_{CC} = 2.7 V to 5.5 V; GND = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified

Parameter	Description	Test Conditions[1]	Min.	Typ.[2]	Max.	Unit
Input and output SDAn and SCLn						
V_{IH}	HIGH-level input voltage	-	$0.7V_{CC}$	-	5.5	V
V_{IL} [1]	LOW-level input voltage	-	-0.5	-	+0.3Vcc	
V_{ILc}	Contention LOW-level input voltage	-	-0.5	0.4	-	
V_{IK}	Input clamping voltage	I_I = -18 mA	-	-	-1.2	V
I_{LI}	Input leakage current	V_I = 3.6 V	-	-	±1	µA
I_{IL}	LOW-level input current	Vcc=2.3-2.7V ; SDA, SCL; V_I = 0.2 V	-	-	10	µA
		Vcc=3.0-3.6V ; SDA, SCL; V_I = 0.2 V	-	-	5	µA
V_{OL}	LOW-level output voltage	I_{OL} = 20 µA or 6 mA	0.47	0.52	0.6	V
V_{OL}-V_{ILc}	Difference between LOW-level output and LOW-level input voltage contention	guaranteed by design	-	70	-	mV
I_{LOH}	HIGH-level output leakage current	V_O = 3.6 V			10	µA
Cio	input/output capacitance	V_I = 3 V or 0 V	-	6	-	pF
Enable						
V_{IH}	HIGH-level input voltage	-	2.0	-	5.5	V
V_{IL}	LOW-level input voltage	-	-0.5	-	+0.8	V
I_{IL}	LOW-level input current	V_I = 0.2 V	-	-10	-30	µA
I_{LI}	Input leakage current	V_I=Vcc	-1	-	+1	µA
Ci	Input capacitance	V_I = 3.0 V or 0 V	-	6	-	pF

Notes:

1 V_{IL} specification is for the first LOW level seen by the SDAB/SCLB lines. V_{IL}c is for the second and subsequent LOW levels seen by the SDAn/SCLn lines.

Dynamic characteristics

GND = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified. [(1)(2)]

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vcc=2.3-2.7V						
t_{PLH}	LOW-to-HIGH propagation delay	-	33	113	190	ns
t_{PHL}	HIGH-to-LOW propagation delay	-		82	130	ns
t_{TLH}	LOW-to-HIGH transition time	-	-	148	-	ns
t_{THL}	HIGH-to-LOW transition time	-	-	57	-	ns
t_{SU}	Set-up time	-	100	-	-	ns
t_H	Hold time	-	130	-	-	ns
Vcc=3.0-3.6V						
t_{PLH}	LOW-to-HIGH propagation delay	-	33	102	180	ns
t_{PHL}	HIGH-to-LOW propagation delay	-		68	120	ns
t_{TLH}	LOW-to-HIGH transition time	-	-	147	-	ns
t_{THL}	HIGH-to-LOW transition time	-	-	58	-	ns
t_{SU}	Set-up time	-	100	-	-	ns
t_H	Hold time	-	100	-	-	ns

Notes:
(1) Typical values taken at VCC = 3.3 V and Tamb = 25°C.
(2) Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times.

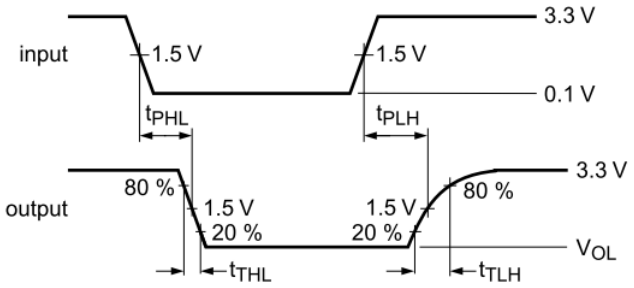
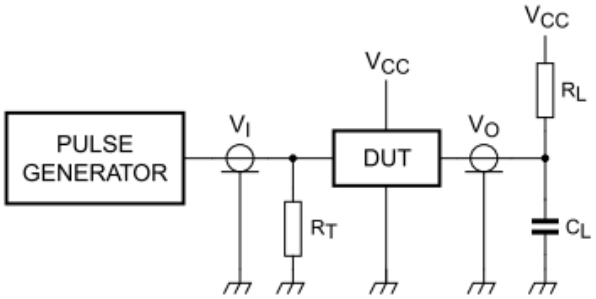


Figure 2: Propagation Delay and Transition Times



R_L = load resistor; 1.35 kΩ
C_L = load capacitance includes jig and probe capacitance; 50 pF
R_T = termination resistance should be equal to Z_o of pulse generators

Figure 3: Test Circuit

Functional Description

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Application Information

A typical application is shown in Figure 4. In this example, the system master is running on a 3.3 V I^2C-bus while the slave is connected to a 5V bus. Both buses run at 400 kHz. Master devices can be placed on either bus.

The PI6ULS5V9515A is 5V tolerant, so it does not require any additional circuitry to translate between different bus voltages.

When one side of the PI6ULS5V9515A is pulled LOW by a device on the I^2C-bus, a CMOS hysteresis type input detects the falling edge and causes the internal driver on the other side to turn on, thus causing the other side to also go LOW. The side driven LOW by the PI6ULS5V9515A will typically be at V_{OL} = 0.5 V.

Figure 5 and Figure 6 show the waveforms that are seen in a typical application. If the bus master in Figure4 writes to the slave through the PI6ULS5V9515A, Bus 0 has the waveform shown in Figure 5. This looks like a normal I^2C transmission until the falling edge of the eighth clock pulse. At that point, the master releases the data line (SDA) while the slave pulls it low through the PI6ULS5V9515A. Because the V_{OL} of the PI6ULS5V9515A typically is around 0.5V, a step in the SDA is seen. After the master has transmitted the ninth clock pulse, the slave releases the data line.

On the Bus 1 side of the PI6ULS5V9515A, the clock and data lines have a positive offset from ground equal to the V_{OL} of the PI6ULS5V9515A. After the eighth clock pulse, the data line is pulled to the V_{OL} of the slave device, which is very close to ground in the example.

It is important to note that any arbitration or clock-stretching events on Bus 1 require that the V_{OL} of the devices on Bus 1 be 70 mV below the V_{OL} of the PI6ULS5V9515A (see V_{OL} - V_{ILC} in Electrical Characteristics) to be recognized by the PI6ULS5V9515A and transmitted to Bus 0.

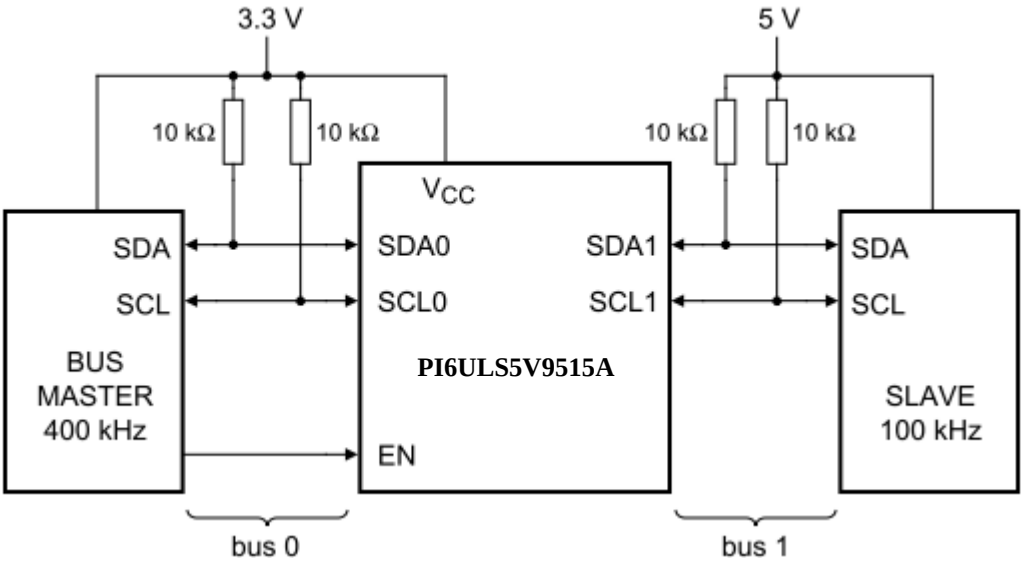


Figure 4: Typical Application

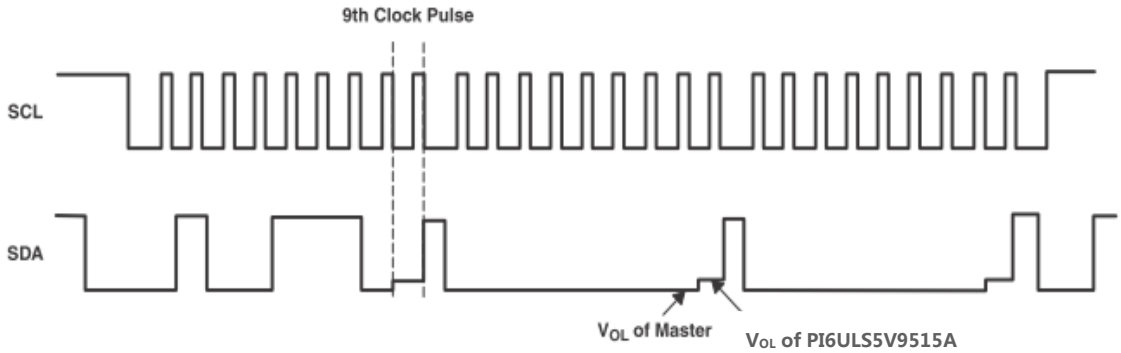


Figure 5: Bus 0 Waveforms

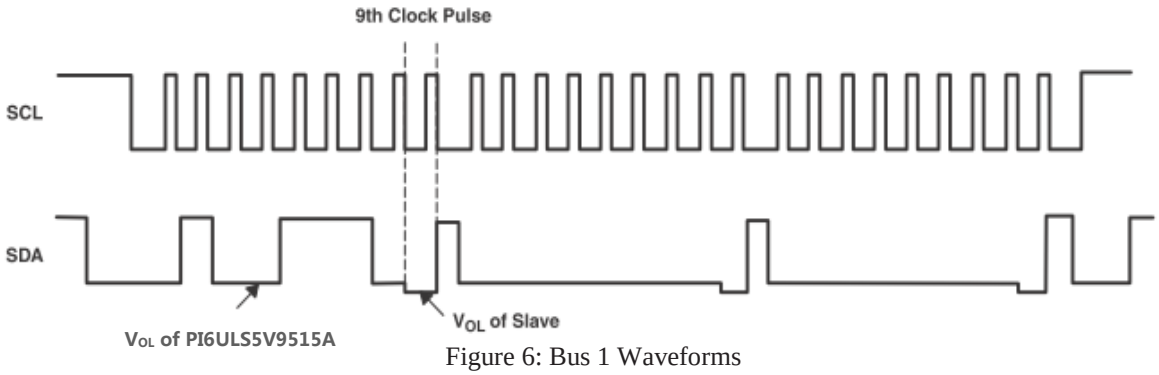
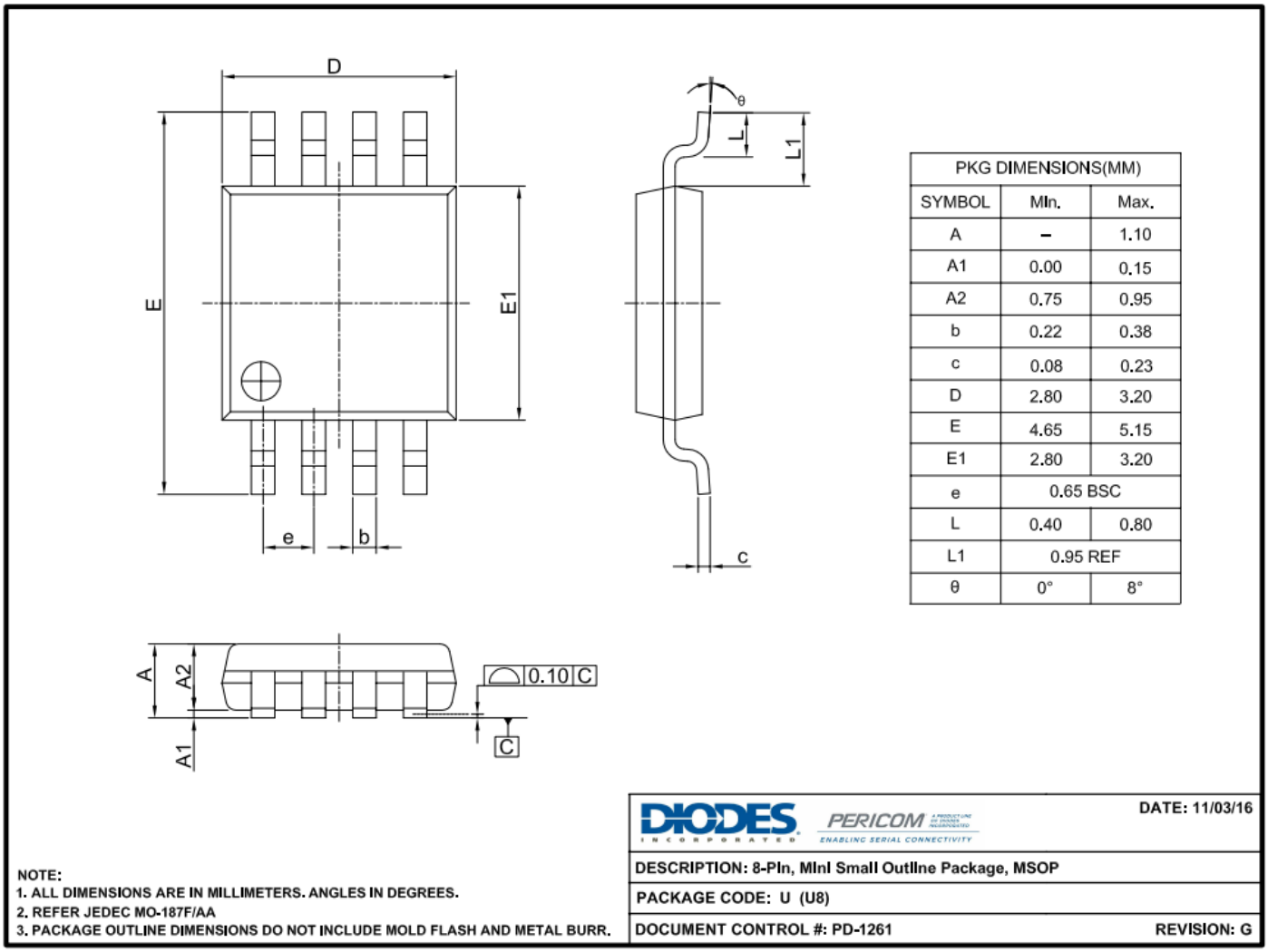


Figure 6: Bus 1 Waveforms

Mechanical Information

MSOP-8



PKG DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	–	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.80	3.20
E	4.65	5.15
E1	2.80	3.20
e	0.65 BSC	
L	0.40	0.80
L1	0.95 REF	
θ	0°	8°

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
2. REFER JEDEC MO-187F/AA
3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR.

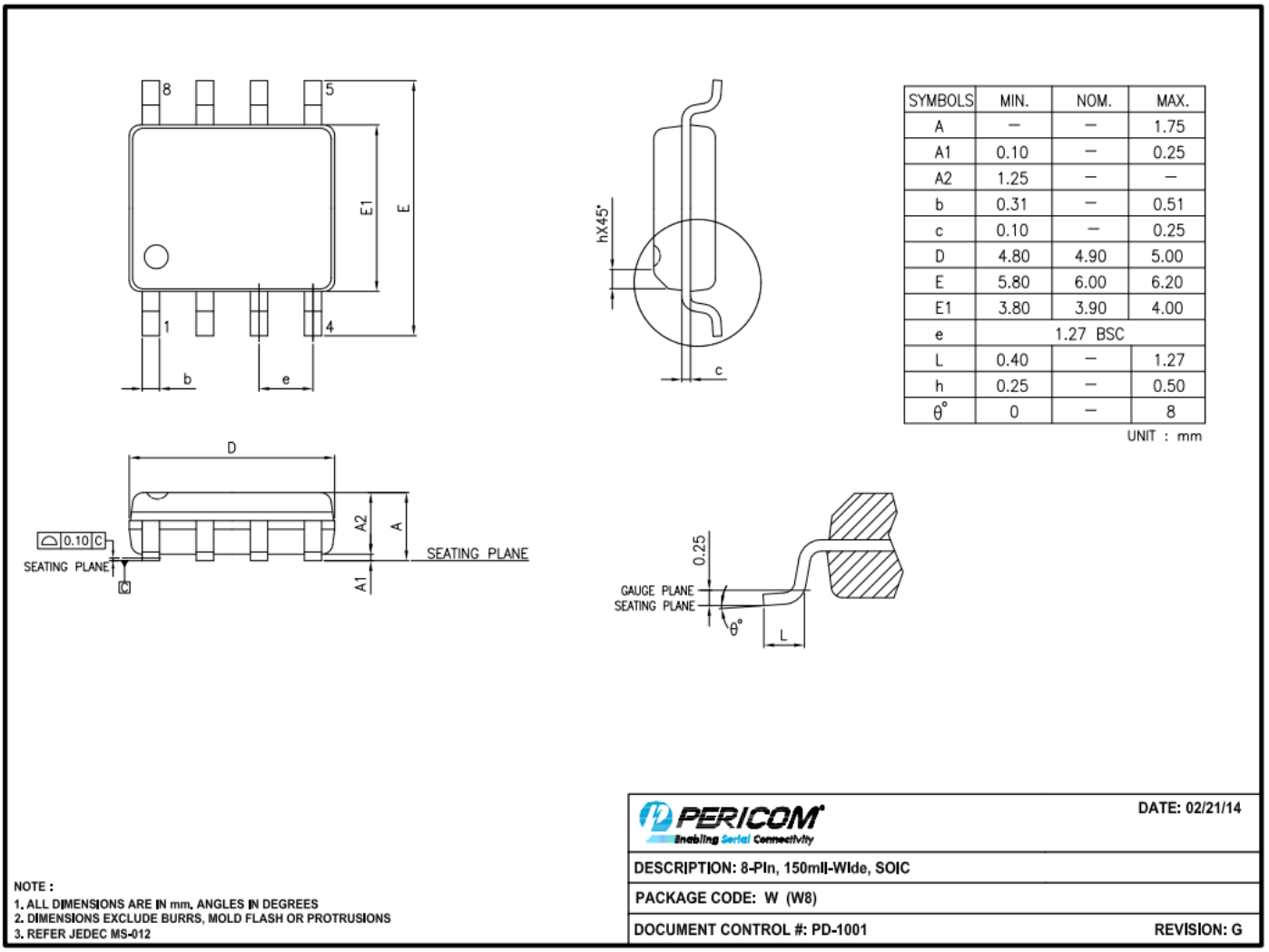
DATE: 11/03/16

DESCRIPTION: 8-Pin, Mini Small Outline Package, MSOP

PACKAGE CODE: U (U8)

DOCUMENT CONTROL #: PD-1261 REVISION: G

SOIC-8



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8

UNIT : mm

NOTE :
1. ALL DIMENSIONS ARE IN mm, ANGLES IN DEGREES
2. DIMENSIONS EXCLUDE BURRS, MOLD FLASH OR PROTRUSIONS
3. REFER JEDEC MS-012

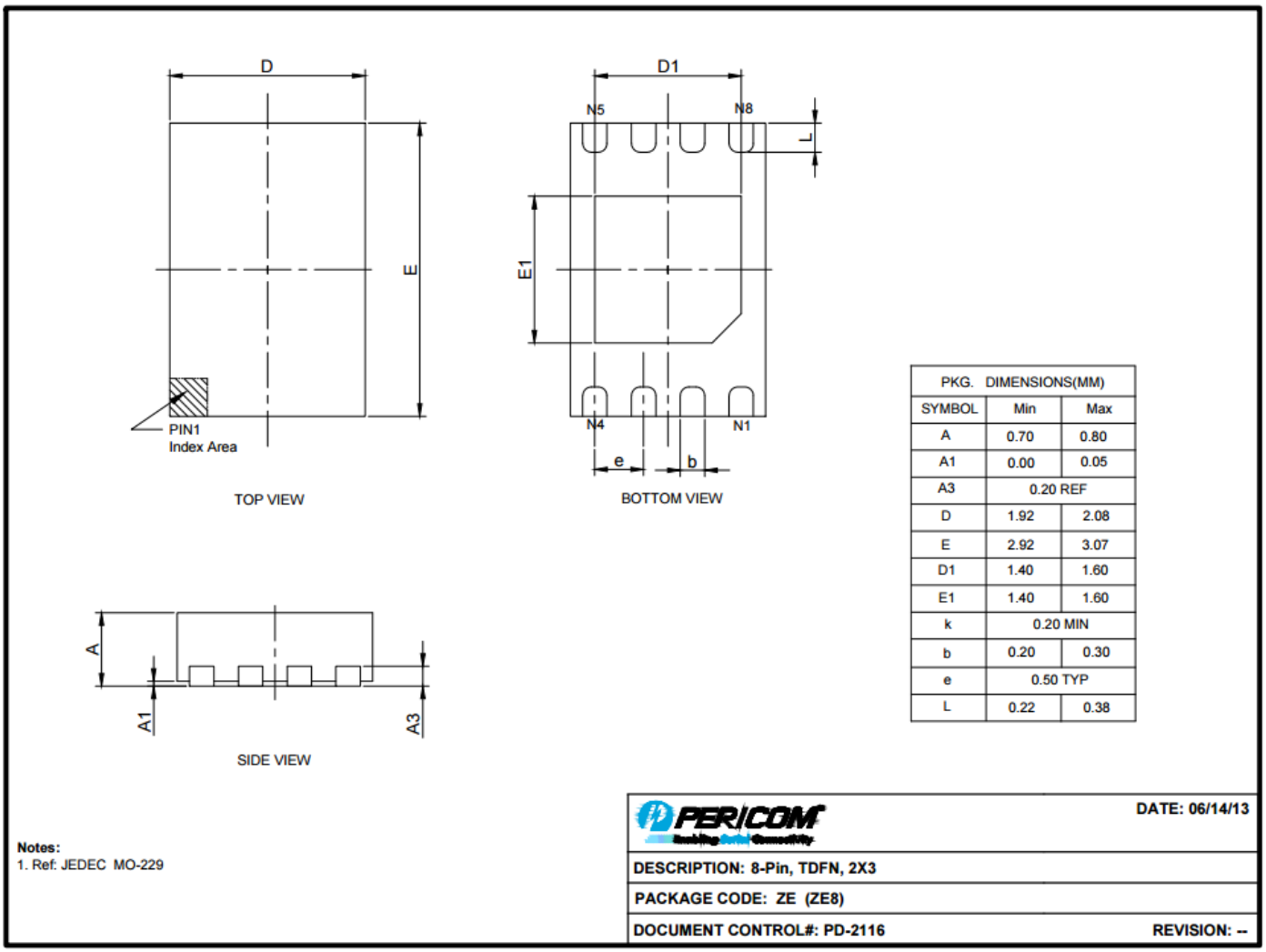
PERICOM Enabling Serial Connectivity — DATE: 02/21/14

DESCRIPTION: 8-Pin, 150mil-Wide, SOIC

PACKAGE CODE: W (W8)

DOCUMENT CONTROL #: PD-1001 — REVISION: G

TDFN2x3-8L



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
D	1.92	2.08
E	2.92	3.07
D1	1.40	1.60
E1	1.40	1.60
k	0.20 MIN	
b	0.20	0.30
e	0.50 TYP	
L	0.22	0.38

Notes:
1. Ref: JEDEC MO-229

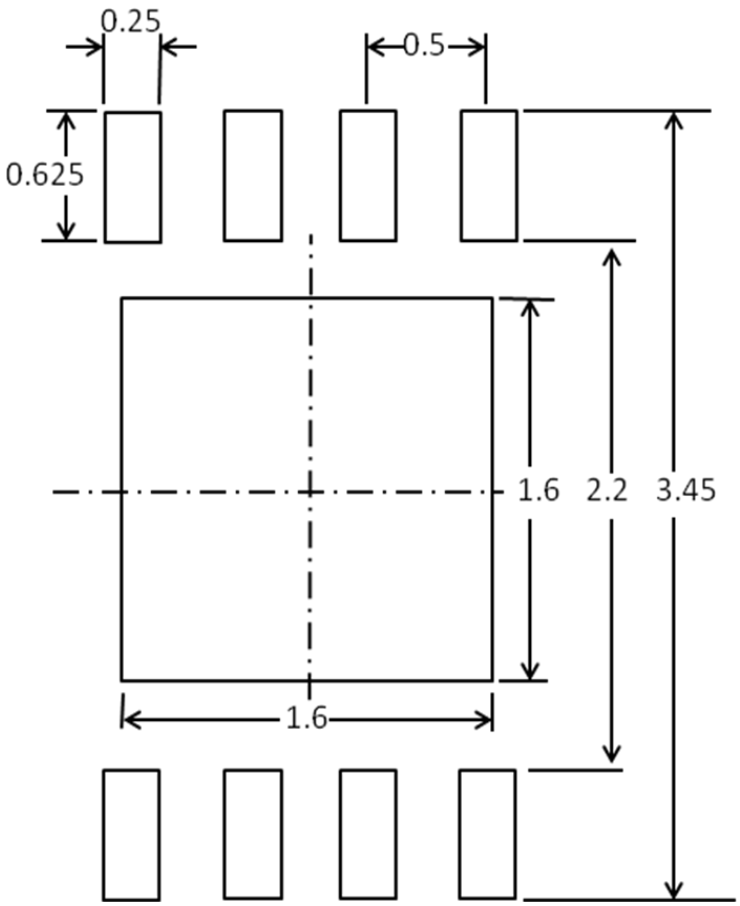
PERICOM Semiconductor Corporation — **DATE: 06/14/13**

DESCRIPTION: 8-Pin, TDFN, 2X3

PACKAGE CODE: ZE (ZE8)

DOCUMENT CONTROL#: PD-2116 **REVISION: --**

Recommended Land pattern for TDFN2*3-8L



Note:
All linear dimensions are in millimeters

Ordering Information

Part No.	Package Code	Package
PI6ULS5V9515AUE	U	8-pin, Mini Small Outline Package (MSOP)
PI6ULS5V9515AUEX	U	8-pin, Mini Small Outline Package (MSOP), Tape & Reel
PI6ULS5V9515AWE	W	8-pin, 150mil-Wide (SOIC)
PI6ULS5V9515AWEX	W	8-pin, 150mil-Wide (SOIC), Tape & Reel
PI6ULS5V9515AZEEX	ZE	8-pin, 2x3 (TDFN), Tape & Reel

Note:
- E = Pb-free
- Adding X Suffix= Tape/Reel

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B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

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