Dual, 12-Bit + Sign, 5Msps Differential Input ADC with Wide Input Common Mode Range

FEATURES

- **5Msps Throughput Rate**
- **±0.5LSB INL (Typ)**
- **Guaranteed 12-Bit, No Missing Codes**
- **8V$_{P-P}$ Differential Inputs with Wide Input Common Mode Range**
- **73dB SNR (Typ) at f$_{IN}$ = 2MHz**
- **–85dB THD (Typ) at f$_{IN}$ = 2MHz**
- Guaranteed Operation to 125°C
- Single 3.3V or 5V Supply
- Low Drift (20ppm/°C Max) 2.048V or 4.096V Internal Reference
- 1.8V to 2.5V I/O Voltages
- CMOS or LVDS SPI-Compatible Serial I/O
- Power Dissipation 38mW/Ch (Typ)
- Small 28-Lead (4mm × 5mm) QFN Package

APPLICATIONS

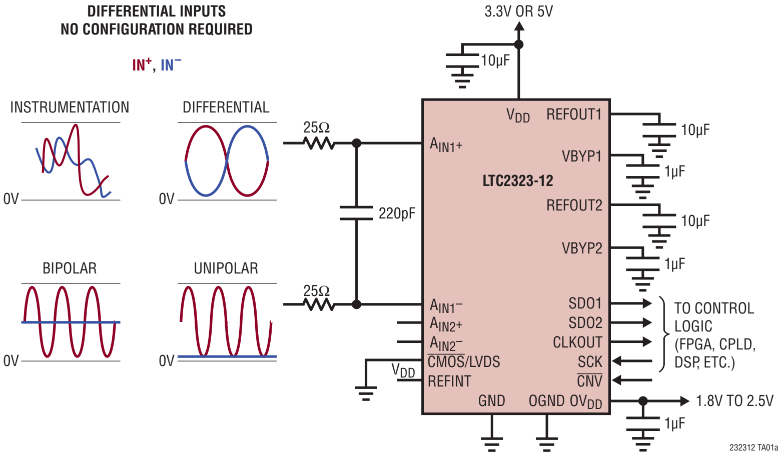
- High Speed Data Acquisition Systems
- Communications
- Remote Data Acquisition
- Imaging
- Optical Networking
- Automotive
- Multiphase Motor Control

DESCRIPTION

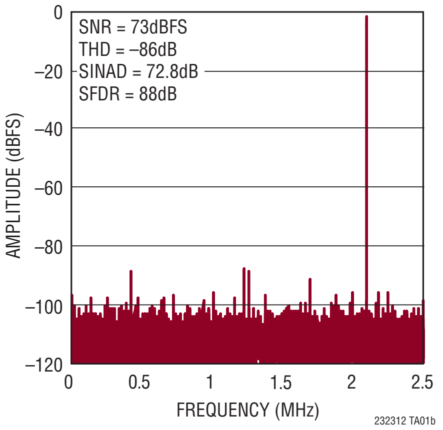
The LTC®2323-12 is a low noise, high speed dual 12-bit + sign successive approximation register (SAR) ADC with differential inputs and wide input common mode range. Operating from a single 3.3V or 5V supply, the LTC2323-12 has an 8V$_{P-P}$ differential input range, making it ideal for applications which require a wide dynamic range with high common mode rejection. The LTC2323-12 achieves ±0.5LSB INL typical, no missing codes at 12 bits and 73dB SNR.

The LTC2323-12 has an onboard low drift (20ppm/°C max) 2.048V or 4.096V temperature-compensated reference. The LTC2323-12 also has a high speed SPI-compatible serial interface that supports CMOS or LVDS. The fast 5Msps per channel throughput with one-cycle latency makes the LTC2323-12 ideally suited for a wide variety of high speed applications. The LTC2323-12 dissipates only 38mW per channel and offers nap and sleep modes to reduce the power consumption to 5μW for further power savings during inactive periods.

TYPICAL APPLICATION



16k Point FFT f_S = 5Msps, f_{IN} = 2.2MHz

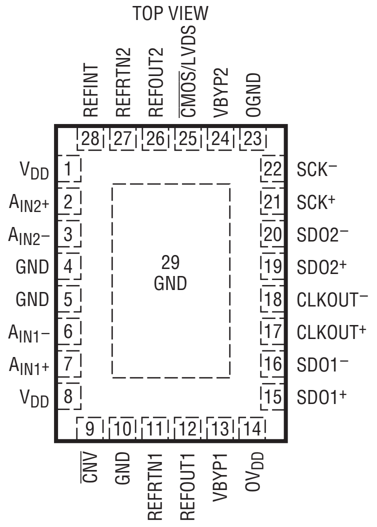


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD})	6V
Supply Voltage (OV_{DD})	3V
Supply Bypass Voltage (V_{BYP1}, V_{BYP2})	3V
Analog Input Voltage	
A_{IN+}, A_{IN-} (Note 3)	–0.3V to (V_{DD} + 0.3V)
REFOUT1,2	–0.3V to (V_{DD} + 0.3V)
$\overline{\text{CNV}}$ (Note 15)	–0.3V to (V_{DD} + 0.3V)
Digital Input Voltage	
(Note 3)	(GND – 0.3V) to (OV_{DD} + 0.3V)
Digital Output Voltage	
(Note 3)	(GND – 0.3V) to (OV_{DD} + 0.3V)
Power Dissipation	200mW
Operating Temperature Range	
LTC2323C	0°C to 70°C
LTC2323I	–40°C to 85°C
LTC2323H	–40°C to 125°C
Storage Temperature Range	–65°C to 150°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION http://www.linear.com/product/LTC2323-12#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2323CUFD-12#PBF	LTC2323CUFD-12#TRPBF	23232	28-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC2323IUFD-12#PBF	LTC2323IUFD-12#TRPBF	23232	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C
LTC2323HUFD-12#PBF	LTC2323HUFD-12#TRPBF	23232	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN+}	Absolute Input Range (A_{IN1+}, A_{IN2+})	(Note 5)	●	0		V_{DD}	V
V_{IN-}	Absolute Input Range (A_{IN1-}, A_{IN2-})	(Note 5)	●	0		V_{DD}	V
$V_{IN+} – V_{IN-}$	Input Differential Voltage Range	$V_{IN} = V_{IN+} – V_{IN-}$	●	–REFOUT1,2		REFOUT1,2	V
V_{CM}	Common Mode Input Range	$V_{IN} = (V_{IN+} + V_{IN-})/2$	●	0		V_{DD}	V
I_{IN}	Analog Input DC Leakage Current		●	–1		1	µA
C_{IN}	Analog Input Capacitance				10		pF
CMRR	Input Common Mode Rejection Ratio	f_{IN} = 2.2MHz			85		dB
I_{REFOUT}	External Reference Current	REFINT = 0V, REFOUT = 4.096V			675		µA

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Notes 4, 16).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution		●	12			Bits
	No Missing Codes		●	12			Bits
	Transition Noise				0.2		LSB_{RMS}
INL	Integral Linearity Error	(Note 6)	●	–1	±0.5	1	LSB
DNL	Differential Linearity Error		●	–0.99	±0.4	0.99	LSB
BZE	Bipolar Zero-Scale Error	(Note 7)	●	–3	0	3	LSB
	Bipolar Zero-Scale Error Drift				0.0015		LSB/°C
FSE	Bipolar Full-Scale Error	$V_{REFOUT1,2}$ = 4.096V (REFINT Grounded) (Note 7)	●	–20	±3	20	LSB
	Bipolar Full-Scale Error Drift	$V_{REFOUT1,2}$ = 4.096V (REFINT Grounded)			15		ppm/°C

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and A_{IN} = –1dBFS (Notes 4, 8).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	f_{IN} = 2.2MHz, $V_{REFOUT1,2}$ = 4.096V, Internal Reference	●	69.8	72.9		dB
		f_{IN} = 2.2MHz, $V_{REFOUT1,2}$ = 5V, External Reference			73.2		dB
SNR	Signal-to-Noise Ratio	f_{IN} = 2.2MHz, $V_{REFOUT1,2}$ = 4.096V, Internal Reference	●	70	73		dB
		f_{IN} = 2.2MHz, $V_{REFOUT1,2}$ = 5V, External Reference			73.5		dB
THD	Total Harmonic Distortion	f_{IN} = 2.2MHz, $V_{REFOUT1,2}$ = 4.096V, Internal Reference	●		–85	–80	dB
		f_{IN} = 2.2MHz, $V_{REFOUT1,2}$ = 5V, External Reference			–84		dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 2.2MHz, $V_{REFOUT1,2}$ = 4.096V, Internal Reference	●	78	88		dB
		f_{IN} = 2.2MHz, $V_{REFOUT1,2}$ = 5V, External Reference			88		dB
	–3dB Input Linear Bandwidth				10		MHz
	Aperture Delay				500		ps
	Aperture Delay Matching				500		ps
	Aperture Jitter				1		ps_{RMS}
	Transient Response	Full-Scale Step			3		ns

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{REFOUT1,2}$	Internal Reference Output Voltage	4.75V < V_{DD} < 5.25V 3.13V < V_{DD} < 3.47V	● ●	4.088 2.044	4.096 2.048	4.106 2.053	V
	$V_{REFOUT1,2}$ Temperature Coefficient	(Note 14)	●		3	20	ppm/°C
	REFOUT1,2 Output Impedance				0.25		Ω
	$V_{REFOUT1,2}$ Line Regulation	V_{DD} = 4.75V to 5.25V			0.3		mV/V

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		●	$0.8 \bullet OV_{DD}$			V
V_{IL}	Low Level Input Voltage		●			$0.2 \bullet OV_{DD}$	V
I_{IN}	Digital Input Current	V_{IN} = 0V to OV_{DD}	●	–10		10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	I_O = -500µA	●	OV_{DD} – 0.2			V
V_{OL}	Low Level Output Voltage	I_O = 500µA	●			0.2	V
I_{OZ}	Hi-Z Output Leakage Current	V_{OUT} = 0V to OV_{DD}	●	–10		10	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = OV_{DD}			10		mA
V_{ID}	LVDS Differential Input Voltage	100Ω Differential Termination, OV_{DD} = 2.5V	●	240		600	mV
V_{IS}	LVDS Common Mode Input Voltage	100Ω Differential Termination, OV_{DD} = 2.5V	●	1		1.45	V
V_{OD}	LVDS Differential Output Voltage	100Ω Differential Load, LVDS Mode, OV_{DD} = 2.5V	●	100	150	300	mV
V_{OS}	LVDS Common Mode Output Voltage	100Ω Differential Load, LVDS Mode, OV_{DD} = 2.5V	●	0.85	1.2	1.4	V
V_{OD_LP}	Low Power LVDS Differential Output Voltage	100Ω Differential Load, Low Power, LVDS Mode ,OV_{DD} = 2.5V	●	75	100	200	mV
V_{OS_LP}	Low Power LVDS Common Mode Output Voltage	100Ω Differential Load, Low Power, LVDS Mode ,OV_{DD} = 2.5V	●	0.9	1.2	1.4	V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 4).

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage	5V Operation 3.3V Operation		● ●	4.75 3.13		5.25 3.47	V V
OV_{DD}	Supply Voltage			●	1.71		2.63	V
I_{VDD}	Supply Current	5Msps Sample Rate ($IN^+ = IN^- = 0V$)		●		14	18	mA
I_{OVDD}	Supply Current	5Msps Sample Rate (C_L = 5pF) 5Msps Sample Rate (R_L = 100Ω)	CMOS Mode LVDS Mode	● ●		2.8 9.5	5 12	mA mA
I_{NAP}	Nap Mode Current	Conversion Done (I_{VDD})		●		2.85	5	mA
I_{SLEEP}	Sleep Mode Current	Sleep Mode ($I_{VDD} + I_{OVDD}$) Sleep Mode ($I_{VDD} + I_{OVDD}$)	CMOS Mode LVDS Mode	● ●		1 1	5 5	µA µA
$P_{D\_3.3V}$	Power Dissipation	V_{DD} = 3.3V 5Msps Sample Rate ($IN^+ = IN^- = 0V$) V_{DD} = 3.3V 5Msps Sample Rate ($IN^+ = IN^- = 0V$)	CMOS Mode LVDS Mode	● ●		55 72	58 86	mW mW
	Nap Mode	V_{DD} = 3.3V Conversion Done ($I_{VDD} + I_{OVDD}$) V_{DD} = 3.3V Conversion Done ($I_{VDD} + I_{OVDD}$)	CMOS Mode LVDS Mode	● ●		9 32	13 41	mW mW
	Sleep Mode	V_{DD} = 3.3V Sleep Mode ($I_{VDD} + I_{OVDD}$) V_{DD} = 3.3V Sleep Mode ($I_{VDD} + I_{OVDD}$)	CMOS Mode LVDS Mode	● ●		5 5	16.5 16.5	µW µW
P_{D_5V}	Power Dissipation	V_{DD} = 5V 5Msps Sample Rate ($IN^+ = IN^- = 0V$) V_{DD} = 5V 5Msps Sample Rate ($IN^+ = IN^- = 0V$)	CMOS Mode LVDS Mode	● ●		76 105	100 110	mW mW
	Nap Mode	V_{DD} = 5V Conversion Done ($I_{VDD} + I_{OVDD}$) V_{DD} = 5V Conversion Done ($I_{VDD} + I_{OVDD}$)	CMOS Mode LVDS Mode	● ●		15 38	25 40	mW mW
	Sleep Mode	V_{DD} = 5V Sleep Mode ($I_{VDD} + I_{OVDD}$) V_{DD} = 5V Sleep Mode ($I_{VDD} + I_{OVDD}$)	CMOS Mode LVDS Mode	● ●		5 5	25 25	µW µW

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$ (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SMPL}	Maximum Sampling Frequency		●			5	Msps
t_{CYC}	Time Between Conversions	(Note 11)	●	200		1000000	ns
t_{CONV}	Conversion Time		●	161.9			ns
t_{CNVH}	$\overline{CNV}$ High Time		●	35			ns
$t_{DCNVSCKL}$	SCK Quiet Time from $\overline{CNV}$↓	(Note 11)	●	10			ns
$t_{DSCKLCNVH}$	SCK Delay Time to $\overline{CNV}$↑	(Note 11)	●	20			ns
t_{SCK}	SCK Period	(Notes 12, 13)	●	9.4			ns
t_{SCKH}	SCK High Time		●	4			ns
t_{SCKL}	SCK Low Time		●	4			ns
$t_{DSCKCLKOUT}$	SCK to CLKOUT Delay	(Note 12)	●	2.5			ns
$t_{DCLKOUTSDOV}$	SDO Data Valid Delay from CLKOUT↓	C_L = 5pF (Note 12)	●			2	ns
t_{HSDO}	SDO Data Remains Valid Delay from CLKOUT↓	C_L = 5pF (Note 11)	●			2	ns
$t_{DCNVSDOV}$	SDO Data Valid Delay from $\overline{CNV}$↓	C_L = 5pF (Note 11)	●		2.5	3	ns
$t_{DCNVSDOZ}$	Bus Relinquish Time After $\overline{CNV}$↑	(Note 11)	●			3	ns
t_{WAKE}	REFOUT1,2 Wakeup Time	$C_{REFOUT1,2}$ = 10µF			10		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground.

Note 3: When these pin voltages are taken below ground, or above V_{DD} or OV_{DD}, they will be clamped by internal diodes. This product can handle input currents up to 100mA below ground, or above V_{DD} or OV_{DD}, without latch-up.

Note 4: V_{DD} = 5V, OV_{DD} = 2.5V, REFOUT1,2 = 4.096V, f_{SMPL} = 5MHz.

Note 5: Recommended operating conditions.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Bipolar zero error is the offset voltage measured from –0.5LSB when the output code flickers between 0 0000 0000 0000 and 1 1111 1111 1111. Full-scale bipolar error is the worst-case of –FS or +FS un-trimmed deviation from ideal first and last code transitions and includes the effect of offset error.

Note 8: All specifications in dB are referred to a full-scale ±4.096V input with REFIN = 4.096V.

Note 9: When REFOUT1,2 is overdriven, the internal reference buffer must be turned off by setting REFINT = 0V.

Note 10: f_{SMPL} = 5MHz, I_{REFBUF} varies proportionally with sample rate.

Note 11: Guaranteed by design, not subject to test.

Note 12: Parameter tested and guaranteed at OV_{DD} = 1.71V and OV_{DD} = 2.5V.

Note 13: t_{SCK} of 9.4ns maximum allows a shift clock frequency up to 105MHz for rising edge capture.

Note 14: Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

Note 15: $\overline{CNV}$ is driven from a low jitter digital source, typically at OV_{DD} logic levels. This input pin has a TTL style input that will draw a small amount of current.

Note 16: 1LSB = 2 • REFOUT1,2/2^{12}

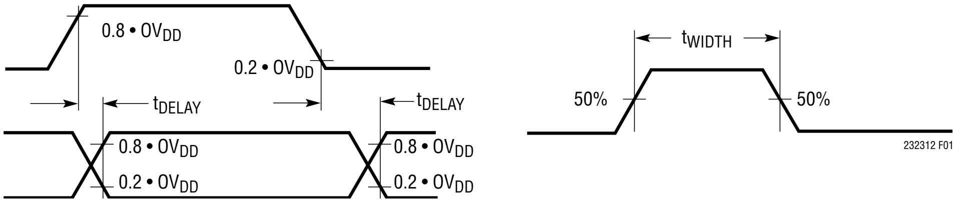
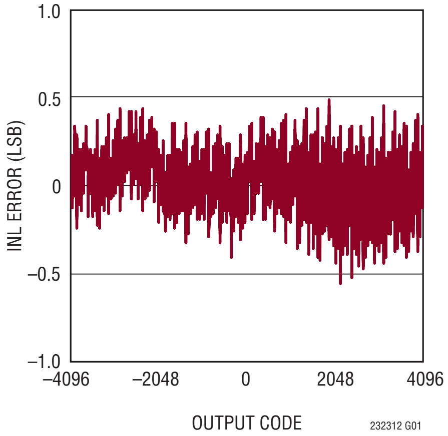


Figure 1. Voltage Levels for Timing Specifications

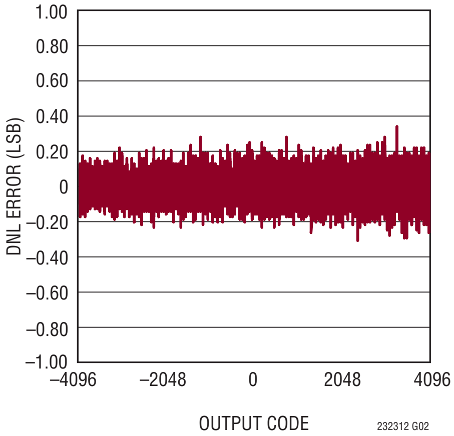
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFOUT1,2 = 4.096V, f_{SMPL} = 5Msps, unless otherwise noted. (Note 16)

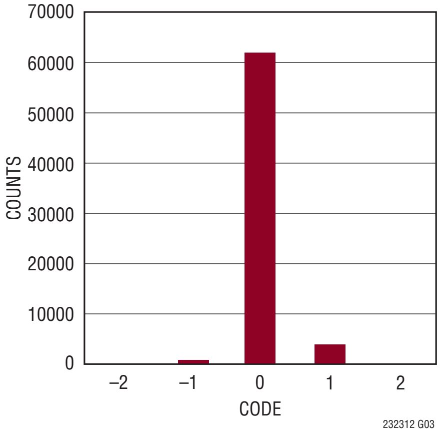
Integral Nonlinearity vs Output Code



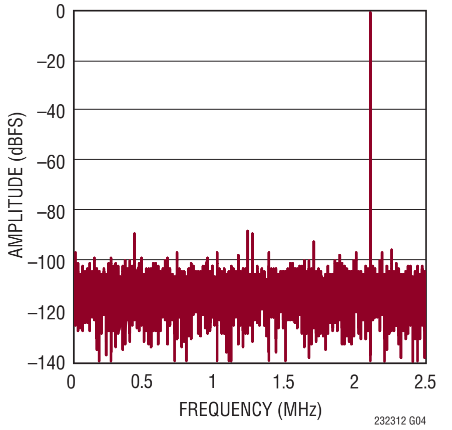
Differential Nonlinearity vs Output Code



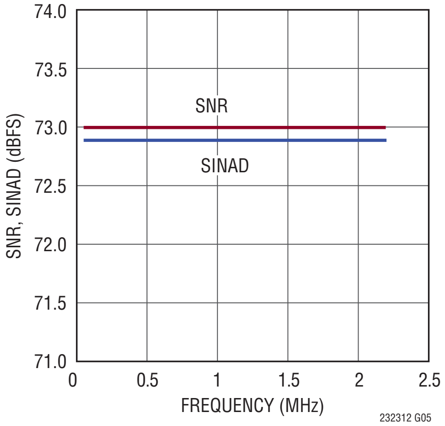
DC Histogram



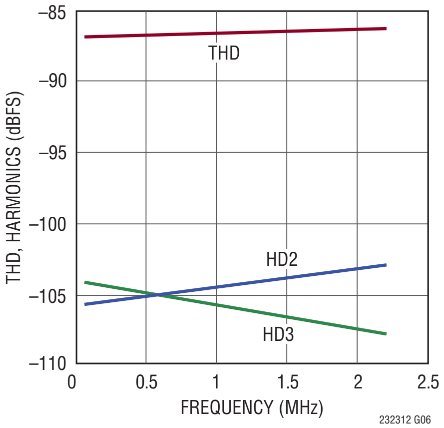
16k Point FFT, f_S = 5Msps, f_{IN} = 2.2MHz



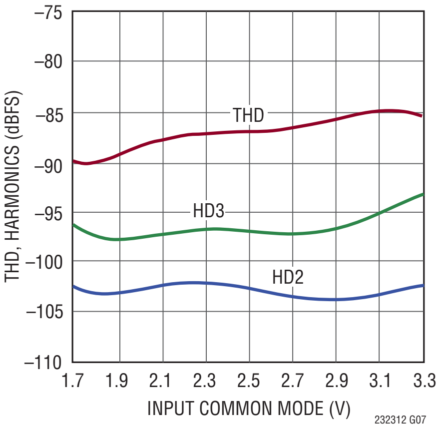
SNR, SINAD vs Input Frequency (50kHz to 2.2MHz)



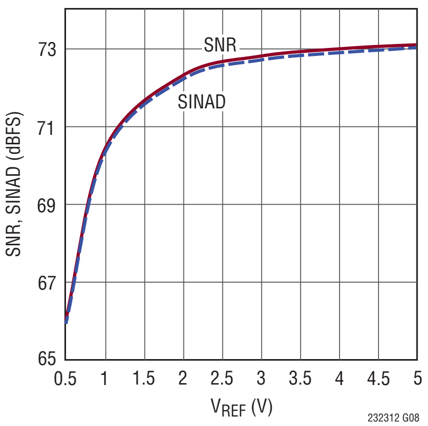
THD, Harmonics vs Input Frequency (50kHz to 2.2MHz)



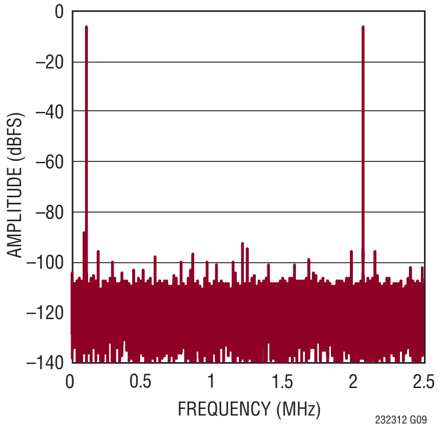
THD, Harmonics vs Input Common Mode (100kHz to 2.2MHz)



SNR, SINAD vs Reference Voltage, f_{IN} = 500kHz



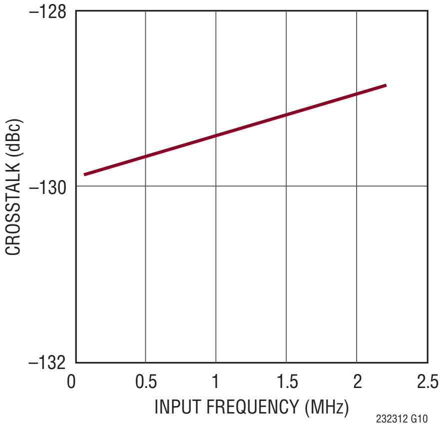
32k Point FFT, IMD, f_S = 5Msps, V_{IN}^+ = 100kHz, V_{IN}^- = 2.2MHz



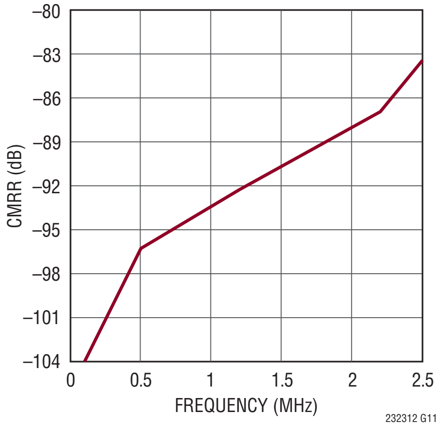
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFOUT1,2 = 4.096V, f_{SMPL} = 5Msps, unless otherwise noted. (Note 16)

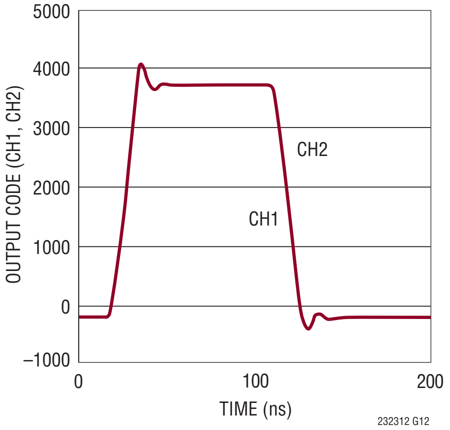
Crosstalk vs Input Frequency



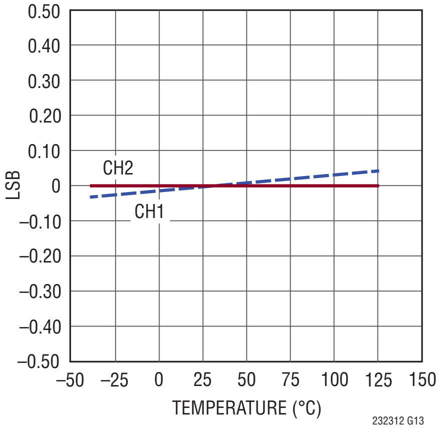
CMRR vs Input Frequency



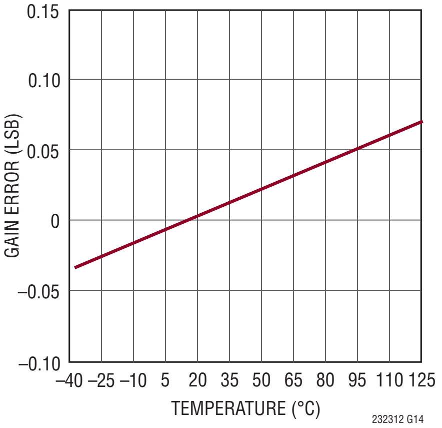
Output Match with Simultaneous Input Steps at CH1, CH2



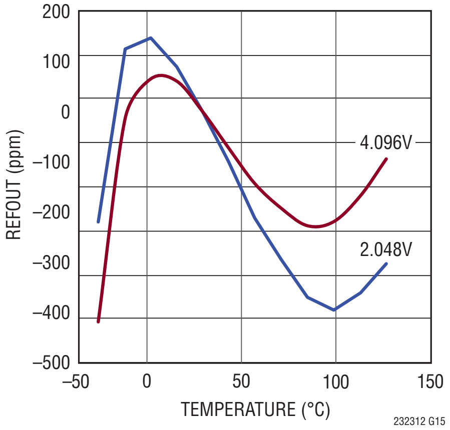
Offset Error vs Temperature



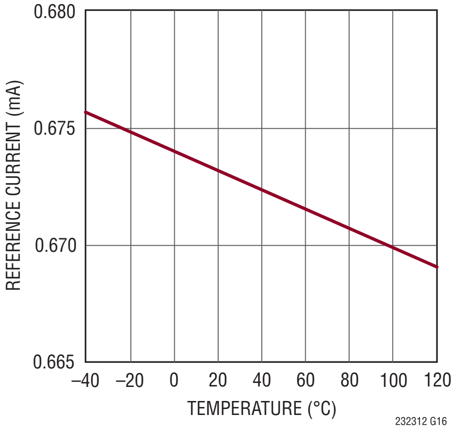
Gain Error vs Temperature



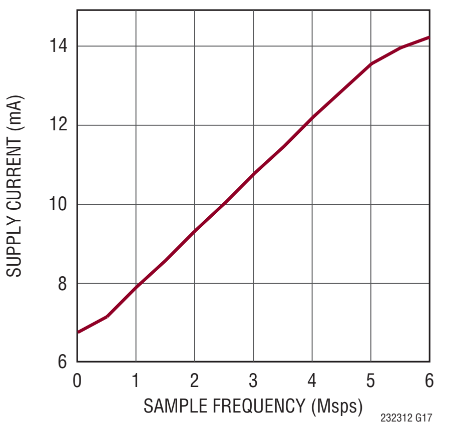
REFOUT1,2 Output vs Temperature



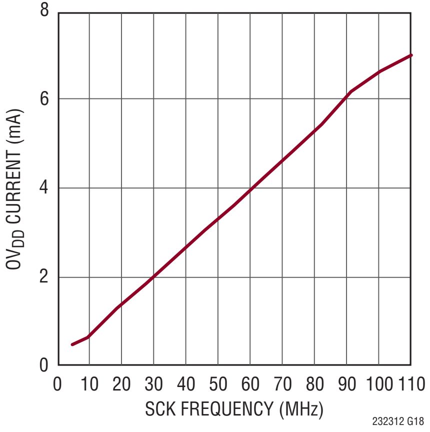
Reference Current vs Temperature, V_{REF} = 4.096V



Supply Current vs Sample Frequency



OV_{DD} Current vs SCK Frequency, C_{LOAD} = 10pF



PIN FUNCTIONS

V_{DD} (Pins 1, 8): Power Supply. Bypass V_{DD} to GND with a 10µF ceramic and a 0.1µF ceramic close to the part. The V_{DD} pins should be shorted together and driven from the same supply.

A_{IN2+}, $A_{IN2–}$ (Pins 2, 3): Analog Differential Input Pins. Full-scale range (A_{IN2+} – $A_{IN2–}$) is ±REFOUT2 voltage. These pins can be driven from V_{DD} to GND.

GND (Pins 4, 5, 10, 29): Ground. These pins and exposed pad (Pin 29) must be tied directly to a solid ground plane.

$A_{IN1–}$, A_{IN1+} (Pins 6, 7): Analog Differential Input Pins. Full-scale range (A_{IN1+} – $A_{IN1–}$) is ±REFOUT1 voltage. These pins can be driven from V_{DD} to GND.

$\overline{\text{CNV}}$ (Pin 9): Conversion Start Input. A falling edge on $\overline{\text{CNV}}$ puts the internal sample-and-hold into the hold mode and starts a conversion cycle. $\overline{\text{CNV}}$ must be driven by a low jitter clock as shown in the Typical Application on the back page. The $\overline{\text{CNV}}$ pin is unaffected by the CMOS/LVDS pin.

REFRTN1 (Pin 11): Reference Buffer 1 Output Return. Bypass REFRTN1 to REFOUT1. Do not tie the REFRTN1 pin to the ground plane.

REFOUT1 (Pin 12): Reference Buffer 1 Output. An onboard buffer nominally outputs 4.096V to this pin. This pin is referred to REFRTN1 and should be decoupled closely to the pin (no vias) with a 0.1µF (X7R, 0402 size) capacitor and a 10µF (X5R, 0805 size) ceramic capacitor in parallel. The internal buffer driving this pin may be disabled by grounding the REFINT pin. If the buffer is disabled, an external reference may drive this pin in the range of 1.25V to 5V.

VBYP1 (Pin 13): Bypass this internally supplied pin to ground with a 1µF ceramic capacitor. The nominal output voltage on this pin is 1.6V.

OV_{DD} (Pin 14): I/O Interface Digital Power. The range of OV_{DD} is 1.71V to 2.5V. This supply is nominally set to the same supply as the host interface (CMOS: 1.8V or 2.5V, LVDS: 2.5V). Bypass OV_{DD} to OGND with a 0.1µF capacitor.

$SDO1^+$, $SDO1^–$ (Pins 15, 16): Channel 1 Serial Data Output. The conversion result is shifted MSB first on each falling edge of SCK. In CMOS mode, the result is output on $SDO1^+$. The logic level is determined by OV_{DD}. Do not connect $SDO1^–$. In LVDS mode, the result is output differentially on $SDO1^+$ and $SDO1^–$. These pins must be differentially terminated by an external 100Ω resistor at the receiver (FPGA).

$CLKOUT^+$, $CLKOUT^–$ (Pins 17, 18): Serial Data Clock Output. CLKOUT provides a skew-matched clock to latch the SDO output at the receiver. In CMOS mode, the skew-matched clock is output on $CLKOUT^+$. The logic level is determined by OV_{DD}. Do not connect $CLKOUT^–$. For low throughput applications using SCK to latch the SDO output, $CLKOUT^+$ can be disabled by tying $CLKOUT^–$ to OV_{DD}. In LVDS mode, the skew-matched clock is output differentially on $CLKOUT^+$ and $CLKOUT^–$. These pins must be differentially terminated by an external 100Ω resistor at the receiver (FPGA).

$SDO2^+$, $SDO2^–$ (Pins 19, 20): Channel 2 Serial Data Output. The conversion result is shifted MSB first on each falling edge of SCK. In CMOS mode, the result is output on $SDO2^+$. The logic level is determined by OV_{DD}. Do not connect $SDO2^–$. In LVDS mode, the result is output differentially on $SDO2^+$ and $SDO2^–$. These pins must be differentially terminated by an external 100Ω resistor at the receiver (FPGA).

SCK^+, $SCK^–$ (Pins 21, 22): Serial Data Clock Input. The falling edge of this clock shifts the conversion result MSB first onto the SDO pins. In CMOS mode, drive SCK^+ with a single-ended clock. The logic level is determined by OV_{DD}. Do not connect $SCK^–$. In LVDS mode, drive SCK^+ and $SCK^–$. with a differential clock. These pins must be differentially terminated by an external 100Ω resistor at the receiver (ADC).

OGND (Pin 23): I/O Ground. This ground must be tied to the ground plane at a single point. OV_{DD} is bypassed to this pin.

PIN FUNCTIONS

VBYP2 (Pin 24): Bypass this internally supplied pin to ground with a 1µF ceramic capacitor. The nominal output voltage on this pin is 1.6V

$\overline{\text{CMOS}}$/LVDS (Pin 25): I/O Mode Select. Ground this pin to enable CMOS mode, tie to OV_{DD} to enable LVDS mode. Float this pin to enable low power LVDS mode.

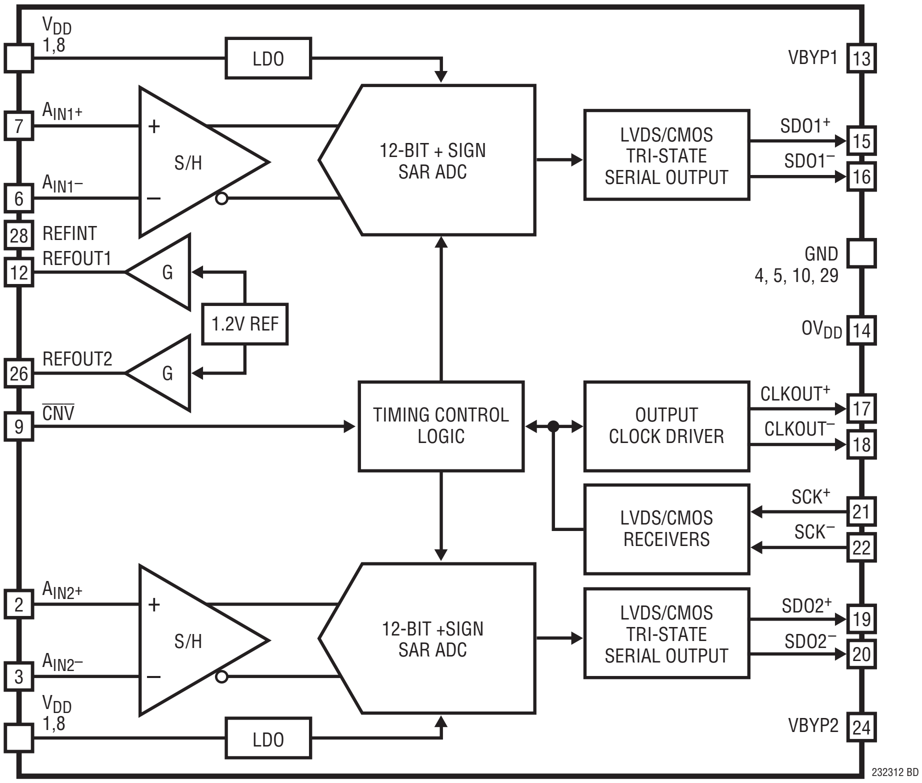
REFOUT2 (Pin 26): Reference Buffer 2 Output. An onboard buffer nominally outputs 4.096V to this pin. This pin is referred to REFRTN2 and should be decoupled closely to the pin (no vias) with a 0.1µF (X7R, 0402 size) capacitor and a 10µF (X5R, 0805 size) ceramic capacitor in parallel. The internal buffer driving this pin may be disabled by grounding the REFINT pin. If the buffer is disabled, an external reference may drive this pin in the range of 1.25V to V_{DD}.

REFRTN2 (Pin 27): Reference Buffer 2 Output Return. Bypass REFRTN2 to REFOUT2. Do not tie the REFRTN2 pin to the ground plane.

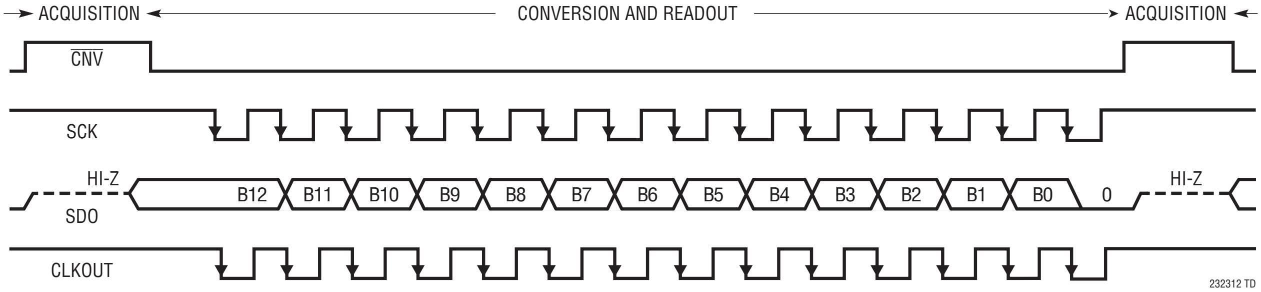
REFINT (Pin 28): Reference Buffer Output Enable. Tie to V_{DD} when using the internal reference. Tie to ground to disable the internal REFOUT1 and REFOUT2 buffers for use with external voltage references. This pin has a 500k internal pull-up to V_{DD}.

Exposed Pad (Pin 29): Ground. Solder this pad to ground.

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAM



SERIAL DATA BITS B[12:0] CORRESPOND TO PREVIOUS CONVERSION

APPLICATIONS INFORMATION

OVERVIEW

The LTC2323-12 is a low noise, high speed 12-bit + sign dual successive approximation register (SAR) ADC with differential inputs and wide input common mode range. The flexible analog inputs support fully differential, pseudo-differential bipolar and pseudo-differential unipolar drive without requiring any hardware configuration. The MSB of the 12-bit + sign two's complement output indicates the sign of the differential analog input voltage.

The ADC's transfer function provides 13-bits of resolution across the full-scale span of 2 • REFOUT, as shown in Figure 2. If the analog input spans less than this full-scale, such as in the case of pseudo-differential drive, the ADC provides 12-bits of resolution across this reduced span, with the additional benefit of digitizing over- and underrange conditions, as shown in Table 1. This unique feature is particularly useful in control loop applications.

CONVERTER OPERATION

The LTC2323-12 operates in two phases. During the acquisition phase, the sample capacitor is connected to the analog input pins A_{IN+} and A_{IN-} to sample the differential analog input voltage, as shown in Figure 3. A falling edge on the $\overline{CNV}$ pin initiates a conversion. During the conversion phase, the 13-bit CDAC is sequenced through a successive approximation algorithm for each input SCK pulse, effectively comparing the sampled input with binary-weighted fractions of the reference voltage (e.g., $V_{REFOUT}/2$, $V_{REFOUT}/4$ … $V_{REFOUT}/4096$) using a differential comparator. At the end of conversion, a CDAC output approximates the sampled analog input. The ADC control logic then prepares the 13-bit digital output code for serial transfer.

TRANSFER FUNCTION

The LTC2323-12 digitizes the full-scale voltage of 2 • REFOUT into 2^{13} levels, resulting in an LSB size of 1mV with REFBUF = 4.096V. The ideal transfer function is shown in Figure 2. The output data is in 2's complement format. When driven by fully differential inputs, the transfer function spans 2^{13} codes. When driven by pseudo-differential inputs, the transfer function spans 2^{12} codes.

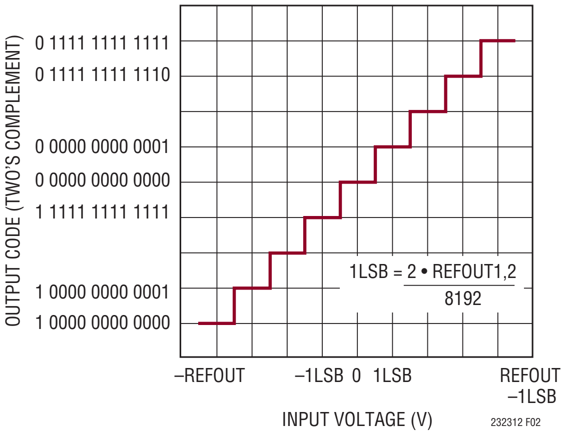


Figure 2. LTC2323-12 Transfer Function

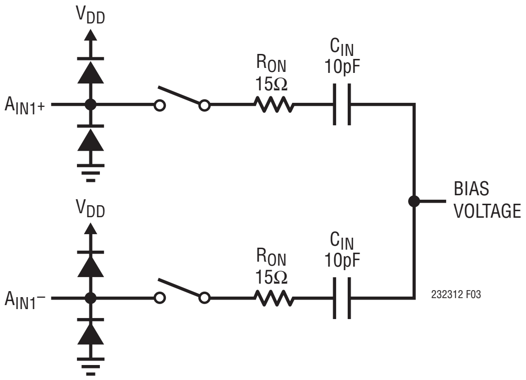


Figure 3. The Equivalent Circuit for the Differential Analog Input of the LTC2323-12

Table 1. Code Ranges for the Analog Input Operational Modes

MODE	SPAN ($V_{IN}^+ – V_{IN}^-$)	MIN CODE	MAX CODE
Fully Differential	–REFOUT to +REFOUT	1 0000 0000 0000	0 1111 1111 1111
Pseudo-Differential Bipolar	–-REFOUT/2 to +REFOUT/2	1 1000 0000 0000	0 0111 1111 1111
Pseudo-Differential Unipolar	0 to REFOUT	0 0000 0000 0000	0 1111 1111 1111

APPLICATIONS INFORMATION

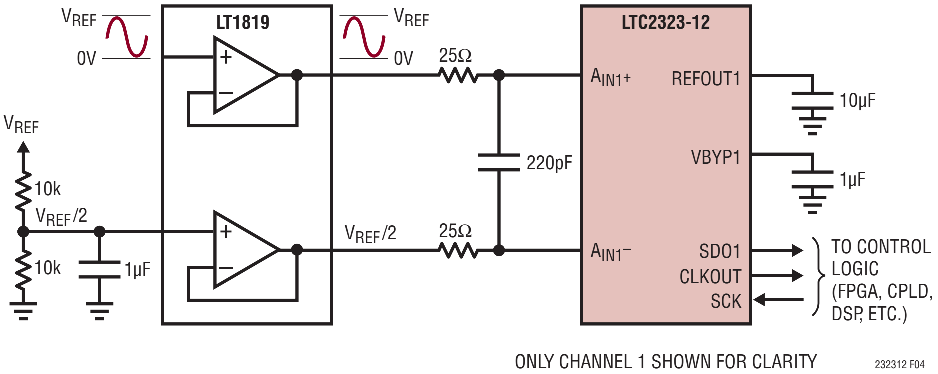


Figure 4. Pseudo-Differential Bipolar Application Circuit

Analog Input

The differential inputs of the LTC2323-12 provide great flexibility to convert a wide variety of analog signals with no configuration required. The LTC2323-12 digitizes the difference voltage between the A_{IN+} and A_{IN-} pins while supporting a wide common mode input range. The analog input signals can have an arbitrary relationship to each other, provided that they remain between V_{DD} and GND. The LTC2323-12 can also digitize more limited classes of analog input signals such as pseudo-differential unipolar/bipolar and fully differential with no configuration required.

The analog inputs of the LTC2323-12 can be modeled by the equivalent circuit shown in Figure 3. The back-to-back diodes at the inputs form clamps that provide ESD protection. In the acquisition phase, 10pF (C_{IN}) from the sampling capacitor in series with approximately 15Ω (R_{ON}) from the on-resistance of the sampling switch is connected to the input. Any unwanted signal that is common to both inputs will be reduced by the common mode rejection of the ADC sampler. The inputs of the ADC core draw a small current spike while charging the C_{IN} capacitors during acquisition.

Single-Ended Signals

Single-ended signals can be directly digitized by the LTC2323-12. These signals should be sensed pseudo-differentially for improved common mode rejection. By connecting the reference signal (e.g., ground sense) of the main analog signal to the other A_{IN} pin, any noise or disturbance common to the two signals will be rejected by the high CMRR of the ADC. The LTC2323-12 flexibility handles both pseudo-differential unipolar and bipolar signals, with no configuration required. The wide common mode input range relaxes the accuracy requirements of any signal conditioning circuits prior to the analog inputs.

Pseudo-Differential Bipolar Input Range

The pseudo-differential bipolar configuration represents driving one of the analog inputs at a fixed voltage, typically $V_{REF}/2$, and applying a signal to the other A_{IN} pin. In this case the analog input swings symmetrically around the fixed input yielding bipolar two's complement output codes with an ADC span of half of full-scale. This configuration is illustrated in Figure 4, and the corresponding transfer function in Figure 5. The fixed analog input pin need not be set at $V_{REF}/2$, but at some point within the V_{DD} rails allowing the alternate input to swing symmetrically around this voltage. If the input signal ($A_{IN+} – A_{IN-}$)

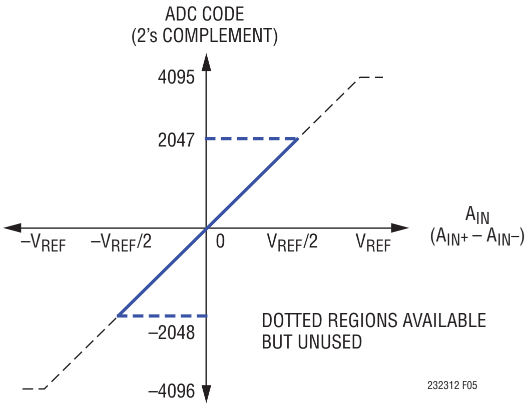


Figure 5. Pseudo-Differential Bipolar Transfer Function

APPLICATIONS INFORMATION

swings beyond ±REFOUT/2, valid codes will be generated by the ADC and must be clamped by the user, if necessary.

Pseudo-Differential Unipolar Input Range

The pseudo-differential unipolar configuration represents driving one of the analog inputs at ground and applying a signal to the other A_{IN} pin. In this case, the analog input swings between ground and V_{REF} yielding unipolar two's complement output codes with an ADC span of half of full-scale. This configuration is illustrated in Figure 6, and the corresponding transfer function in Figure 7. If the input signal ($A_{IN+} – A_{IN–}$) swings negative, valid codes will be

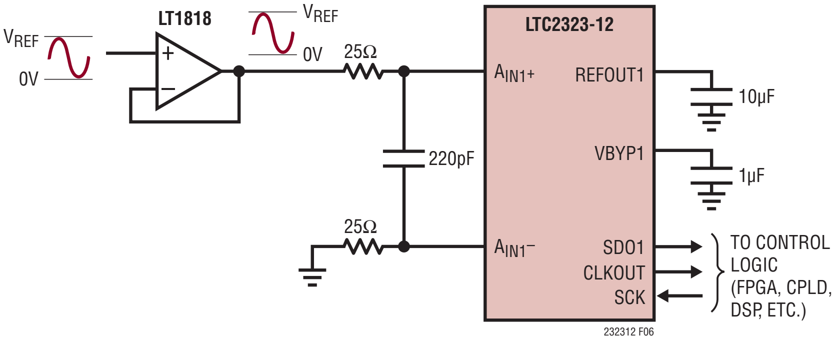


Figure 6. Pseudo-Differential Unipolar Application Circuit

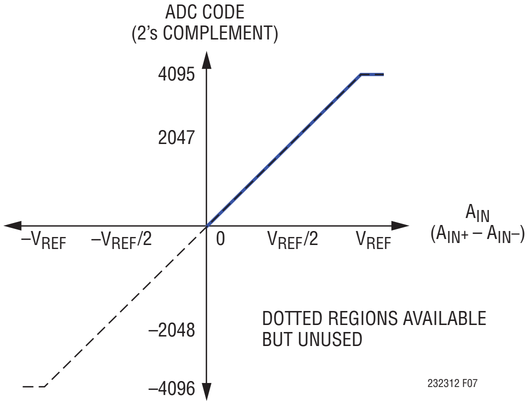


Figure 7. Pseudo-Differential Unipolar Transfer Function

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generated by the ADC and must be clamped by the user, if necessary.

Single-Ended-to-Differential Conversion

While single-ended signals can be directly digitized as previously discussed, single-ended to differential conversion circuits may also be used when higher dynamic range is desired. By producing a differential signal at the inputs of the LTC2323-12, the signal swing presented to the ADC is maximized, thus increasing the achievable SNR.

The LT®1819 high speed dual operational amplifier is recommended for performing single-ended-to-differential conversions, as shown in Figure 8. In this case, the first amplifier is configured as a unity-gain buffer and the single-ended input signal directly drives the high impedance input of this amplifier.

Fully-Differential Inputs

To achieve the full distortion performance of the LTC2323-12, a low distortion fully-differential signal source driven through the LT1819 configured as two unity-gain buffers, as shown in Figure 9, can be used. This circuit achieves the full data sheet THD specification of –85dB at input frequencies of 500kHz and less. Data sheet typical performance curves taken at higher frequencies used a harmonic rejection filter between the ADC and the signal source to eliminate the op amp as the dominant source of distortion.

The fully-differential configuration yields an analog input span ($A_{IN+} – A_{IN–}$) of ±REFOUT. In this configuration, the input signal is driven on each AIN pin, typically at equal spans but opposite polarity. This yields a high common mode rejection on the input signals. The common mode voltage of the analog input can be anywhere within the V_{DD} input range, but will be limited by the peak swing of the full-range input signal. For example, if the internal reference is used with $V_{DD} = 5V_{DC}$, the full-range input span will be ±4.096V. Half of the input span is typically driven on each AIN pin, yielding a signal span for each AIN pin of $4.096V_{P-P}$. This leaves ~0.9V of common mode variation tolerance. When using external references, it is possible to increase common mode tolerance by compressing the ADC full-range codes into a tighter range. For example, using an external 2.048V reference with V_{DD} = 5V the total span would be ±2.048V and each AIN span would

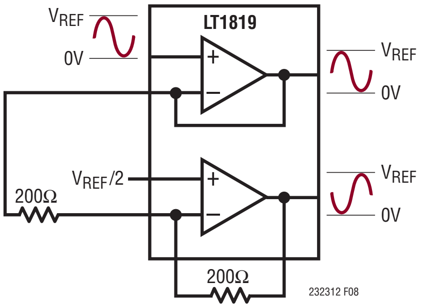

Figure 8. Single-Ended to Differential Driver

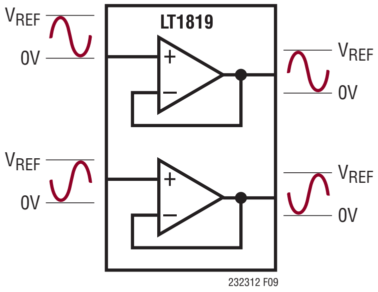

Figure 9. LT1819 Buffering a Fully-Differential Signal Source

APPLICATIONS INFORMATION

be limited to 2.048V_{P-P} allowing a common mode range of ~3V. Compressing the input span would incur a SNR penalty of approximately 1dB. Input span compression may be useful if single-supply analog input drivers are used which cannot swing rail-to-rail. The fully-differential configuration is illustrated in Figure 10, with the corresponding transfer function illustrated in Figure 11.

INPUT DRIVE CIRCUITS

A low impedance source can directly drive the high impedance inputs of the LTC2323-12 without gain error. A high impedance source should be buffered to minimize settling time during acquisition and to optimize the distortion performance of the ADC. Minimizing settling time is important even for DC inputs, because the ADC inputs draw a current spike when during acquisition.

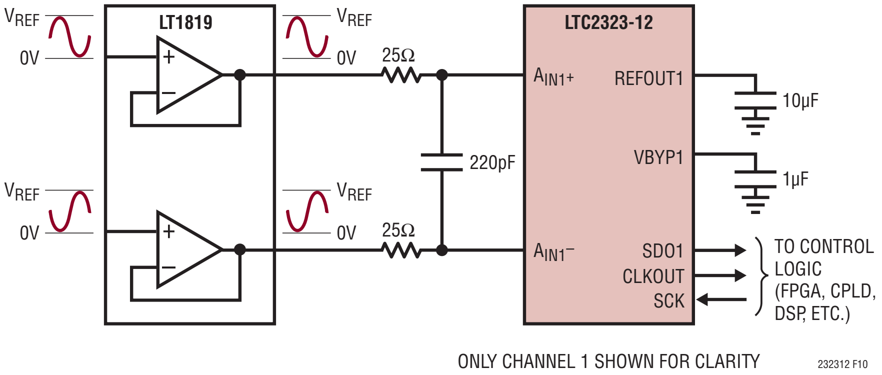

Figure 10. Fully-Differential Application Circuit

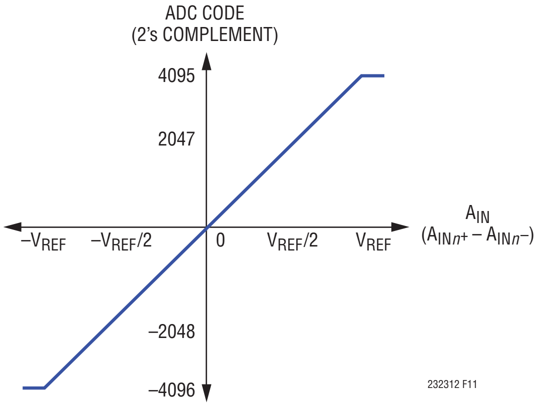

Figure 11. Fully-Differential Transfer Function

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For best performance, a buffer amplifier should be used to drive the analog inputs of the LTC2323-12. The amplifier provides low output impedance to minimize gain error and allow for fast settling of the analog signal during the acquisition phase. It also provides isolation between the signal source and the ADC inputs, which draw a small current spike during acquisition.

Input Filtering

The noise and distortion of the buffer amplifier and signal source must be considered since they add to the ADC noise and distortion. Noisy input signals should be filtered prior to the buffer amplifier input with a low bandwidth filter to minimize noise. The simple 1-pole RC lowpass filter shown in Figure 12 is sufficient for many applications.

The input resistor divider network, sampling switch on-resistance (R_{ON}) and the sample capacitor (C_{IN}) form a second lowpass filter that limits the input bandwidth to the ADC core to 110MHz. A buffer amplifier with a low noise density must be selected to minimize the degradation of the SNR over this bandwidth.

High quality capacitors and resistors should be used in the RC filters since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

ADC REFERENCE

Internal Reference

The LTC2323-12 has an on-chip, low noise, low drift (20ppm/°C max), temperature compensated bandgap reference. It is internally buffered and is available at REFOUT1,2 (Pins 12, 26). The reference buffer gains the internal reference voltage to 4.096V for supply voltages V_{DD} = 5V and to 2.048V for V_{DD} = 3.3V. Bypass REFOUT1,2 to REFRTN1,2 with the parallel combination of a 0.1µF (X7R, 0402 size) capacitor and a 10µF (X5R, 0805 size) ceramic capacitor to compensate the reference buffer and minimize noise. The 0.1µF capacitor should be as close as possible to the LTC2323-12 package to minimize wiring inductance. Tie the REFINT pin to V_{DD} to enable the internal reference buffer.

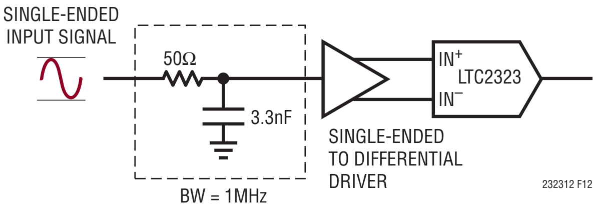


Figure 12. Input Signal Chain

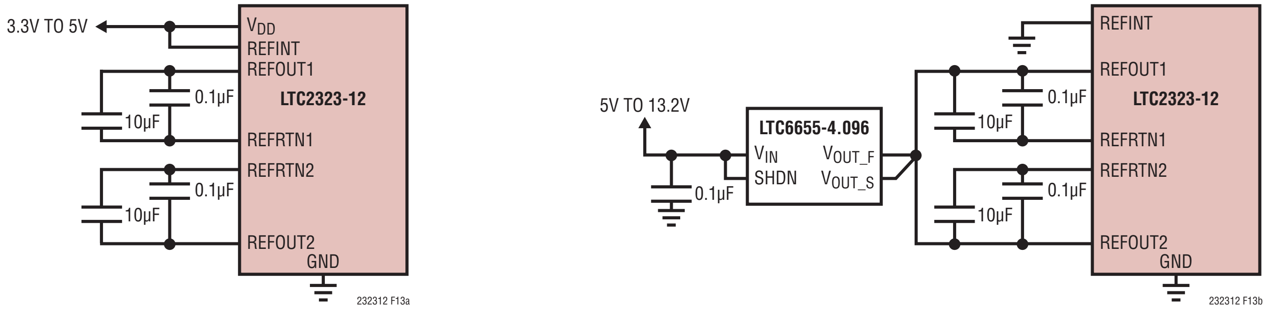
APPLICATIONS INFORMATION

Table 2. REFOUT1,2 Sources and Ranges vs V_{DD}

V_{DD}	REFINT PIN	REFOUT1,2 PIN	DIFFERENTIAL SPAN
5V	5V	Internal 4.096V	±4.096V
5V	0V	External (1.25V to 5V)	±1.25V to ±5V
3.3V	3.3V	Internal 2.048V	±2.048V
3.3V	0V	External (1.25V to 3.3V)	±1.25V to ±3.3V

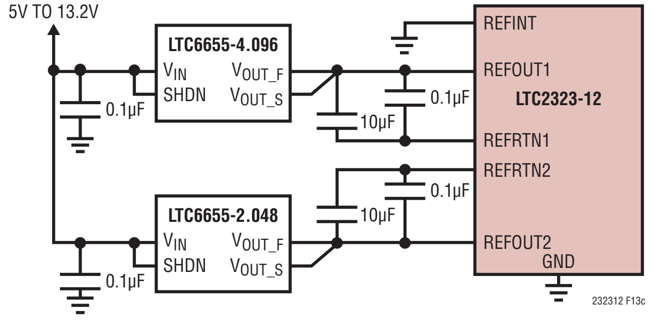
External Reference

The internal reference buffer can also be overdriven from 1.25V to 5V with an external reference at REFOUT1,2 as shown in Figure 13 (b and c). To do so, REFINT must be grounded to disable the reference buffer. A 55k internal resistance loads the REFOUT1,2 pins when the reference buffer is disabled. To maximize the input signal swing and corresponding SNR, the LTC6655-5 is recommended when overdriving REFOUT1,2. The LTC6655-5 offers the same small size, accuracy, drift and extended temperature range as the LTC6655-4.096. By using a 5V reference, a higher SNR can be achieved. We recommend bypassing the LTC6655-5 with a parallel combination of a 0.1µF (X7R, 0402 size) ceramic capacitor and a 10µF ceramic capacitor (X5R, 0805 size) close to each of the REFOUT1,2 and REFRTN1,2 pins.



(13a) LTC2323-12 Internal Reference Circuit

(13b) LTC2323-12 with a Shared External Reference Circuit



(13c) LTC2323-12 with Different External Reference Voltages

Figure 13. Reference Connection

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Internal Reference Buffer Transient Response

The REFOUT1,2 pins of the LTC2323-12 draw charge (Q_{CONV}) from the external bypass capacitors during each conversion cycle. If the internal reference buffer is overdriven, the external reference must provide all of this charge with a DC current equivalent to $I_{REF} = Q_{CONV}/t_{CYC}$. Thus, the DC current draw of REFOUT1,2 depends on the sampling rate and output code. In applications where a burst of samples is taken after idling for long periods, as shown in Figure 14 , I_{REFBUF} quickly goes from approximately ~75µA to a maximum of 500µA for REFOUT1,2 = 5V at 5Msps. This step in DC current draw triggers a transient response in the external reference that must be considered since any deviation in the voltage at REFOUT1,2 will affect the accuracy of the output code. Due to the one-cycle conversion latency, the first conversion result at the beginning of a burst sampling period will be invalid. If an external reference is used to overdrive REFOUT1,2 the fast settling LTC6655 reference is recommended.

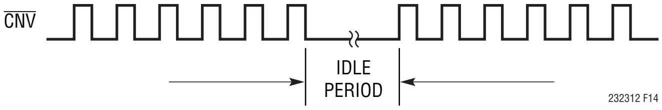


Figure 14. $\overline{CNV}$ Waveform Showing Burst Sampling

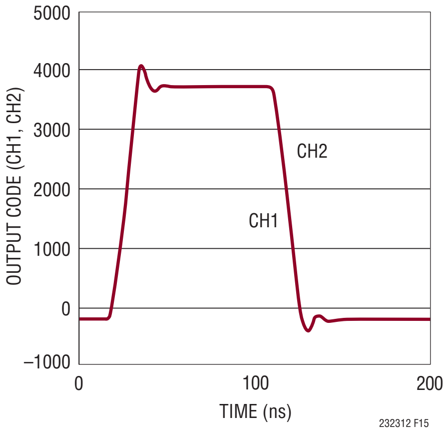


Figure 15. Transient Response of the LTC2323-12

DYNAMIC PERFORMANCE

Fast Fourier transform (FFT) techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. The LTC2323-12 provides guaranteed tested limits for both AC distortion and noise measurements.

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the A/D output. The output is bandlimited to frequencies from above DC and below half the sampling frequency. Figure 16 shows that the LTC2323-12 achieves a typical SINAD of 72.9dB at a 5MHz sampling rate with a 2.2MHz input.

Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC. Figure 16 shows that the LTC2323-12 achieves a typical SNR of 73dB at a 5MHz sampling rate with a 2.2MHz input.

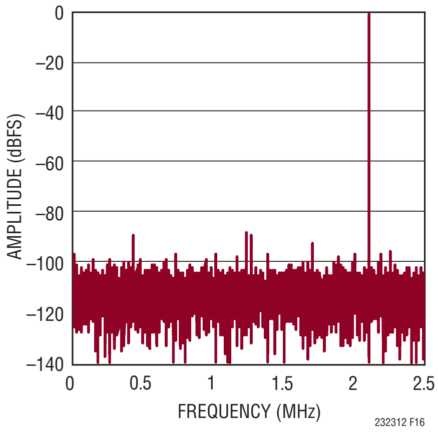


Figure 16. 16k Point FFT of the LTC2323-12

APPLICATIONS INFORMATION

Total Harmonic Distortion (THD)

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{SMPL}/2$). THD is expressed as:

$$THD = 20\log\frac{\sqrt{V2^2 + V3^2 + V4^2 + \ldots + V_N^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through V_N are the amplitudes of the second through Nth harmonics.

POWER CONSIDERATIONS

The LTC2323-12 requires two power supplies: the 5V power supply (V_{DD}), and the digital input/output interface power supply (OV_{DD}). The flexible OV_{DD} supply allows the LTC2323-12 to communicate with any digital logic operating between 1.8V and 2.5V. When using LVDS I/O, the OV_{DD} supply must be set to 2.5V.

Power Supply Sequencing

The LTC2323-12 does not have any specific power supply sequencing requirements. Care should be taken to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The LTC2323-12 has a power-on-reset (POR) circuit that will reset the LTC2323-12 at initial power-up or whenever the power supply voltage drops below 2V. Once the supply voltage re-enters the nominal supply voltage range, the POR will reinitialize the ADC. No conversions should be initiated until 10ms after a POR event to ensure the reinitialization period has ended. Any conversions initiated before this time will produce invalid results.

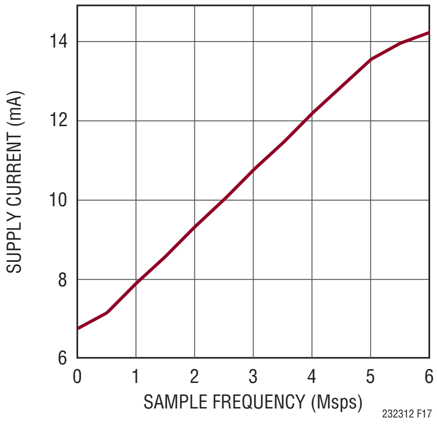


Figure 17. Power Supply Current of the LTC2323-12 Versus Sampling Rate

APPLICATIONS INFORMATION

TIMING AND CONTROL

$\overline{\text{CNV}}$ Timing

A rising edge on $\overline{\text{CNV}}$ initiates the acquisition phase and puts the internal sample-and-hold into the sample mode. A falling edge on $\overline{\text{CNV}}$ puts the internal sample-and-hold into the hold mode and starts a conversion cycle. The $\overline{\text{CNV}}$ pulse must be at least 30ns wide for proper operation. $\overline{\text{CNV}}$ must be driven by a fast low jitter signal with a fall time from OV_{DD} to below 100mV of less than 1ns. To achieve this fast falling edge, the distance from the $\overline{\text{CNV}}$ source to the $\overline{\text{CNV}}$ pin should be minimized. The trace for this pulse should be kept as narrow as possible and routed away from adjacent traces or planes to minimize capacitance. The drive strength of the gate driving the $\overline{\text{CNV}}$ line must be sufficient to yield a fast falling edge at the ADC pin to below 100mV. We recommend the Typical Application on the back page, which uses a high speed flip-flop to generate the $\overline{\text{CNV}}$ pulse to the ADC, eliminating the effect of jitter from the FPGA. If jitter from the FPGA is not a concern, the flip-flop can be eliminated and replaced with an inverter such as the NC7SZ04P5X.

SCK Serial Data Clock Input

The falling edge of this clock shifts the conversion result MSB first onto the SDO pins. A 105MHz external clock must be applied at the SCK pin to achieve 5Msps throughput.

CLKOUT Serial Data Clock Output

The CLKOUT output provides a skew-matched clock to latch the SDO output at the receiver. The timing skew of the CLKOUT and SDO outputs are matched. For high throughput applications, using CLKOUT instead of SCK to capture the SDO output eases timing requirements at the receiver. For low throughput applications, CLKOUT$^+$ can be disabled by tying CLKOUT$^-$ to OV_{DD}.

Nap/Sleep Modes

Nap mode is a method to save power without sacrificing power-up delays for subsequent conversions. Sleep mode has substantial power savings, but a power-up delay is incurred to allow the reference and power systems to become valid. To enter nap mode on the LTC2323-12, the SCK signal must be held high or low and a series of two $\overline{\text{CNV}}$ pulses must be applied. This is the case for both CMOS and LVDS modes. The second rising edge of $\overline{\text{CNV}}$ initiates the nap state. The nap state will persist until either a single rising edge of SCK is applied, or further $\overline{\text{CNV}}$ pulses are applied. The SCK rising edge will put the LTC2323-12 back into the operational (full-power) state. When in nap mode, two additional pulses will put the LTC2323-12 in sleep mode. When configured for CMOS I/O operation, a single rising edge of SCK can return the LTC2323-12 into operational mode. A 10ms delay is necessary after exiting sleep mode to allow the reference buffer to recharge the external filter capacitor. In LVDS mode, exit sleep mode by supplying a fifth $\overline{\text{CNV}}$ pulse. The fifth pulse will return the LTC2323-12 to operational mode, and further SCK pulses will keep the part from re-entering nap and sleep modes. The fifth SCK pulse also works in CMOS mode as a method to exit sleep. In the absence of SCK pulses, repetitive $\overline{\text{CNV}}$ pulses will cycle the LTC2323-12 between operational, nap and sleep modes indefinitely.

Refer to the timing diagrams in Figure 18, Figure 19, Figure 20 and Figure 21 for more detailed timing information about sleep and nap modes.

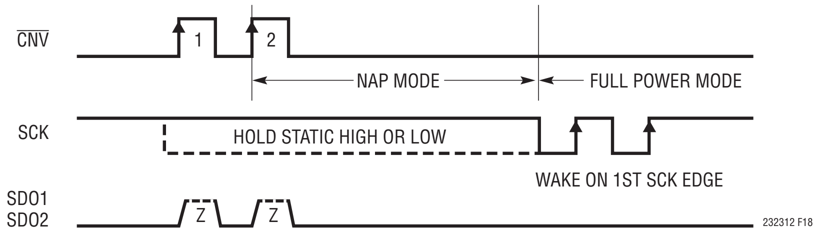


Figure 18. CMOS and LVDS Mode NAP and WAKE Using SCK

APPLICATIONS INFORMATION

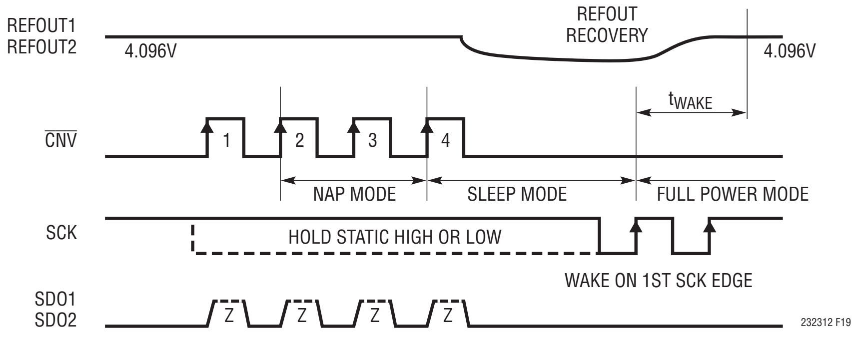


Figure 19. CMOS Mode SLEEP and WAKE Using SCK

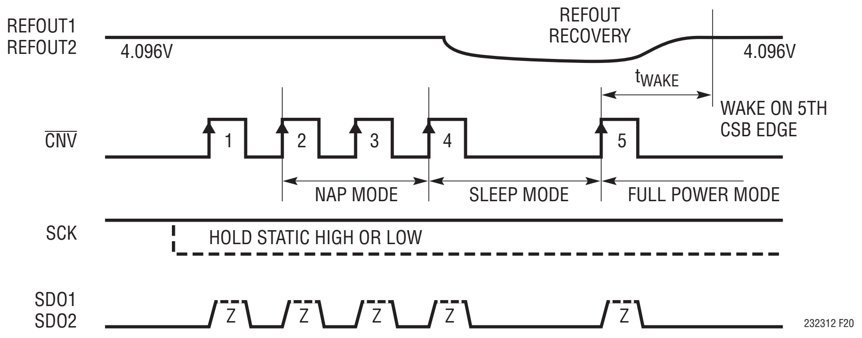
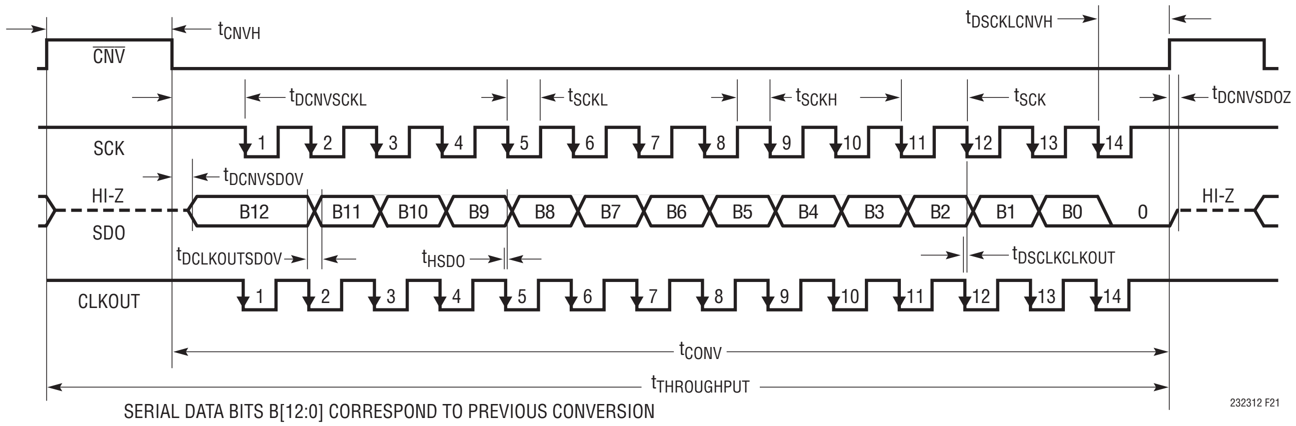


Figure 20. LVDS and CMOS Mode SLEEP and WAKE Using $\overline{CNV}$



SERIAL DATA BITS B[12:0] CORRESPOND TO PREVIOUS CONVERSION

Figure 21. LTC2323-12 Timing Diagram

APPLICATIONS INFORMATION

DIGITAL INTERFACE

The LTC2323-12 features a serial digital interface that is simple and straight forward to use. The flexible OV_{DD} supply allows the LTC2323-12 to communicate with any digital logic operating between 1.8V and 2.5V. A 105MHz external clock must be applied at the SCK pin to achieve 5Msps throughput.

In addition to a standard CMOS SPI interface, the LTC2323-12 provides an optional LVDS SPI interface to support low noise digital design. The CMOS/LVDS pin is used to select the digital interface mode.

The falling edge of SCK outputs the conversion result MSB first on the SDO pins. CLKOUT provides a skew-matched clock to latch the SDO output at the receiver. The timing skew of the CLKOUT and SDO outputs are matched. For high throughput applications, using CLKOUT instead of SCK to capture the SDO output eases timing requirements at the receiver.

In CMOS mode, use the $SDO1^+$, $SDO2^+$ and $CLKOUT^+$ pins as outputs. Use the SCK^+ pin as an input. Do not connect the $SDO1^-$, $SDO2^-$, SCK^- and $CLKOUT^-$ pins, as they each have internal pull-down circuitry to OGND.

In LVDS mode, use the $SDO1^+/SDO1^-$, $SDO2^+/SDO2^-$ and $CLKOUT^+/CLKOUT^-$ pins as differential outputs. These pins must be differentially terminated by an external 100Ω resistor at the receiver (FPGA). The SCK^+/SCK^- pins are differential inputs and must be terminated differentially by an external 100Ω resistor at the receiver (ADC).

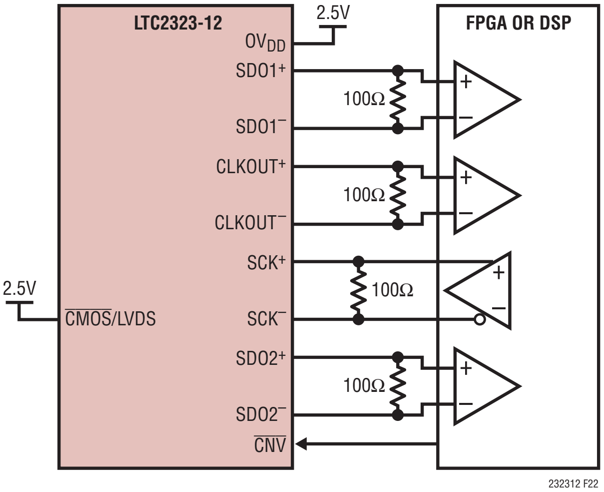


Figure 22. LTC2323 Using the LVDS Interface

APPLICATIONS INFORMATION

BOARD LAYOUT

To obtain the best performance from the LTC2323-12, a printed circuit board is recommended. Layout for the printed circuit board (PCB) should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital clocks or signals adjacent to analog signals or underneath the ADC.

Recommended Layout

The following is an example of a recommended PCB layout. A single solid ground plane is used. Bypass capacitors to the supplies are placed as close as possible to the supply pins. Low impedance common returns for these bypass capacitors are essential to the low noise operation of the ADC. The analog input traces are screened by ground. For more details and information, refer to the DC1996, the evaluation kit for the LTC2323-12.

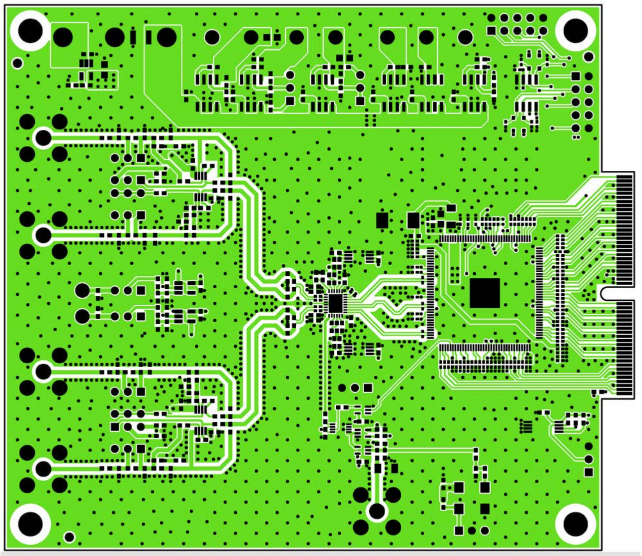


Figure 23. Layer 1, Top Layer

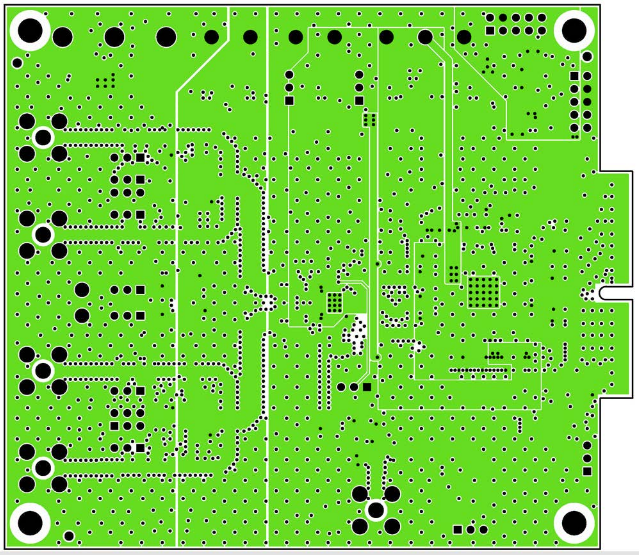


Figure 25. Layer 3, Power Plane

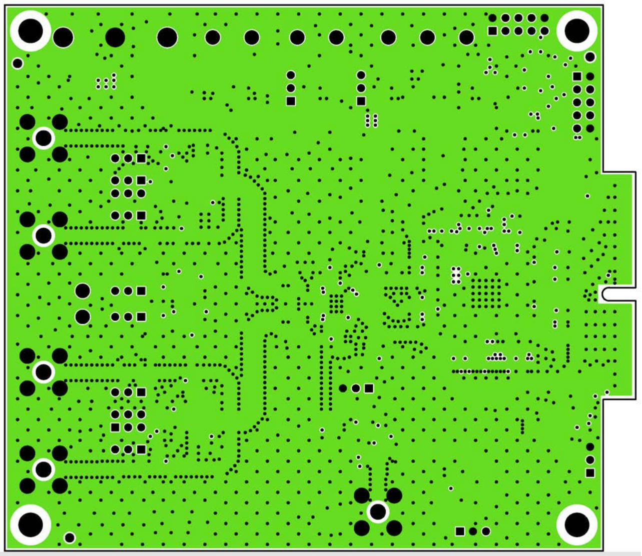


Figure 24. Layer 2, Ground Plane

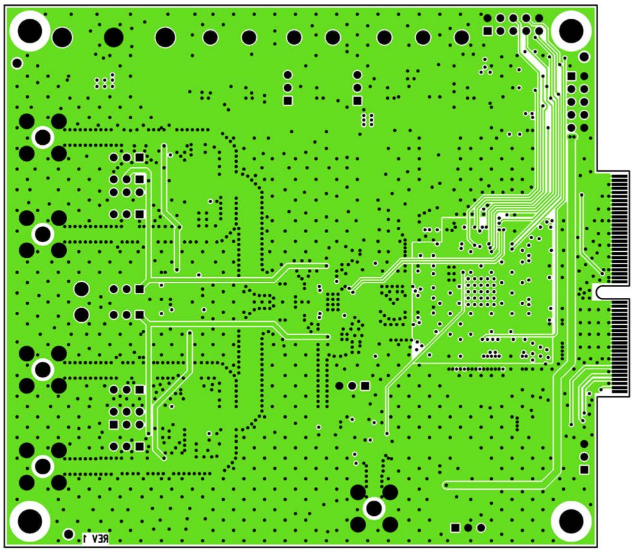
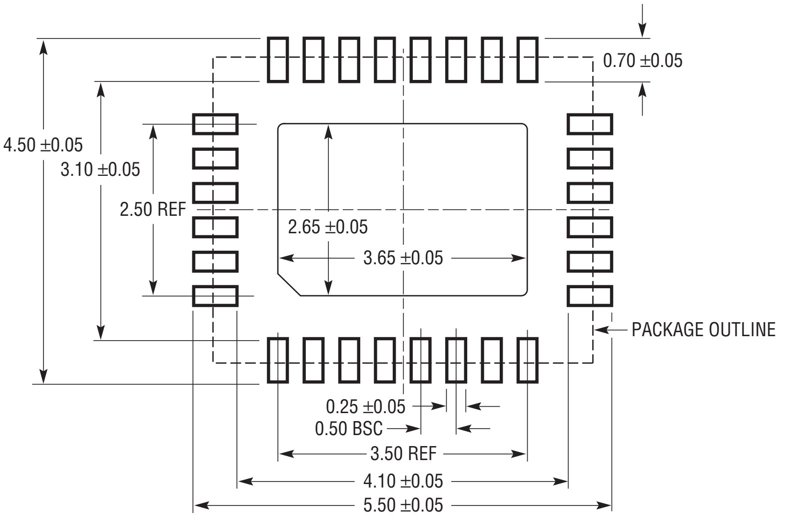


Figure 26. Layer 4, Bottom Layer

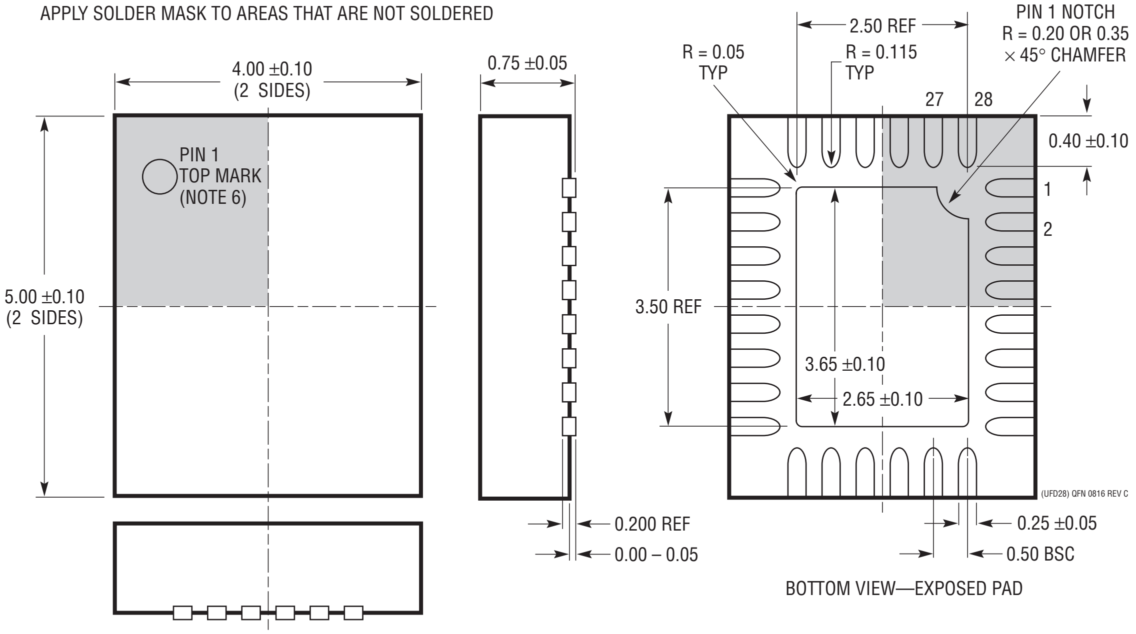
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC2323-12#packaging for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



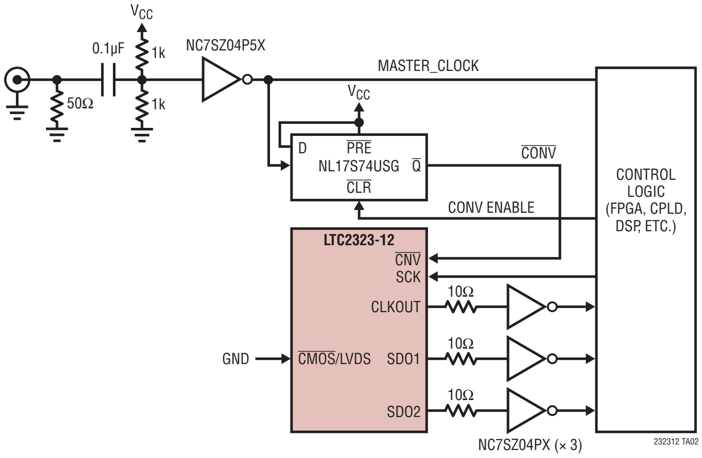
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	5/17	Changed the $\overline{\text{CNV}}$ pin description in the Pin Functions section, and the $\overline{\text{CNV}}$ Timing section in the Applications Information section.	8, 20
		Changed Fairchild components on the Typical Application.	26

TYPICAL APPLICATION

Low Jitter Clock Timing with RF Sine Generator Using Clock Squaring/Level-Shifting Circuit and Retiming Flip-Flop



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC2323-16/LTC2323-14	16-/14-Bit, 5Msps Simultaneous Sampling ADC	3.3V/5V Supply, Differential Input with Wide Input Common Mode Range, 45mW/Ch, 4mm × 5mm QFN-28 Package
LTC2321-16/LTC2321-14/ LTC2321-12	16-/14-/12-Bit, Dual, 2Msps Simultaneous Sampling ADC	3.3V/5V Supply, Differential Input with Wide Input Common Mode Range, 33mW/Ch, 4mm × 5mm QFN-28 Package
LTC2314-14	14-Bit, 4.5Msps Serial ADC	3V/5V Supply, 18mW/31mW, 20ppm/°C Max Internal Reference, Unipolar Inputs, 8-Lead TSOT-23 Package
LTC2370-16/LTC2368-16/ LTC2367-16/LTC2364-16	16-Bit, 2Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Pseudo-Differential Unipolar Input, 94dB SNR, 5V Input Range, DGC, Pin-Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2380-16/LTC2378-16/ LTC2377-16/LTC2376-16	16-Bit, 2Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Differential Input, 96.2dB SNR, ±5V Input Range, DGC, Pin-Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
DACs		
LTC2632	Dual 12-/10-/8-Bit, SPI V_{OUT} DACs with Internal Reference	2.7V to 5.5V Supply Range, 10ppm/°C Reference, External REF Mode, Rail-to-Rail Output, 8-Pin ThinSOT™ Package
LTC2602/LTC2612/ LTC2622	Dual 16-/14-/12-Bit SPI V_{OUT} DACs with External Reference	300µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, 8-Lead MSOP Package
References		
LTC6655	Precision Low Drift, Low Noise Buffered Reference	5V/4.096V/3.3V/3V/2.5V/2.048V/1.25V, 5ppm/°C, 0.25ppm Peak-to-Peak Noise, MSOP-8 Package
LTC6652	Precision Low Drift, Low Noise Buffered Reference	5V/4.096V/3.3V/3V/2.5V/2.048V/1.25V, 5ppm/°C, 2.1ppm Peak-to-Peak Noise, MSOP-8 Package
Amplifiers		
LT1818/LT1819	400MHz, 2500V/µs, 9mA Single/Dual Operational Amplifiers	–85dBc Distortion at 5MHz, 6nV/$\sqrt{Hz}$ Input Noise Voltage, 9mA Supply Current, Unity-Gain Stable
LT1806	325MHz, Single, Rail-to-Rail Input and Output, Low Distortion, Low Noise Precision Op Amps	–80dBc Distortion at 5MHz, 3.5nV/$\sqrt{Hz}$ Input Noise Voltage, 9mA Supply Current, Unity-Gain Stable

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