First Edition
Apr 20, 2005

LCD Module Technical Specification

Final Revision
******

Type No. **F-51851GNFQJ-LY-ADN**

Approved by (Quality Assurance Division)

Checked by (ACI Engineering Division)

T.Yuchi

Prepared by (ACI Engineering Division)

Table of Contents

Revision History

Rev.	Date	Page	Comment

1.General Specifications

Operating Temp.	:	min. -20°C ~max. 70°C
Storage Temp.	:	min. -30°C ~max. 80°C
Dot Pixels	:	240 (W) × 64 (H) dots
Dot Size	:	0.50 (W) × 0.50 (H) mm
Dot Pitch	:	0.53 (W) × 0.53 (H) mm
Viewing Area	:	130.2 (W) × 37.6 (H) mm
Outline Dimensions	:	135.2* (W) × 51.7** (H) × 9.8* (D) mm * Without Hook **Without Flat Cable and LED Cable
Weight	:	77g max.
LCD Type	:	NTD-23162 (F-STN / Black&White-mode / Transmissive)
Viewing Angle	:	6:00
Data Transfer	:	8-bit parallel data transfer Serial data transfer
Backlight	:	LED Backlight / Yellow
Additional Spec.	:	Vivid Color Display Specification (High Performance Color is Used)
Drawing	:	Dimensional Outline UE-312338
RoHS regulation	:	To our best knowledge, this product satisfies material requirement of RoHS regulation. Our company is doing the best efforts to obtain the equivalent certificate from our suppliers.

2.Electrical Specifications

2.1.Absolute Maximum Ratings

V_{SS}=0V

Parameter	Symbol	Conditions	Min.	Max.	Units
Supply Voltage (Logic)	V_{DD}-V_{SS}	-	-0.3	7.0	V
Supply Voltage (Booster Circuit)	V_{SS2}	With Double *1	-7.0	+0.3	V
		With Triple *1	-6.0	+0.3	
		With Quad *1	-4.5	+0.3	
Supply Voltage 1 (LCD Drive)	V_5,V_{OUT}	*1	-18.0	+0.3	V
Supply Voltage 2 (LCD Drive)	V_1, V_2, V_3, V_4	*1	V_5	+0.3	V
Input Voltage	V_{IN}	-	-0.3	V_{DD}+0.3	V
Output Voltage	V_O	-	-0.3	V_{DD}+0.3	V

*1 Relative to V_{DD}.

The relation of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 > V_{OUT}$; $V_{DD} > V_{SS} \geq V_{OUT}$ must be maintained.

In case of inputting external LCD driving voltage, LCD drive voltage should start supplying toNJU6676 at the mean time of turning on VDD power supply or after turned on VDD.

In use of the voltage boost circuit, the condition that the supply voltage : $18V \geq V_{DD}$-V_{OUT} is necessary.

Decoupling capacitor should be connected between VDD and VSS due to the stabilized operation for the voltage converter.

2.2.DC Characteristics

Ta=25°C, V_{SS}=0V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage (Logic) *1	V_{DD}-V_{SS}	-	2.2	-	5.5	V
Supply Voltage (Booster Circuit)	V_{SS2}	*2	-6.0	-	-2.5	V
Supply Voltage (LCD Drive)	V_5	*2	-18.0	-	-6.0	V
	V_1, V_2	*2	0.4×V_5	-	V_{DD}	V
	V_3, V_4	*2	V_5	-	0.6×V_5	V
Supply Voltage (Booster Circuit)	V_{SS2}	With Triple *2	-6.0	-	-2.5	V
		With Quad *2	-4.5	-	-2.5	
Booster Output Voltage	V_{OUT}	*2	-18.0	-	-	V
Voltage Regulator Operating Voltage	V_{OUT2}	Voltage converter off External power supply	-18.0	-	-6.0	V
Voltage Follower Operating Voltage	V_5	Voltage regulator off External power supply	-18.0	-	-6.0	V
Base Voltage	V_{REG}%	V_{DD}=3.0V	-	-	3.0	%
"High" Level Input Voltage	V_{IH}	-	0.8×V_{DD}	-	V_{DD}	V
"Low" Level Input Voltage	V_{IL}	-	V_{SS}	-	0.2×V_{DD}	V

"High" Level Output Voltage	V_{OH}	I_{OH}=-0.5mA	0.8×V_{DD}	-	V_{DD}	V
"Low" Level Output Voltage	V_{OL}	I_{OL}=0.5mA	V_{SS}	-	0.2×V_{DD}	V
Supply Current	I_{DD}	V_{DD}-V_{SS}=5.0V	-	3.3	5.0	mA
	I_5	V_{DD}-V_5=10.4V	-	0.4	0.6	mA

*1 Although the NJU6676 can operate in wide range of the operation voltage, it shall not be guaranteed in a sudden voltage fluctuation during the access with MPU.

*2 Relative to V_{DD}.

2.3. AC Characteristics

2.3.1. Read/Write Operation Sequence (80 series CPU)

V_{DD}=4.5~5.5V

Parameter	Symbol	Min.	Max.	Units
Address Hold Time	t_{AH8}	0	-	ns
Address Setup Time	t_{AW8}	0	-	ns
System Cycle Time	t_{CYC8}	166	-	ns
Control Low Pulse Width(Write)	t_{CCLW}	30	-	ns
Control Low Pulse Width(Read)	t_{CCLR}	70	-	ns
Control High Pulse Width(Write)	t_{CCHW}	30	-	ns
Control High Pulse Width(Read)	t_{CCHR}	30	-	ns
Data Setup Time	t_{DS8}	30	-	ns
Data Hold Time	t_{DH8}	10	-	ns
RD Access Time	t_{ACC8}	-	70	ns
Output Disable Time	t_{OH8}	10	50	ns
Input Signal Rise/Fall Time	t_r, t_f	-	15	ns

V_{DD}=2.7~4.5V

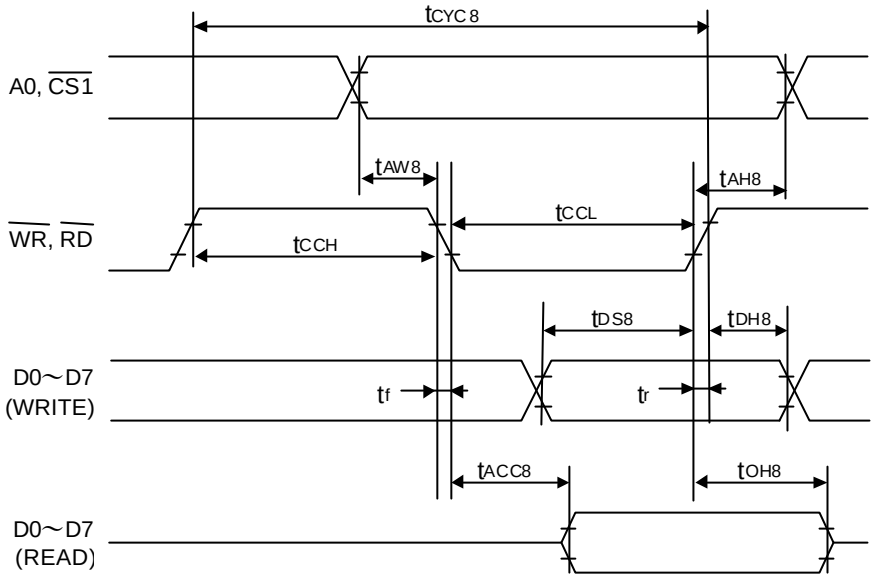
Parameter	Symbol	Min.	Max.	Units
Address Hold Time	t_{AH8}	0	-	ns
Address Setup Time	t_{AW8}	0	-	ns
System Cycle Time	t_{CYC8}	300	-	ns
Control Low Pulse Width(Write)	t_{CCLW}	60	-	ns
Control Low Pulse Width(Read)	t_{CCLR}	120	-	ns
Control High Pulse Width(Write)	t_{CCHW}	60	-	ns
Control High Pulse Width(Read)	t_{CCHR}	60	-	ns
Data Setup Time	t_{DS8}	40	-	ns
Data Hold Time	t_{DH8}	15	-	ns
RD Access Time	t_{ACC8}	-	140	ns
Output Disable Time	t_{OH8}	10	100	ns
Input Signal Rise/Fall Time	t_r, t_f	-	15	ns

V_{DD}=2.2~2.7V

Parameter	Symbol	Min.	Max.	Units
Address Hold Time	t_{AH8}	0	-	ns
Address Setup Time	t_{AW8}	0	-	ns
System Cycle Time	t_{CYC8}	1000	-	ns
Control Low Pulse Width(Write)	t_{CCLW}	120	-	ns
Control Low Pulse Width(Read)	t_{CCLR}	240	-	ns
Control High Pulse Width(Write)	t_{CCHW}	120	-	ns
Control High Pulse Width(Read)	t_{CCHR}	120	-	ns
Data Setup Time	t_{DS8}	80	-	ns

Data Hold Time	t_{DH8}	30	-	ns
RD Access Time	t_{ACC8}	-	280	ns
Output Disable Time	t_{OH8}	10	200	ns
Input Signal Rise/Fall Time	t_r, t_f	-	15	ns

Each timing is specified based on 0.2×VDD and 0.8×VDD.



2.3.2. Read/Write Operation Sequence (68 series CPU)

V_{DD}=4.5~5.5V

Parameter	Symbol	Min.	Max.	Units
Address Hold Time	t_{AH6}	0	-	ns
Address Setup Time	t_{AW6}	0	-	ns
System Cycle Time	t_{CYC6}	166	-	ns
Enable High Pulse Width (Read)	t_{EWHR}	70	-	ns
Enable High Pulse Width (Write)	t_{EWHW}	30	-	ns
Enable Low Pulse Width (Read)	t_{EWLR}	30	-	ns
Enable Low Pulse Width (Write)	t_{EWLW}	30	-	ns
Data Setup Time	t_{DS6}	30	-	ns
Data Hold Time	t_{DH6}	10	-	ns
Access Time (CL=100pF)	t_{ACC6}	-	70	ns
Output Disable Time	t_{OH6}	10	50	ns
Input Signal Rise/Fall Time	t_r, t_f	-	15	ns

V_{DD}=2.7~4.5V

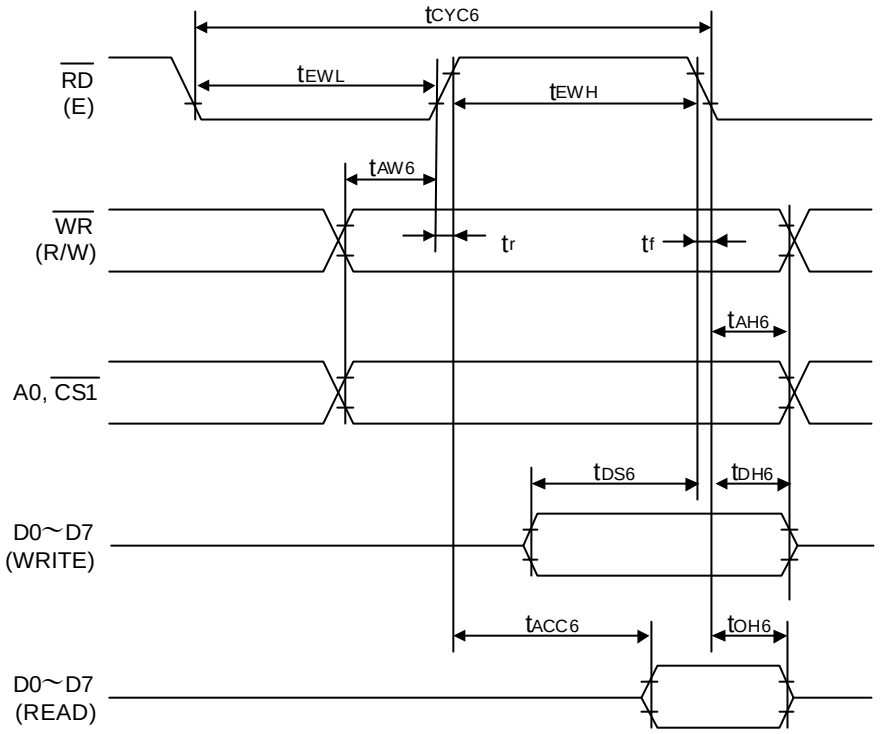
Parameter	Symbol	Min.	Max.	Units
Address Hold Time	t_{AH6}	0	-	ns
Address Setup Time	t_{AW6}	0	-	ns
System Cycle Time	t_{CYC6}	300	-	ns
Enable High Pulse Width (Read)	t_{EWHR}	120	-	ns
Enable High Pulse Width (Write)	t_{EWHW}	60	-	ns
Enable Low Pulse Width (Read)	t_{EWLR}	60	-	ns
Enable Low Pulse Width (Write)	t_{EWLW}	60	-	ns
Data Setup Time	t_{DS6}	40	-	ns
Data Hold Time	t_{DH6}	15	-	ns
Access Time (CL=100pF)	t_{ACC6}	-	140	ns
Output Disable Time	t_{OH6}	10	100	ns
Input Signal Rise/Fall Time	t_r, t_f	-	15	ns

V_{DD}=2.2~2.7V

Parameter	Symbol	Min.	Max.	Units
Address Hold Time	t_{AH6}	0	-	ns
Address Setup Time	t_{AW6}	0	-	ns
System Cycle Time	t_{CYC6}	1000	-	ns
Enable High Pulse Width (Read)	t_{EWHR}	240	-	ns
Enable High Pulse Width (Write)	t_{EWHW}	120	-	ns
Enable Low Pulse Width (Read)	t_{EWLR}	120	-	ns
Enable Low Pulse Width (Write)	t_{EWLW}	120	-	ns
Data Setup Time	t_{DS6}	80	-	ns

Data Hold Time	t_{DH6}	30	-	ns
Access Time (CL=100pF)	t_{ACC6}	-	280	ns
Output Disable Time	t_{OH6}	10	200	ns
Input Signal Rise/Fall Time	t_r, t_f	-	15	ns

Each timing is specified based on 0.2×VDD and 0.8×VDD.



2.3.3. Serial Interface Sequence

V_{DD}=4.5~5.5V

Parameter	Symbol	Min.	Max.	Units
Serial Clock Cycle	t_{SCYC}	200	-	ns
Serial Clock High Pulse Width	t_{SHW}	75	-	ns
Serial Clock Low Pulse Width	t_{SLW}	75	-	ns
Address Setup Time	t_{SAS}	50	-	ns
Address Hold Time	t_{SAH}	100	-	ns
Data Setup Time	t_{SDS}	50	-	ns
Data Hold Time	t_{SDH}	50	-	ns
CS-SCL Time	t_{CSS}	100	-	ns
	t_{CSH}	100	-	ns
Input Signal Rise/Fall Time	t_r, t_f	-	15	ns

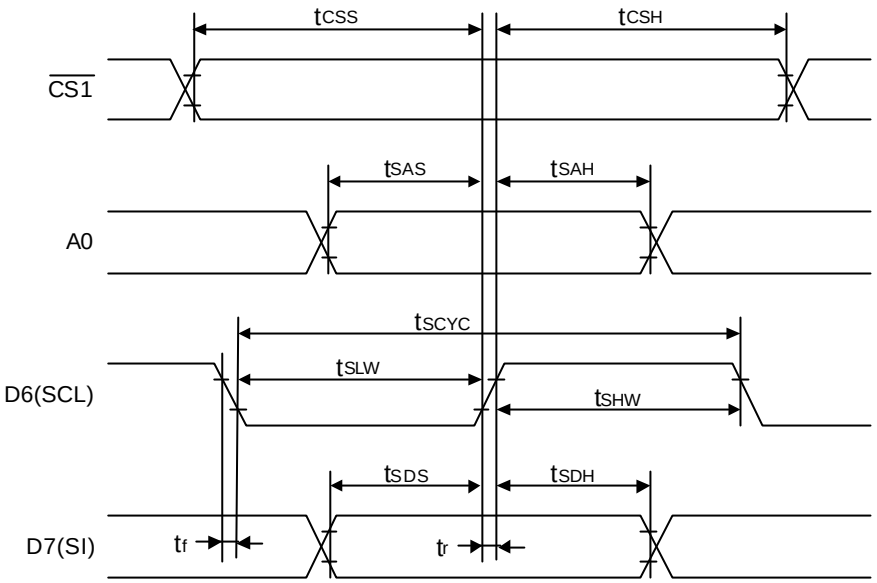
V_{DD}=2.7~4.5V

Parameter	Symbol	Min.	Max.	Units
Serial Clock Cycle	t_{SCYC}	250	-	ns
Serial Clock High Pulse Width	t_{SHW}	100	-	ns
Serial Clock Low Pulse Width	t_{SLW}	100	-	ns
Address Setup Time	t_{SAS}	150	-	ns
Address Hold Time	t_{SAH}	150	-	ns
Data Setup Time	t_{SDS}	100	-	ns
Data Hold Time	t_{SDH}	100	-	ns
CS-SCL Time	t_{CSS}	150	-	ns
	t_{CSH}	150	-	ns
Input Signal Rise/Fall Time	t_r, t_f	-	15	ns

V_{DD}=2.2~2.7V

Parameter	Symbol	Min.	Max.	Units
Serial Clock Cycle	t_{SCYC}	400	-	ns
Serial Clock High Pulse Width	t_{SHW}	150	-	ns
Serial Clock Low Pulse Width	t_{SLW}	150	-	ns
Address Setup Time	t_{SAS}	250	-	ns
Address Hold Time	t_{SAH}	250	-	ns
Data Setup Time	t_{SDS}	150	-	ns
Data Hold Time	t_{SDH}	150	-	ns
CS-SCL Time	t_{CSS}	250	-	ns
	t_{CSH}	250	-	ns
Input Signal Rise/Fall Time	t_r, t_f	-	15	ns

Each timing is specified based on 0.2×VDD and 0.8×VDD.


tCSS
tCSH
CS1
tSAS
tSAH
A0
tSCYC
tSLW
tSHW
D6(SCL)
tSDS
tSDH
D7(SI)
tf
tr

2.3.4. Display Control Timing Characteristics

Reset Input Timing V_{DD}=4.5~5.5V

Parameter	Symbol	Min.	Typ.	Max.	Units
Reset time	t_R	-	-	0.5	µs
Reset "L" Pulse Width	t_{RW}	0.5	-	-	

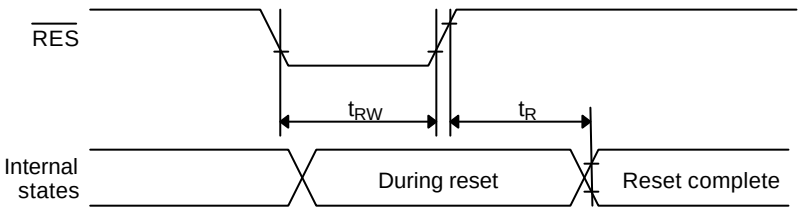
Reset Input Timing V_{DD}=2.7~4.5V

Parameter	Symbol	Min.	Typ.	Max.	Units
Reset time	t_R	-	-	1	µs
Reset "L" Pulse Width	t_{RW}	1	-	-	

Reset Input Timing V_{DD}=2.2~2.7V

Parameter	Symbol	Min.	Typ.	Max.	Units
Reset time	t_R	-	-	1.5	µs
Reset "L" Pulse Width	t_{RW}	1.5	-	-	

Each timing is specified based on 0.2×VDD and 0.8×VDD.



Output Timing V_{DD}=4.5~5.5V

Parameter	Symbol	Min.	Typ.	Max.	Units
FR Delay Time	t_{DFR}	-	10	40	ns

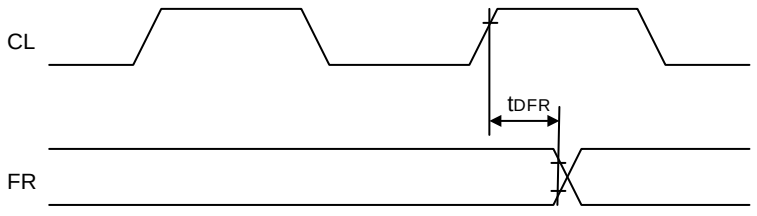
Output Timing V_{DD}=2.7~4.5V

Parameter	Symbol	Min.	Typ.	Max.	Units
FR Delay Time	t_{DFR}	-	10	80	ns

Output Timing V_{DD}=2.2~2.7V

Parameter	Symbol	Min.	Typ.	Max.	Units
FR Delay Time	t_{DFR}	-	50	200	ns

Each timing is specified based on 0.2×VDD and 0.8×VDD.
(The delay time is applied to the master operation only.)



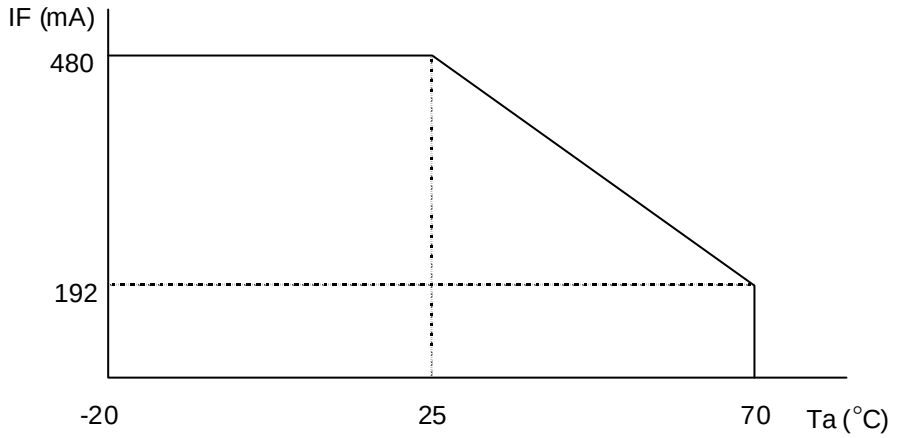
2.4. Lighting Specifications

2.4.1. Absolute Maximum Ratings

Ta=25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Foward Current	I_F	Note 1	-	-	480	mA
Reverse Voltage	V_R	-	-	-	4	V
LED Power Dissipation	P_D	-	-	-	1728	mW

Note 1 : Refer to the foward current derating curve.



2.4.2. Operating Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Foward Voltage	V_F	I_F=240mA	-	3.3	3.6	V
Luminance of Module Surface	L	I_F=240mA	49	70	-	cd/m^2

3.Optical Specifications

3.1. LCD Driving Voltage

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Recommended	V_{DD}-V_5	Ta= -20°C	-	-	11.3	V
LCD Driving Voltage		Ta=25°C	9.6	10.4	11.1	V
Note 1		Ta=70°C	9.1	-	-	V

Note 1 : Voltage (Applied actual waveform to LCD Module) for the best contrast. The range of minimum and maximum shows tolerance of the operating voltage. The specified contrast ratio and response time are not guaranteed over the entire range.

3.2. Optical Characteristics

Ta=25°C, 1/65 Duty, 1/9 Bias, V_{OD}=10.4V (Note 4), θ= 0°, ϕ=-°

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Units
Contrast Ratio Note 1		CR	θ= 0° , ϕ=-°	-	60	-	
Viewing Angle			Shown in 3.3				
Response	Rise Note 2	T_{ON}	-	-	130	200	ms
Time	Decay Note 3	T_{OFF}	-	-	180	270	ms

Note 1 :Contrast ratio is defined as follows. (CR = L_{ON} / L_{OFF})

L_{ON} : Luminance of the ON segments

L_{OFF}: Luminance of the OFF segments

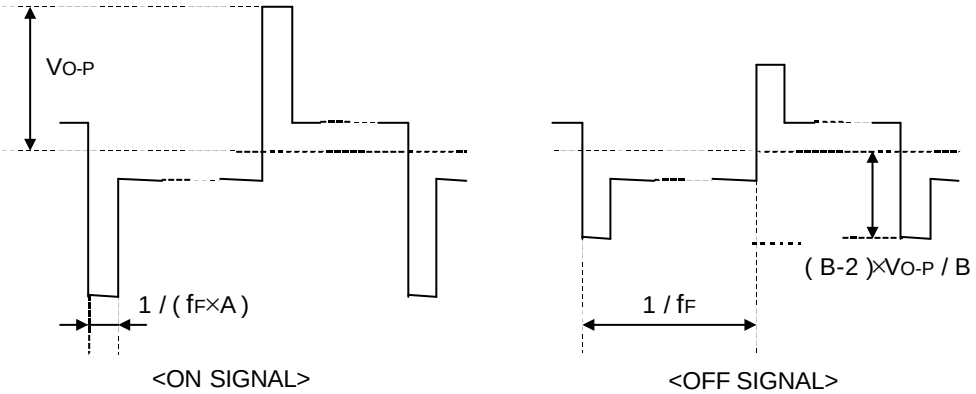
Measuring Spot : 3.0mmϕ

Note 2 :The time that the luminance level reaches 90% of the saturation level from 0% when ON signal is applied.

Note 3 :The time that the luminance level reaches 10% of the saturation level from 100% when OFF signal is applied.

Note 4 :Definition of Driving Voltage V_{OD}

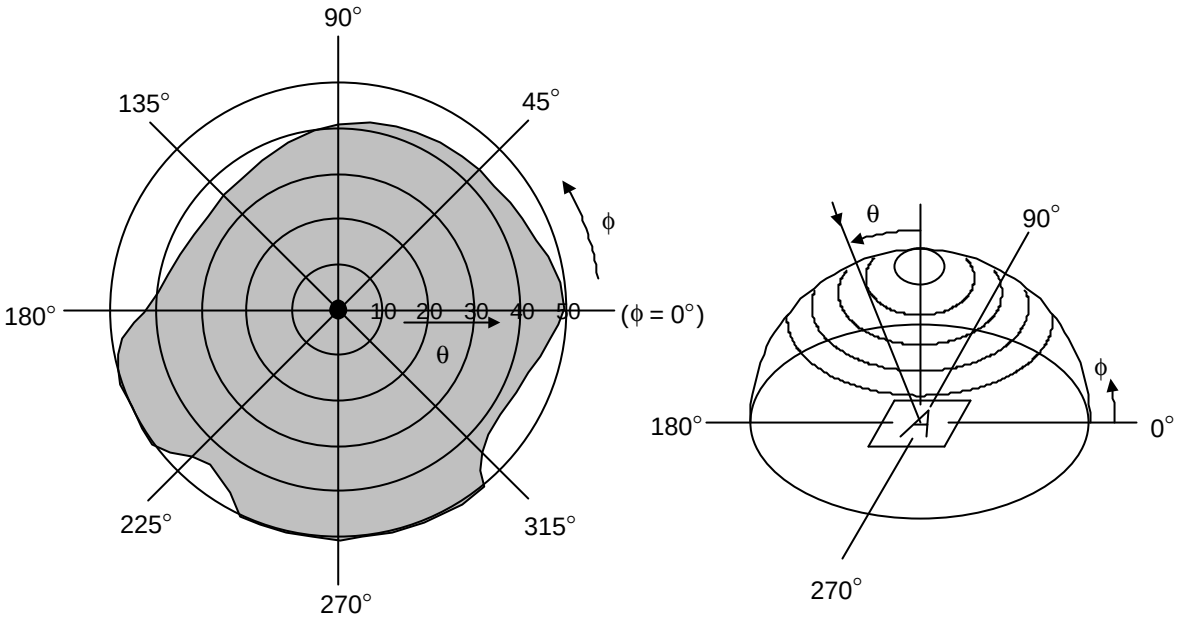
Assuming that the typical driving waveforms shown below are applied to the LCD Panel at 1/A Duty - 1/B Bias (A: Duty Number, B: Bias Number). Driving voltage V_{OD} is defined as the voltage V_{O-P} when the contrast ratio (CR=L_{ON} / L_{OFF}) is at its maximum.



<ON SIGNAL> <OFF SIGNAL>

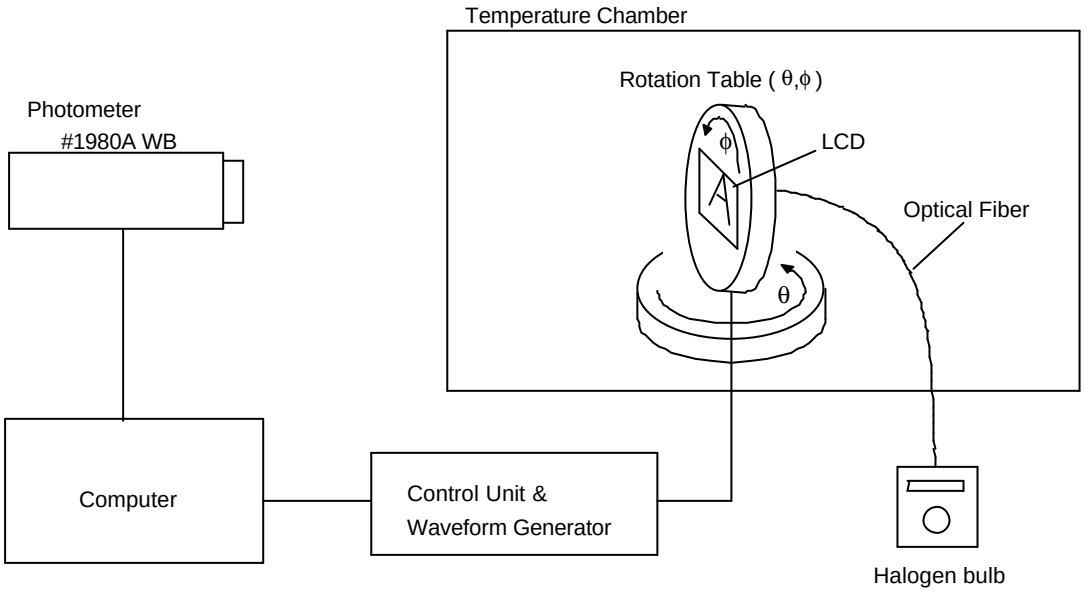
3.3. Definition of Viewing Angle and Optimum Viewing Area

*Point • shows the point where contrast ratio is measured. : θ= 0°, ϕ=-°
*Driving condition: 1/65 Duty, 1/9 Bias, V_{OD}=10.4V, f_F=84.6Hz



*Area ▭ shows typ. CR≥5(Measuring Spot : 3.0mmϕ)

3.4. System Block Diagram



4.I/O Terminal

4.1. Pin Assignment

CN1,CN2

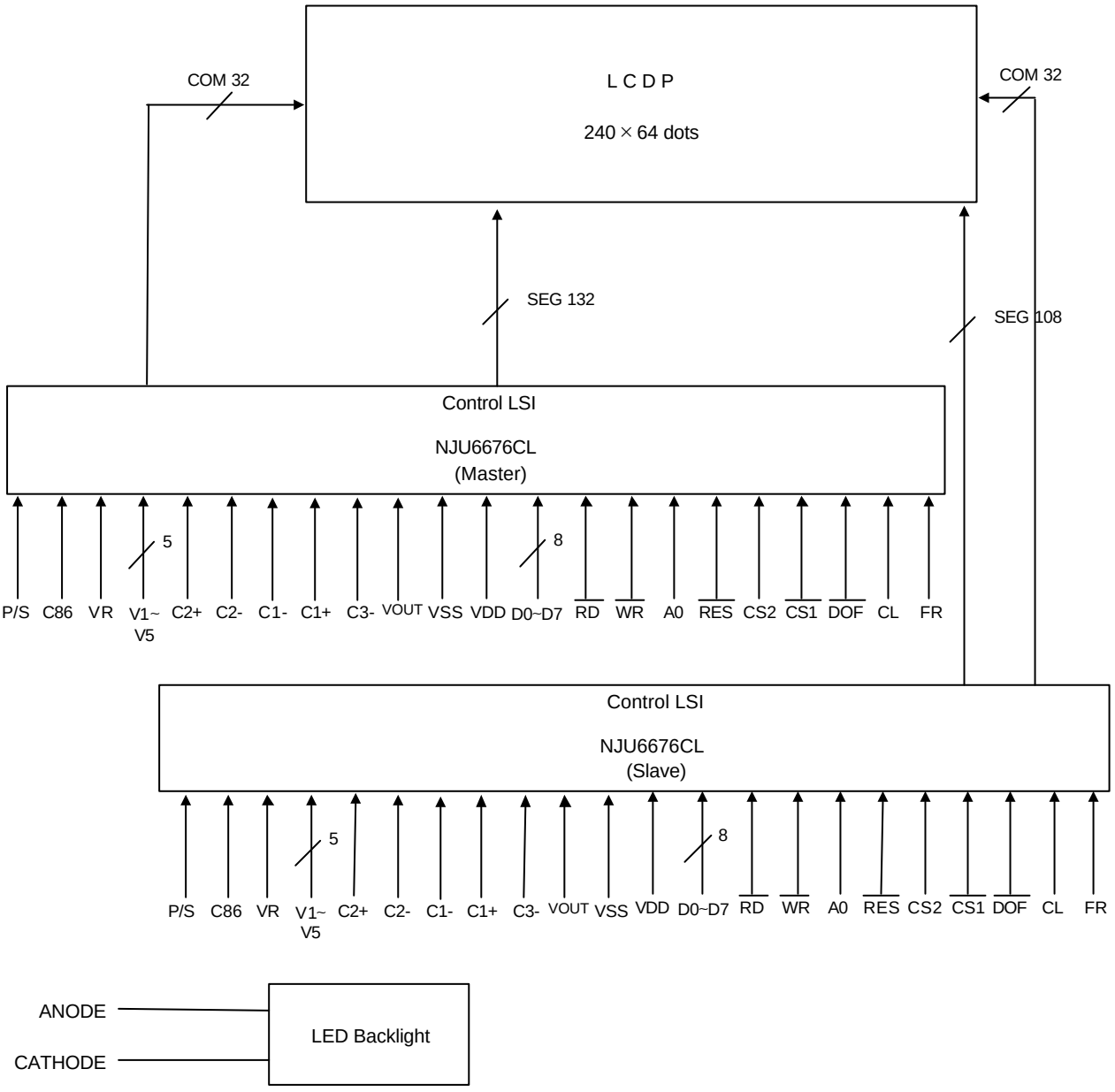
No.	Symbol	Function
1	NC	Non-connection
2	FR	Input/Output for LCD AC Drive
3	CL	Input for Display Clock
4	$\overline{DOF}$	LCD Display Blanking Control Terminal
5	$\overline{CS1}$	Chip Select Signal L : Active
6	CS2	Chip Select Signal H : Active
7	$\overline{RES}$	Reset Signal L : Reset
8	A0	H : D0~D7 are Display Data L : D0~D7 are Instructions
9	$\overline{WR}$	80 family CPU : Write Signal L : Active
10	$\overline{RD}$	80 family CPU : Read Signal L : Active
11	D0	Display Data
12	D1	Display Data
13	D2	Display Data
14	D3	Display Data
15	D4	Display Data
16	D5	Display Data
17	D6(SCL)	Display Data
18	D7(SI)	Display Data
19	V_{DD}	Power Supply for Logic
20	V_{SS}	Power Supply (0V, GND)
21	V_{OUT}	DC/DC Voltage Converter Output
22	C3-	DC/DC Voltage Converter Negative Connection
23	C1+	DC/DC Voltage Converter Positive Connection
24	C1-	DC/DC Voltage Converter Negative Connection
25	C2-	DC/DC Voltage Converter Negative Connection
26	C2+	DC/DC Voltage Converter Positive Connection
27	V_1	Power Supply for LCD Drive $V_1 = 1/9 \cdot V_5$
28	V_2	Power Supply for LCD Drive $V_2 = 2/9 \cdot V_5$
29	V_3	Power Supply for LCD Drive $V_3 = 7/9 \cdot V_5$
30	V_4	Power Supply for LCD Drive $V_4 = 8/9 \cdot V_5$
31	V_5	Power Supply for LCD Drive V_5, V_{OUT}
32	VR	Voltage Adjustment Pin Applies voltage between V_{CC} and V_5 using a resistive divider.
33	C86	Interface Mode Select Signal H : 68 series L : 80 series

34	P/S	Parallel/Serial Data Select Signal H : Parallel L : Serial
35	NC	Non-connection
36	NC	Non-connection

CN3

No.	Symbol	Function
1	ANODE	LED Anode Terminal
2	CATHODE	LED Cathode Terminal

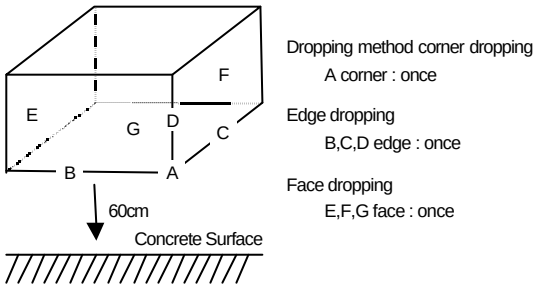
4.2. Block Diagram



5.Test

No change on display and in operation under the following test condition.

Conditions: Unless otherwise specified, tests will be conducted under the following condition.
Temperature: 20±5°C
Humidity : 65±5%RH
tests will be not conducted under functioning state.

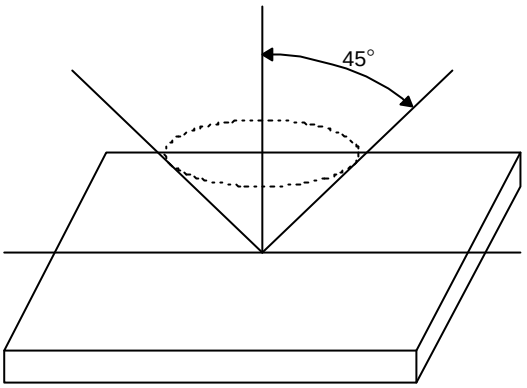
No.	Parameter	Conditions	Notes
1	High Temperature Operating	70°C±2°C, 96hrs (operation state)	
2	Low Temperature Operating	-20°C±2°C, 96hrs (operation state)	1
3	High Temperature Storage	80°C±2°C, 96hrs	2
4	Low Temperature Storage	-30°C±2°C, 96hrs	1,2
5	Damp Proof Test	40°C±2°C,90~95%RH, 96hrs	1,2
6	Vibration Test	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X, Y, Z for each 15 minutes	3
7	Shock Test	To be measured after dropping from 60cm high on the concrete surface in packing state. 	

Note 1 :No dew condensation to be observed.
Note 2 :The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after removed from the test chamber.
Note 3 :Vibration test will be conducted to the product itself without putting it in a container.

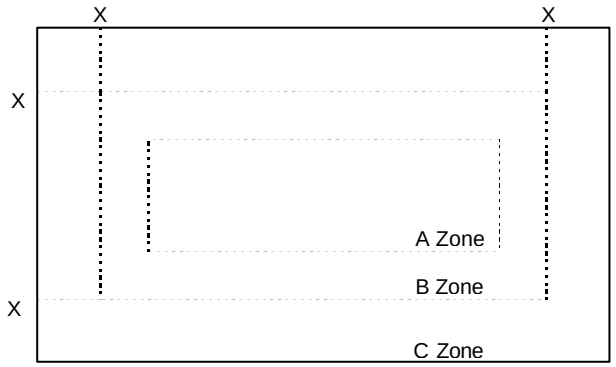
6.Appearance Standards

6.1.Inspection conditions

The LCD shall be inspected under 40W white fluorescent light.
The distance between the eyes and the sample shall be more than 30cm.
All directions for inspecting the sample should be within 45°against perpendicular line.



6.2.Definition of applicable Zones



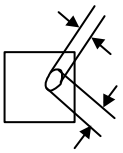
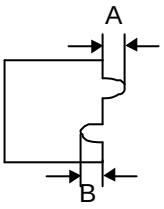
X : Maximum Seal Line

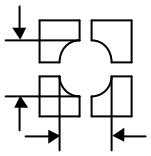
A Zone : Active display area
B Zone : Out of active display area ~ Maximum seal line
C Zone : Rest parts

A Zone + B Zone = Validity viewing area

6.3. Standards(middle scale, LED)

D = (Long + Short) / 2 * : Disregard Units : mm

<table>
<tr><th>No.</th><th>Parameter</th><th>Criteria</th></tr>
<tr><td>1</td><td>The Shape of Dot</td><td>
(1) Pin Hole

<table>
<tr><th>Dimension</th><th>Acceptable Number</th></tr>
<tr><td>D ≤ 0.10</td><td>*</td></tr>
<tr><td>0.10 < D ≤ 0.20</td><td>1 pc / dot or less
5 pcs / cell or less</td></tr>
</table>
(2) Breakage or Chips / Deformation
1.Dot Type


<table>
<tr><th>Dimension</th><th>Acceptable Number</th></tr>
<tr><td>A≤0.10</td><td>*
(Should not be connected to next dot)</td></tr>
<tr><td>0.10<A≤0.15</td><td>1 pc / dot(only segment)or less
5 pcs / cell or less
(Should not be connected to next dot)</td></tr>
<tr><td>B ≤ 0.15</td><td>*</td></tr>
</table>
2.Defective type extends over multiple numbers of dots

<table>
<tr><th>Dimension</th><th>Acceptable Number</th></tr>
<tr><td>D≤0.10</td><td>*</td></tr>
<tr><td>0.10<D≤0.20</td><td>1 pc / dot(only segment)or less
5 pcs / cell or less
(Individual dot must secure 1/2 area or more)</td></tr>
</table>
</td></tr>
</table>

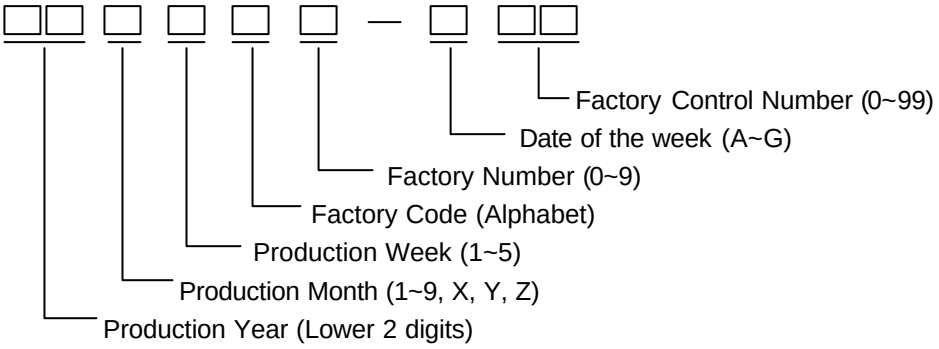
D = (Long + Short) / 2 * : Disregard Units : mm

<table>
<tr><th>No.</th><th>Parameter</th><th>Criteria</th></tr>
<tr><td>2</td><td>Black and White Spots, Foreign Substances</td><td>(1) Round Shape
<table>
<tr><th>Zone / Dimension</th><th>Acceptable Number</th><th></th><th></th></tr>
<tr><td></td><td>A</td><td>B</td><td>C</td></tr>
<tr><td>D ≤ 0.10</td><td>*</td><td>*</td><td>*</td></tr>
<tr><td>0.10< D ≤ 0.20</td><td>6</td><td>6</td><td>*</td></tr>
<tr><td>0.20< D ≤ 0.30</td><td>4</td><td>4</td><td>*</td></tr>
</table>
Individual dot must secure 1/2 area or more.

(2) Line Shape
<table>
<tr><th>Length \ Zone / Width</th><th></th><th>Acceptable Number</th><th></th><th></th></tr>
<tr><td></td><td></td><td>A</td><td>B</td><td>C</td></tr>
<tr><td>*</td><td>W≤0.03</td><td>*</td><td>*</td><td>*</td></tr>
<tr><td>L ≤2.0</td><td>0.03<W≤0.05</td><td>5</td><td>5</td><td>*</td></tr>
<tr><td>L ≤1.0</td><td>≤0.10</td><td>4</td><td>4</td><td>*</td></tr>
<tr><td>*</td><td>0.10<W</td><td colspan="2">In the same way (1)</td><td>*</td></tr>
</table>
No more than 9pcs as total.
(Refer to “Complex Foreign Substance Defects”)</td></tr>
<tr><td>3</td><td>Color Variation</td><td>Not to be conspicuous defects.</td></tr>
<tr><td>4</td><td>Air Bubbles (between glass & polarizer)</td><td>
<table>
<tr><th>Zone / Dimension</th><th>Acceptable Number</th><th></th><th></th></tr>
<tr><td></td><td>A</td><td>B</td><td>C</td></tr>
<tr><td>D ≤ 0.30</td><td>*</td><td>*</td><td>*</td></tr>
<tr><td>0.30< D ≤ 0.40</td><td>3</td><td>*</td><td>*</td></tr>
<tr><td>0.40< D ≤ 0.60</td><td>2</td><td>3</td><td>*</td></tr>
</table>
No more than 3pcs as total.
(Refer to “Complex Foreign Substance Defects”)</td></tr>
<tr><td>5</td><td>Polarizer Scratches</td><td>Not to be conspicuous defects.</td></tr>
<tr><td>6</td><td>Polarizer Dirts</td><td>If the stains are removed easily from LCDP surface, the module is not defective.</td></tr>
<tr><td>7</td><td>Complex Foreign Substance Defects</td><td>Black spots, line shaped foreign substances or air bubbles between glass & polarizer should be 9pcs maximum in total.</td></tr>
<tr><td>8</td><td>Distance between Different Foreign Substance Defects</td><td>20mm or more</td></tr>
</table>

7.Code System of Production Lot

The production lot of module is specified as follows.



8.Type Number

The type number of module is specified as follows.

F-51851GNFQJ-LY-ADN

9.Applying Precautions

Please contact us when questions and/or new problems not specified in this Specifications arise.

10.Precautions Relating Product Handling

The Following precautions will guide you in handling our product correctly.

1) Liquid crystal display devices
   1. The liquid crystal display device panel used in the liquid crystal display module is made of plate glass. Avoid any strong mechanical shock. Should the glass break handle it with care.
   2. The polarizer adhering to the surface of the LCD is made of a soft material. Guard against scratching it.

2) Care of the liquid crystal display module against static electricity discharge.
   1. When working with the module, be sure to ground your body and any electrical equipment you may be using. We strongly recommend the use of anti static mats (made of rubber), to protect work tables against the hazards of electrical shock.
   2. Avoid the use of work clothing made of synthetic fibers. We recommend cotton clothing or other conductivity-treated fibers.
   3. Slowly and carefully remove the protective film from the LCD module, since this operation can generate static electricity.

3) When the LCD module alone must be stored for long periods of time:
   1. Protect the modules from high temperature and humidity.
   2. Keep the modules out of direct sunlight or direct exposure to ultraviolet rays.
   3. Protect the modules from excessive external forces.

4) Use the module with a power supply that is equipped with an overcurrent protector circuit,since the module is not provided with this protective feature.

5) Do not ingest the LCD fluid itself should it leak out of a damaged LCD module. Should hands or clothing come in contact with LCD fluid, wash immediately with soap.

6) Conductivity is not guaranteed for models that use metal holders where solder connections between the metal holder and the PCB are not used. Please contact us to discuss appropriate ways to assure conductivity.

7) For models which use CFL:
   1. High voltage of 1000V or greater is applied to the CFL cable connector area. Care should be taken not to touch connection areas to avoid burns.
   2. Protect CFL cables from rubbing against the unit and thus causing the wire jacket to become worn.
   3. The use of CFLs for extended periods of time at low temperatures will significantly shorten their service life.

8) For models which use touch panels:
   1. Do not stack up modules since they can be damaged by components on neighboring modules.
   2. Do not place heavy objects on top of the product. This could cause glass breakage.

9) For models which use COG,TAB,or COF:
   1. The mechanical strength of the product is low since the IC chip faces out unprotected from the rear. Be sure to protect the rear of the IC chip from external forces.
   2. Given the fact that the rear of the IC chip is left exposed, in order to protect the unit from electrical damage, avoid installation configurations in which the rear of the IC chip runs the risk of making any electrical contact.

10) Models which use flexible cable, heat seal, or TAB:
   1. In order to maintain reliability, do not touch or hold by the connector area.
   2. Avoid any bending, pulling, or other excessive force, which can result in broken connections.

11) In case of buffer material such as cushion / gasket is assembled into LCD module, it may have an adverse effect on connecting parts (LCD panel-TCP / HEAT SEAL / FPC / etc., PCB-TCP / HEAT SEAL / FPC etc., TCP-HEAT SEAL, TCP-FPC, HEAT SEAL-FPC, etc.,) depending on its materials.
   Please check and evaluate these materials carefully before use.

12) In case of acrylic plate is attached to front side of LCD panel, cloudiness (very small cracks) can occur on acrylic plate, being influenced by some components generated from polarizer film..
   Please check and evaluate those acrylic materials carefully before use.

11.Warranty

This product has been manufactured to your company's specifications as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in medical devices, nuclear power control equipment, aerospace equipment, fire and security systems, or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required. If the product is to be used in any of the above applications, we will need to enter into a separate product liability agreement.

1. We cannot accept responsibility for any defect, which may arise from additional manufacturing of the product (including disassembly and reassembly), after product delivery.

2. We cannot accept responsibility for any defect, which may arise after the application of strong external force to the product.

3. We cannot accept responsibility for any defect, which may arise due to the application of static electricity after the product has passed your company's acceptance inspection procedures.

4. When the product is in CFL models, CFL service life and brightness will vary According to the performance of the inverter used, leaks, etc. We cannot accept responsibility for product performance, reliability, or defect, which may arise.

5. We cannot accept responsibility for intellectual property of a third party, which may arise through the application of our product to your assembly with exception to those issues relating directly to the structure or method of manufacturing of our product.

6. Optrex will not be held responsible for any quality guarantee issue for defect products judged as Optrex-origin longer than 2 (two) years from Optrex production or 1(one) year from Optrex, Optrex America, Optrex Europe delivery which ever comes later.