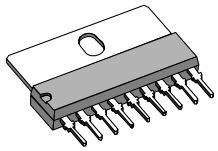
TDA8133

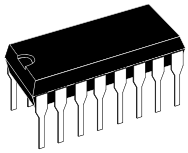
+5.1 V and +8 V dual voltage regulator with disable and reset functions

Features

- Input voltage range: 7 V to 18 V
- Output currents up to 750 mA
- Fixed precision output 1 voltage: 5.1 V ±2%
- Fixed precision output 2 voltage: 8 V ±2%
- Output 1 with reset function
- Output 2 with disable function by TTL Input
- Short-circuit protection at both outputs
- Thermal protection
- Low dropout voltage



SIP9 (plastic package)



DIP16 (8 + 8)

Table 1. Device summary

Order code	Packaging
TDA8133	Tray
TDA8133D	Tray

Description

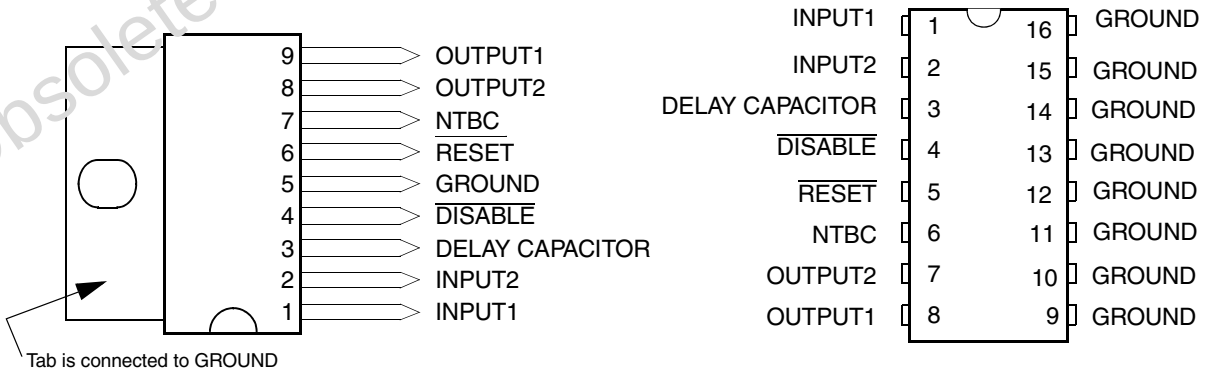
The TDA8133 and the TDA8133D are monolithic dual positive voltage regulators designed to provide fixed precision output voltages of 5.1 V and 8.0 V for currents up to 750 mA.

An internal reset circuit generates a reset pulse when the voltage of output 1 drops below the regulated voltage value.

Output 2 can be disabled via the TTL input.

Short-circuit and thermal protections are included in all versions.

Figure 1. TDA8133 and TDA8133D



Contents

1 Description

Figure 2. TDA8133 block diagram

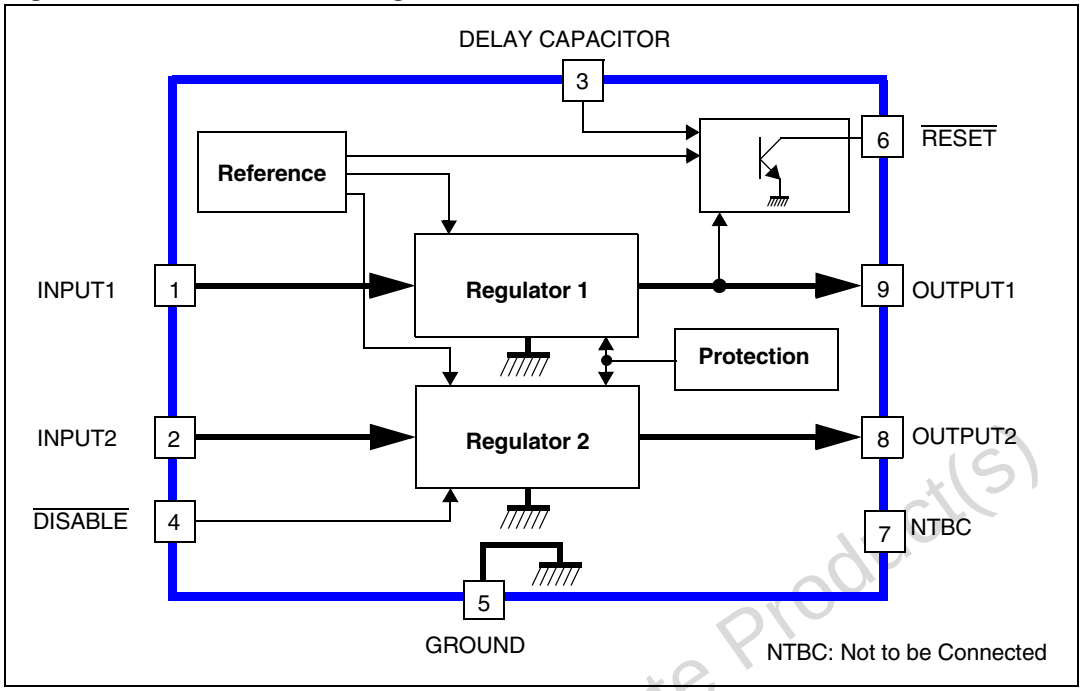
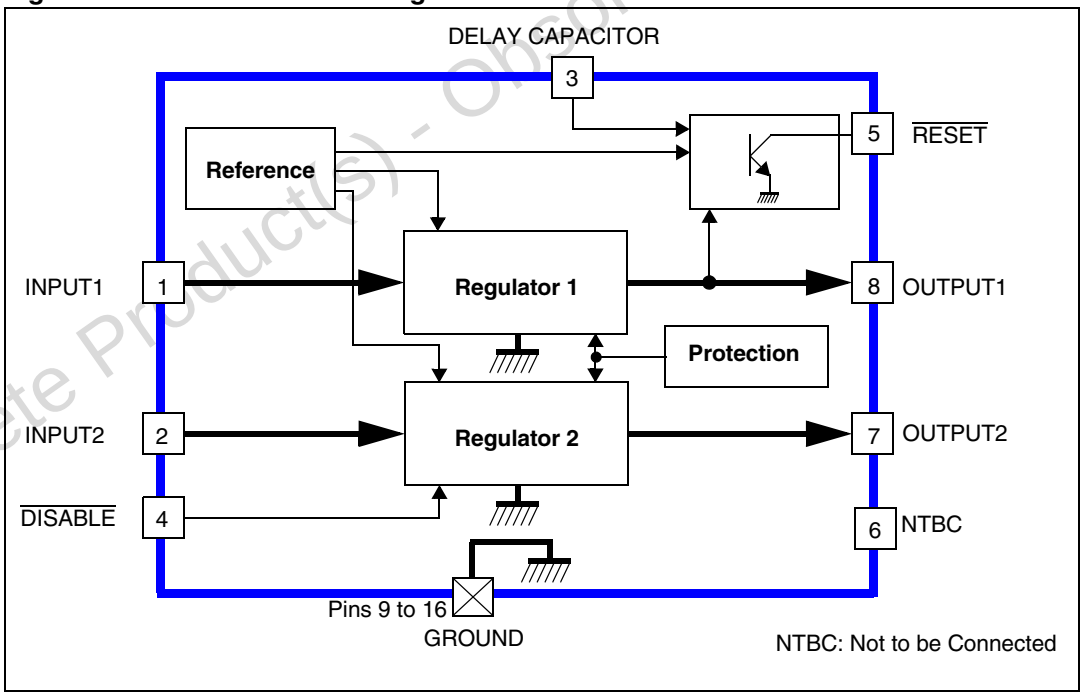


Figure 3. TDA8133D block diagram



2 Electrical characteristics

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	DC input voltage at pins INPUT1 and INPUT2	20	V
V_{DIS}	Disable input voltage at pin $\overline{DISABLE}$	20	V
V_{RST}	Output voltage at pin $\overline{RESET}$	20	V
$I_{O1,2}$	Output currents	Internally limited	
P_t	Power dissipation	Internally limited	
T_{STG}	Storage temperature	-65 to +150	°C
T_J	Junction temperature	0 to +150	°C

Table 3. Thermal data

Symbol	Parameter		Value	Unit
R_{thJC}	Thermal resistance (junction-to-case)	TDA8133 TDA8133D	9 15	°C/W
R_{thJA}	Thermal resistance (1) (junction-to-ambient)	TDA8133 TDA8133D	50 56	°C/W
T_J	Maximum recommended junction temperature		140	°C
T_{OPER}	Operating free air temperature range		0 to +70	°C

1. Mounted on board. For more information, refer to *Section 5*.

Table 4. Electrical characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Output voltage	I_{O1} = 10 mA	5	5.1	5.2	V
V_{O2}	Output voltage	I_{O2} = 10 mA	7.84	8.00	8.16	V
$V_{IO1,2}$	Dropout voltage	$I_{O1,2}$ = 750 mA			1.4	V
$V_{O1,2LI}$	Line regulation	7 V < V_{IN1} < 14 V 10 V < V_{IN2} < 14 V $I_{O1,2}$ = 200 mA			50 80	mV
$V_{O1,2LO}$	Load regulation	5 mA < I_{O1} < 600 mA 5 mA < I_{O2} < 600 mA			100 160	mV
I_Q	Quiescent current	I_{O1} = 10 mA, OUTPUT2 Disabled			2	mA
V_{O1RST}	Reset threshold voltage	K = V_{O1}, $V_{IN1} \geq$ 7 V	K - 0.4	K - 0.25	K - 0.1	V
V_{RTH}	Reset threshold hysteresis	See circuit description	20	50	75	mV
t_{RD}	Reset pulse delay	C_e = 100 nF See circuit description		25		ms

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{RL}	Saturation voltage in reset condition	$I_{\overline{RESET}}$ = 5 mA			0.4	V
I_{RH}	Leakage current in normal condition	$V_{\overline{RESET}}$= 10 V			10	µA
$K_{O1, 2}$	Output voltage thermal drift	$K_0 = \frac{\Delta V_0 \cdot 10^6}{\Delta T \cdot V_0}$ T_J = 0 to + 125°C		100		ppm/°C
$I_{O1,2SC}$	Short circuit output current	V_{IN1} = 7 V, V_{IN2} = 10 V $V_{IN1,2}$ = 16 V(1)			1.6 1.0	A
V_{DISH}	Disable voltage when pin $\overline{DISABLE}$ is high (OUTPUT2 active)		2			V
V_{DISL}	Disable voltage when pin $\overline{DISABLE}$ is low (OUTPUT2 disabled)				0.8	V
I_{DIS}	Disable bias current	0 V < V_{DIS} < 7 V	-100		2	µA
T_{JSD}	Junction temperature for thermal shutdown			145		°C

1. The output short-circuit currents are tested one channel at time. During a short-circuit, a large consumption of power occurs, but the thermal protection circuit prevents any excessive temperatures. A safe permanent short-circuit protection is only guaranteed for input voltages up to 16 V.

Note: T_{AMB} = 25° C, V_{IN1} = 7 V, V_{IN2} = 10 V, unless otherwise specified.

3 Circuit description

The TDA8133 and the TDA8133D are dual-voltage regulators with reset and disable functions.

The two regulation parts are supplied from a single voltage reference circuit trimmed by zener zapping during EWS testing. Since the supply voltage of this voltage reference is connected to pin INPUT1 (V_{IN1}), the second regulator will not work if pin INPUT1 is not supplied.

The output stages are designed using a Darlington configuration with a typical dropout voltage of 1.2 V.

The disable circuit will switch off pin OUTPUT2 if a voltage less than 0.8 V is applied to pin $\overline{\text{DISABLE}}$.

The reset circuit checks the voltage at pin OUTPUT1. If this voltage drops below V_{O1} - 0.25 V (4.85 V Typ.), the "a" comparator (*Figure 4*) rapidly discharges the external capacitor (Ce) and the reset output immediately switches to low. When the voltage at pin OUTPUT1 exceeds V_{O1} - 0.2 V (4.9 V Typ.), the V_{Ce} voltage increases linearly to the reference voltage (V_{REF} = 2.5 V) corresponding to a reset pulse delay (t_{RD}) as shown in *Figure 5*.

$$t_{RD} = \frac{C_e \times 2.5V}{10\mu A}$$

Afterwards, the reset output returns to high. To avoid glitches in the reset output, the second comparator "b" has a large hysteresis (1.9 V).

Figure 4. Reset diagram

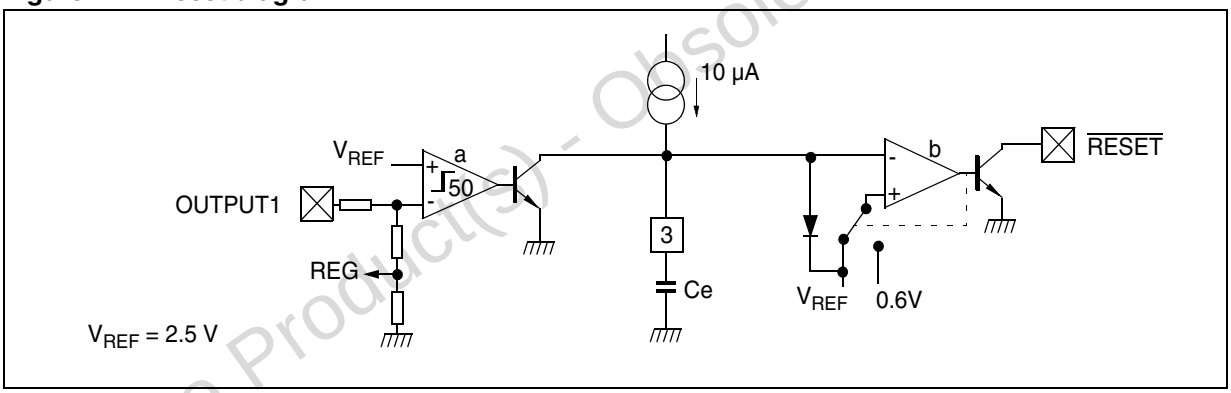
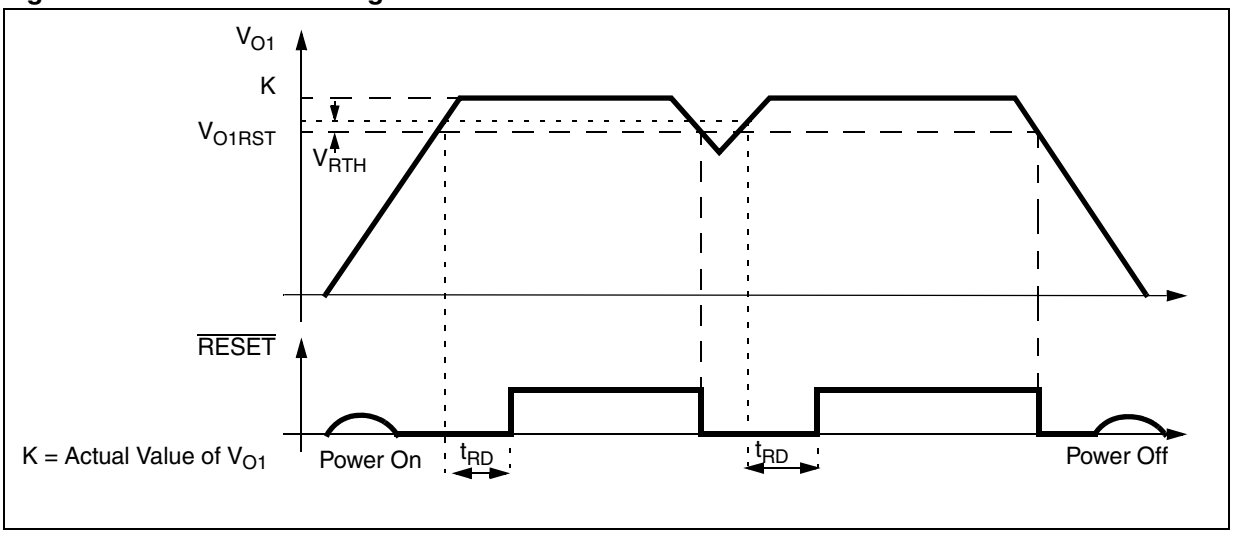


Figure 5. Internal reset diagram



4 Application diagrams

Figure 6. TDA8133 typical application

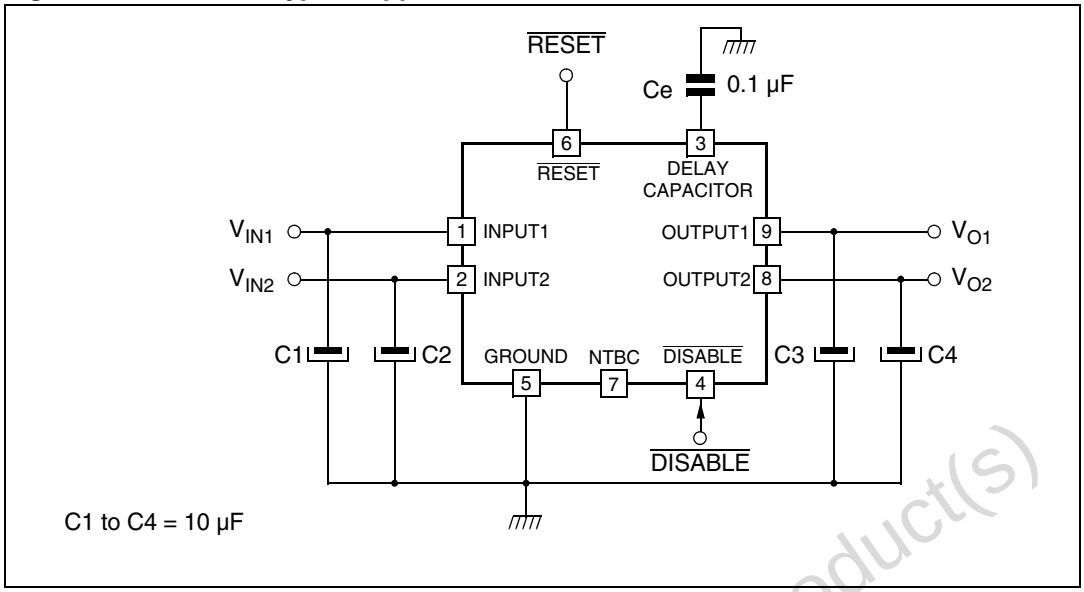
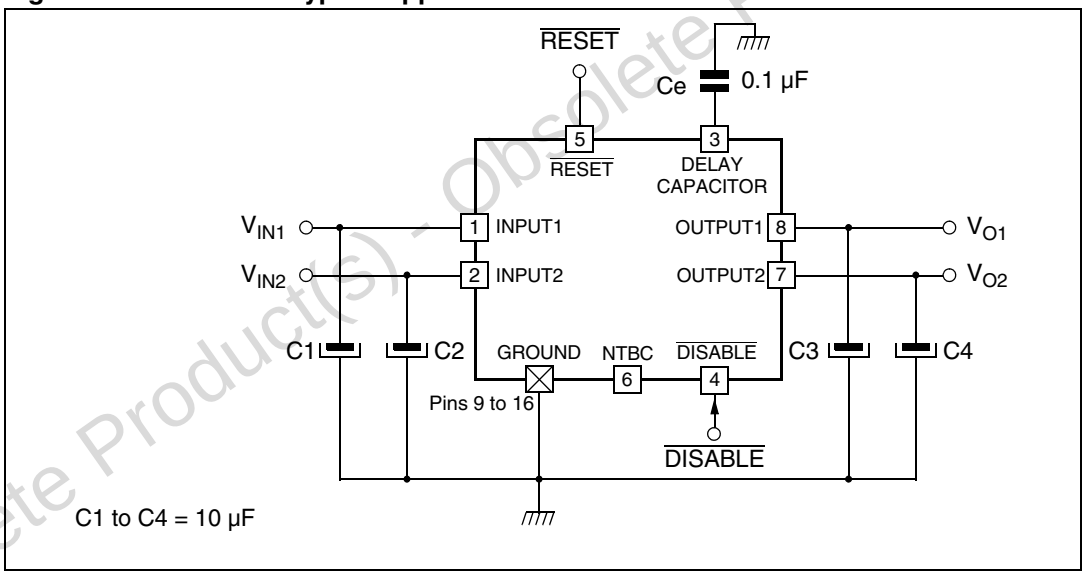


Figure 7. TDA8133D typical application



5 Power dissipation and layout indications

The power is mainly dissipated by the two device buffers. It can be calculated by the equation:

$P = (V_{IN1}-V_{O1}) \times I_{O1} + (V_{IN2}-V_{O2}) \times I_{O2}$

The following table lists the different R_{thJA} values of these packages with or without a heat sink and the corresponding maximum power dissipation assuming:

- Maximum ambient temperature = 70° C
- Maximum junction temperature = 140° C

Table 5. Power dissipation

Device	Heat Sink	R_{thJA} in °C/W	P_{MAX} in W
TDA8133	No	50	1.4
	Yes	20	3.5
TDA8133D	No	56 to 40	1.25 to 1.75
	Yes	32	2.2

Figure 8. Thermal resistance (junction-to-ambient) for DIP16 package without heatsink

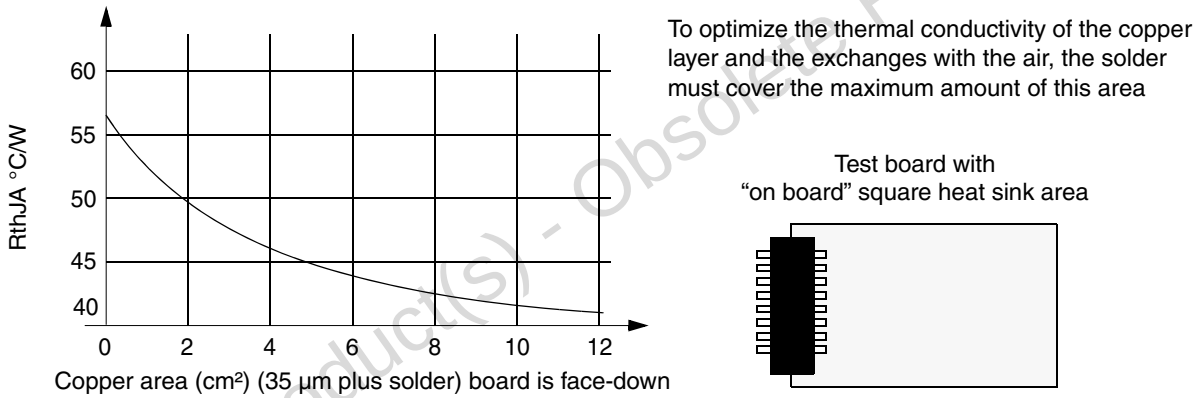
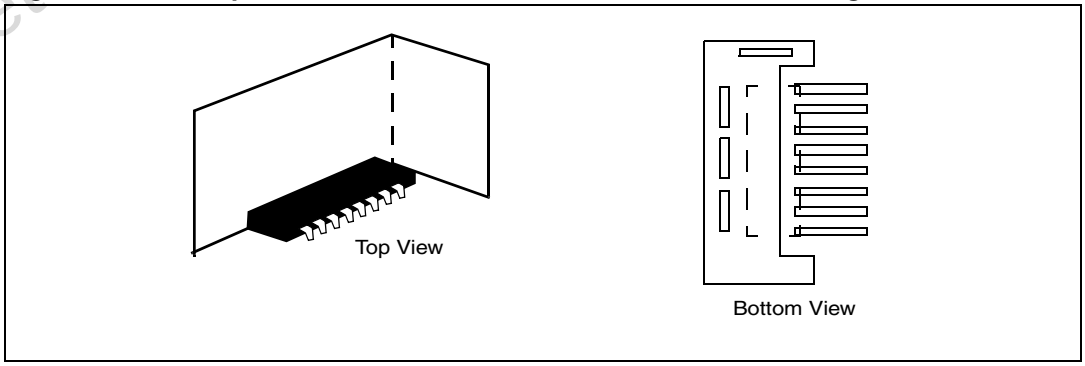


Figure 9. Metal plate mounted near the TDA8133D for heatsinking



6 Package mechanical data

Figure 10. 9-pin plastic single in-line package

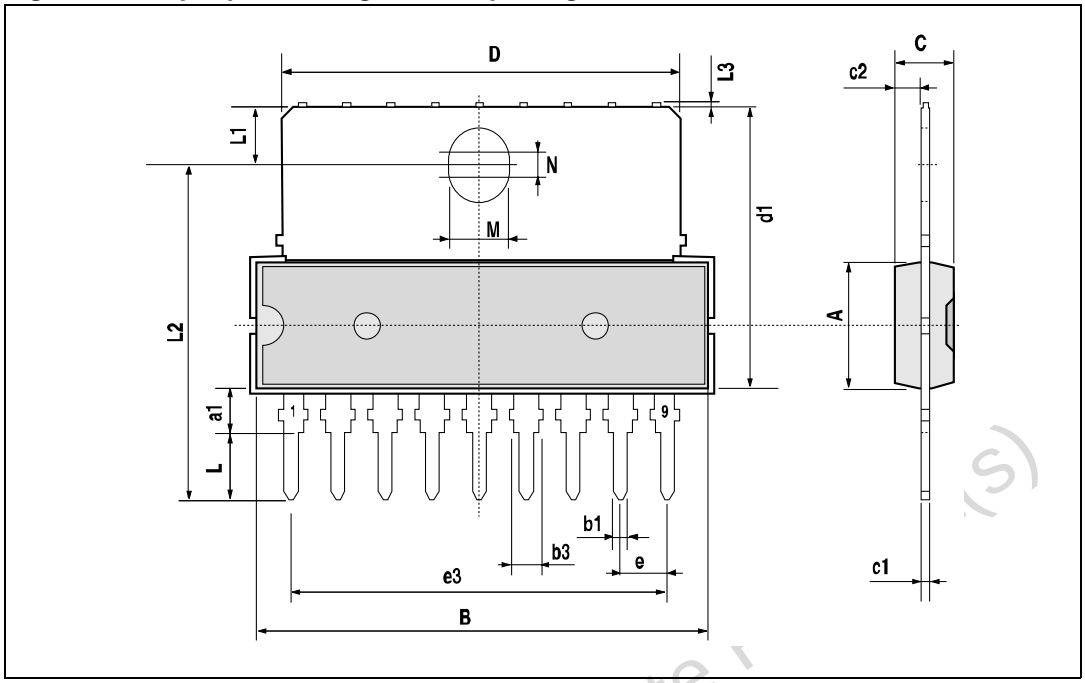


Table 6. 9-pin plastic single in-line package dimensions

Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			7.1			0.280
a1	2.7		3	0.106		0.118
B			24.8			0.976
b1		0.5			0.020	
b3	0.85		1.6	0.033		0.063
C		3.3			0.130	
c1		0.43			0.017	
c2		1.32			0.052	
D			21.2			0.835
d1		14.5			0.571	
e		2.54			0.100	
e3		20.32			0.800	
L	3.1			1.122		
L1		3			0.116	
L2		17.6			0.693	

Table 6. 9-pin plastic single in-line package dimensions (continued)

Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
L3			0.25			0.010
M		3.2			0.126	
N		1			0.039	

Figure 11. 16-pin plastic dual in-line package, 300 mil width

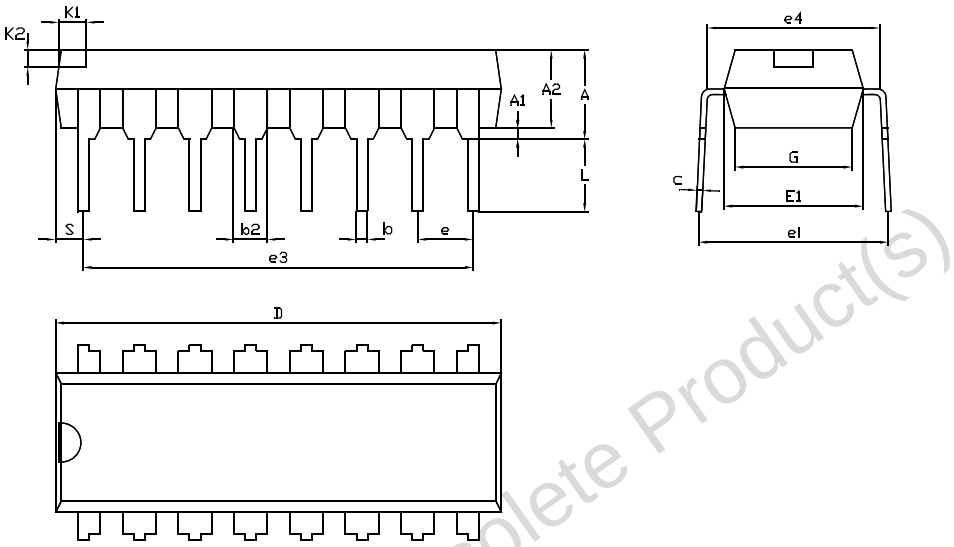


Table 7. 16-pin plastic dual in-line package dimensions

Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36		0.56	0.014		0.022
b2		1.52	1.78		0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	18.67	19.18	19.69	0.735	0.755	0.775
e		2.54			0.100	
E1	6.10	6.35	7.11	0.240	0.250	0.280
L	2.92	3.30	3.81	0.115	0.130	0.150

6.1 Environmentally-friendly packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance.

ECOPACK specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK is an ST trademark.

7 Revision history

Table 8. Document revision history

Date	Revision	Changes
March 1994	1.0	First issue
July 2001	1.1	Datasheet update and addition of DIP16 package
August 2001	1.2	General update; DISABLE pin renamed $\overline{\text{DISABLE}}$ (function remains unchanged)
September 2001	1.3	Thermal data updated
October 2001	1.4	Thermal data updated. *Figure 2* and *Figure 3* updated
05-Mar-2009	2	Preliminary banner removed, template updated and *Section 6.1* added