

NP33N075YDF

R07DS0363EJ0100

Rev.1.00

Jun 30, 2011

MOS FIELD EFFECT TRANSISTOR

Description

The NP33N075YDF is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Low on-state resistance
— $R_{DS(on)} = 28 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 10 \text{ V}$, $I_D = 17 \text{ A}$)
- Low C_{iss} : $C_{iss} = 1300 \text{ pF TYP.}$ ($V_{DS} = 25 \text{ V}$, $V_{GS} = 0 \text{ V}$)
- Logic level drive type
- Designed for automotive application and AEC-Q101 qualified
- Small size package 8-pin HSON

Ordering Information

Part No.	Lead Plating	Packing		Package
NP33N075YDF-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	8-pin HSON
NP33N075YDF-E2-AY *1			Taping (E2 type)	

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	75	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 33	A
Drain Current (pulse) *1	$I_{D(pulse)}$	± 66	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	92	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$) *2	P_{T2}	1.0	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +175	$^\circ\text{C}$
Repetitive Avalanche Current *3	I_{AR}	21	A
Repetitive Avalanche Energy *3	E_{AR}	44	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.63	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	150	$^\circ\text{C/W}$

Notes: *1. $T_C = 25^\circ\text{C}$, $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

*2. Mounted on glass epoxy substrate of 40 mm x 40 mm x 1.6 mm with 4% copper area (35 μm)

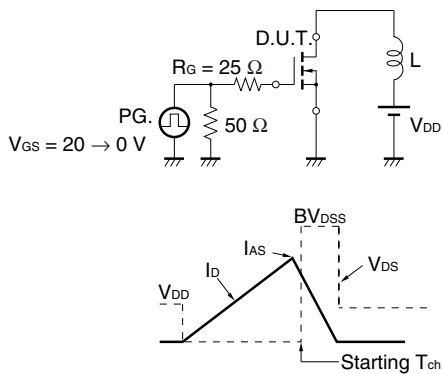
*3. $T_{ch(peak)} \leq 150^\circ\text{C}$, $R_G = 25 \Omega$

Electrical Characteristics (T_A = 25°C)

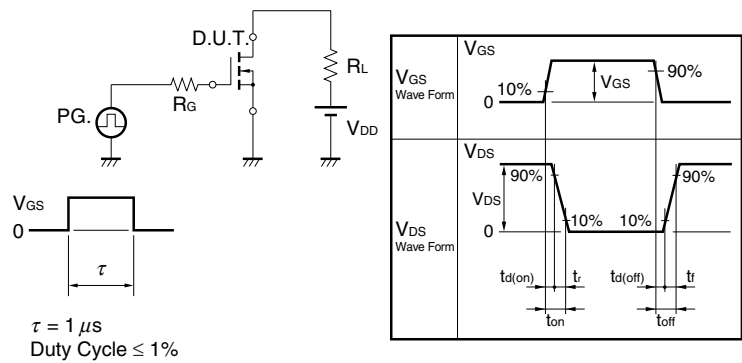
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			1	μA	V _{DS} = 75 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}			±100	nA	V _{GS} = ±20 V, V _{DS} = 0 V
Gate to Source Threshold Voltage	V _{GS(th)}	1.5	2.0	2.5	V	V _{DS} = V _{GS} , I _D = 250 μA
Forward Transfer Admittance *1	y _{fs}	15	30		S	V _{DS} = 5 V, I _D = 17 A
Drain to Source On-state Resistance *1	R _{DS(on)1}		23	28	mΩ	V _{GS} = 10 V, I _D = 17 A
	R _{DS(on)2}		25	32	mΩ	V _{GS} = 5 V, I _D = 17 A
	R _{DS(on)3}		26	35	mΩ	V _{GS} = 4.5 V, I _D = 17 A
Input Capacitance	C _{iss}		1300	2000	pF	V _{DS} = 25 V,
Output Capacitance	C _{oss}		150	200	pF	V _{GS} = 0 V,
Reverse Transfer Capacitance	C _{rss}		60	110	pF	f = 1 MHz
Turn-on Delay Time	t _{d(on)}		15	30	ns	V _{DD} = 38 V, I _D = 17 A, V _{GS} = 10 V, R _G = 0 Ω
Rise Time	t _r		4	10	ns	
Turn-off Delay Time	t _{d(off)}		45	90	ns	
Fall Time	t _f		6	15	ns	
Total Gate Charge	Q _G		28	42	nC	V _{DD} = 60 V, V _{GS} = 10 V, I _D = 33 A
Gate to Source Charge	Q _{GS}		5		nC	
Gate to Drain Charge	Q _{GD}		7		nC	
Body Diode Forward Voltage *1	V _{F(S-D)}		0.9	1.5	V	I _F = 33 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		40		ns	I _F = 33 A, V _{GS} = 0 V,
Reverse Recovery Charge	Q _{rr}		61		nC	di/dt = 100 A/μs

Note: *1. Pulsed test

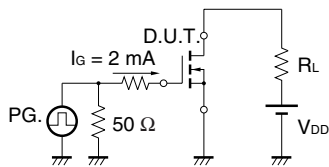
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

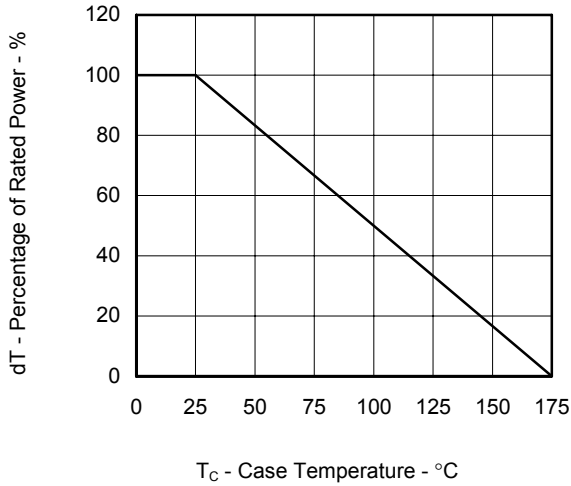


TEST CIRCUIT 3 GATE CHARGE

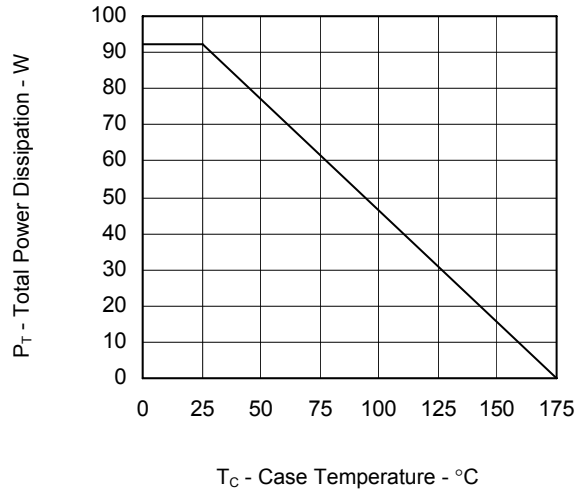


Typical Characteristics (T_A = 25°C)

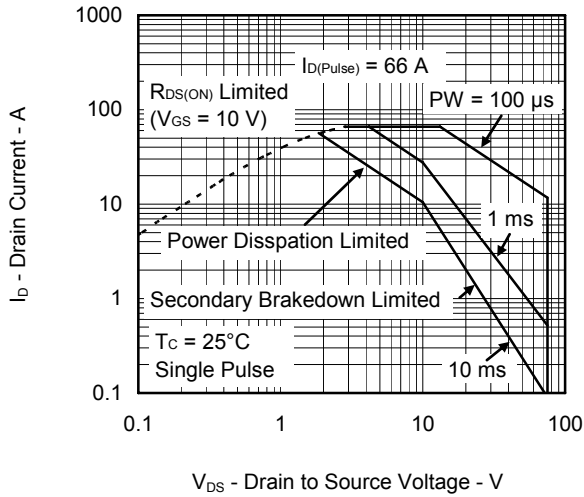
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



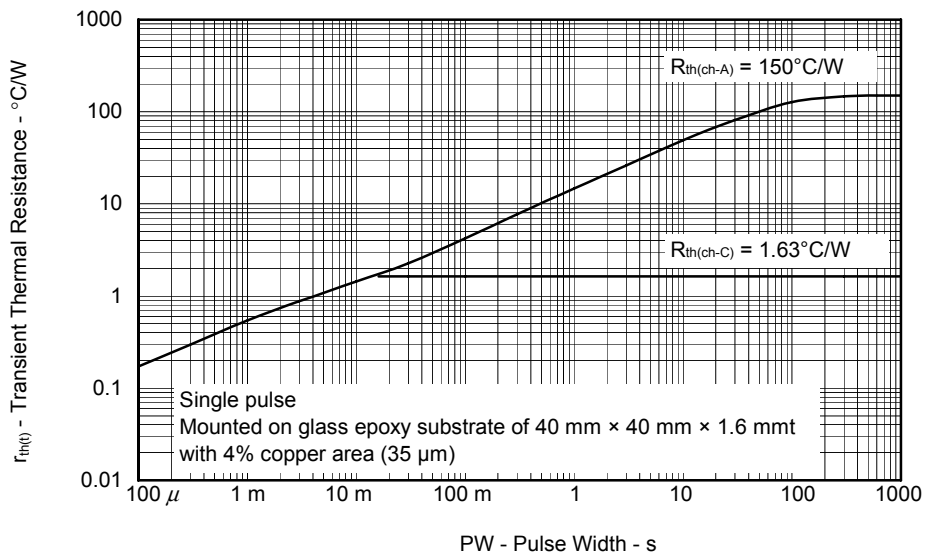
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



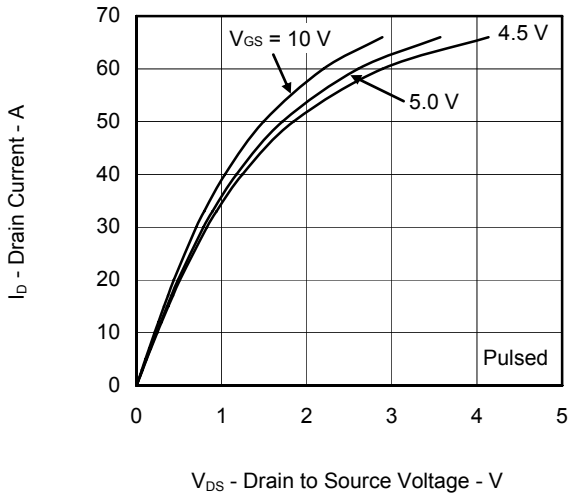
FORWARD BIAS SAFE OPERATING AREA



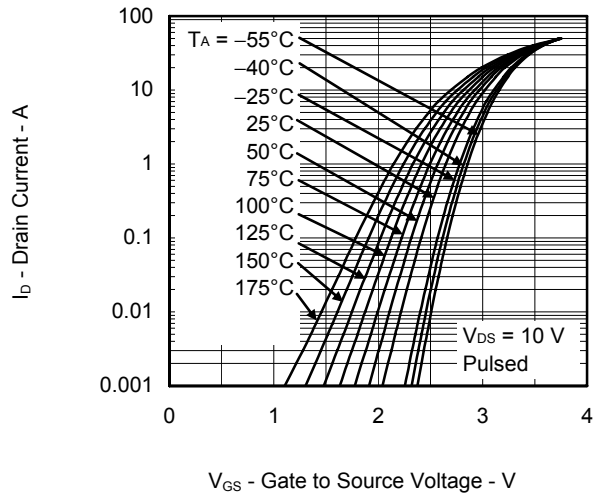
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



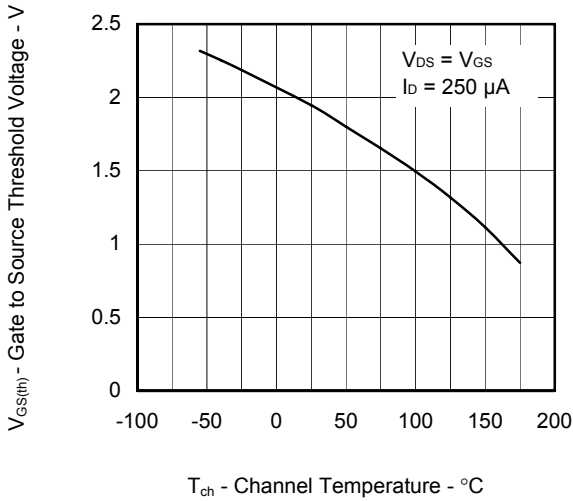
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



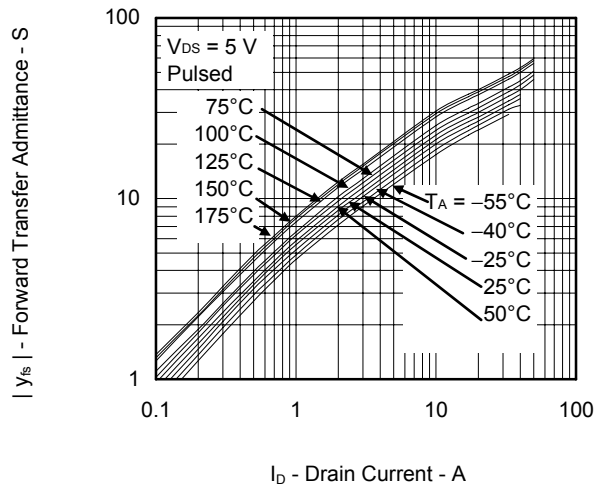
FORWARD TRANSFER CHARACTERISTICS



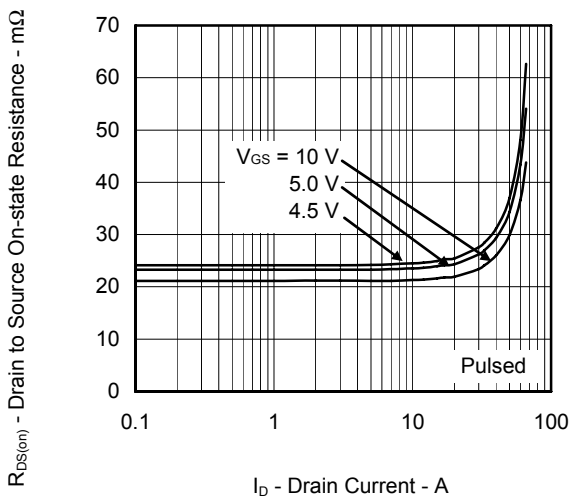
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



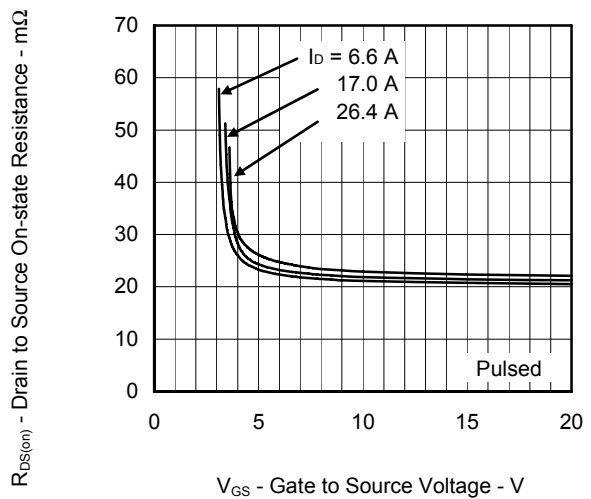
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



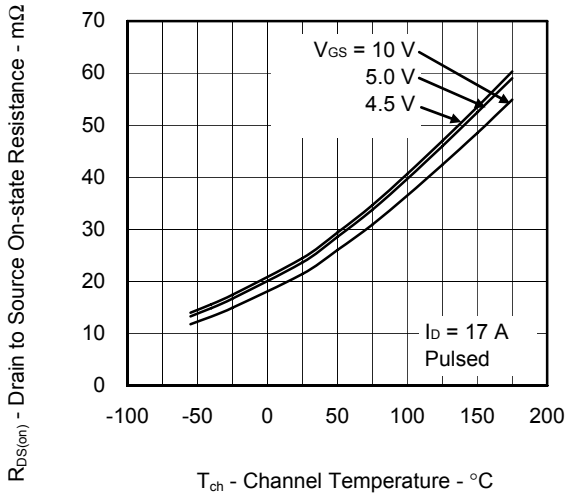
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



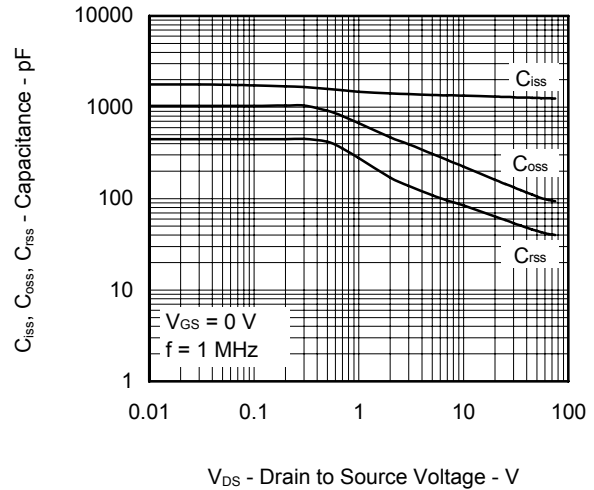
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



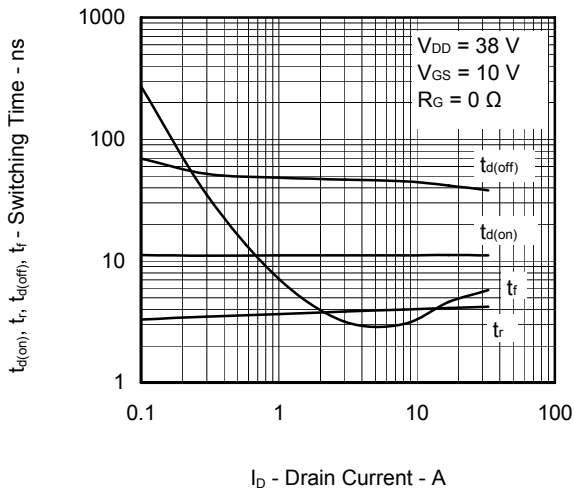
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



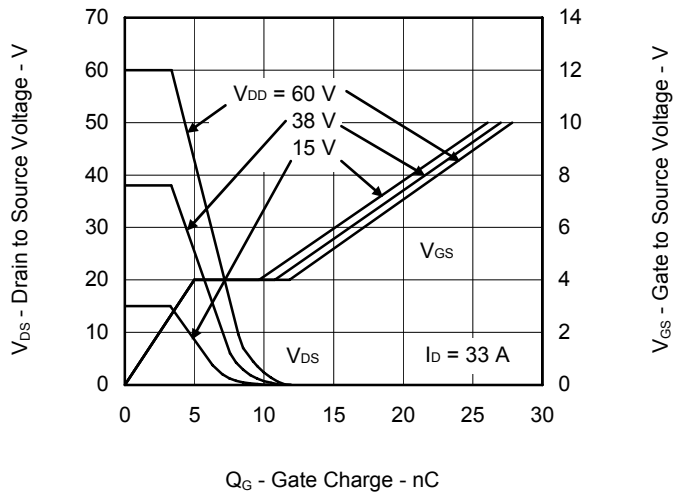
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



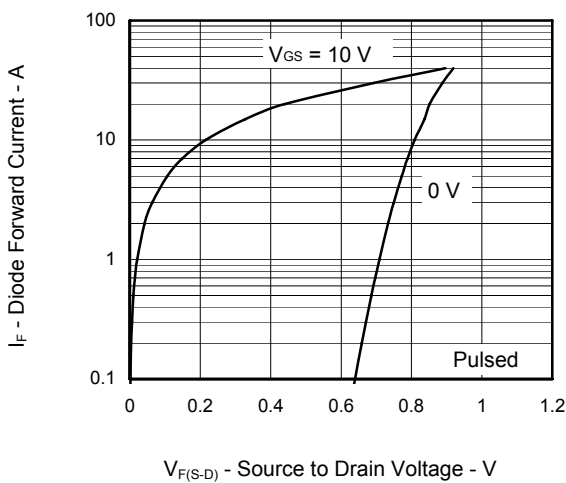
SWITCHING CHARACTERISTICS



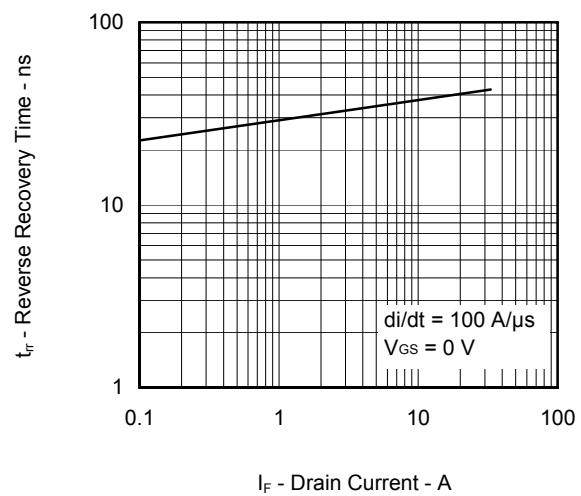
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

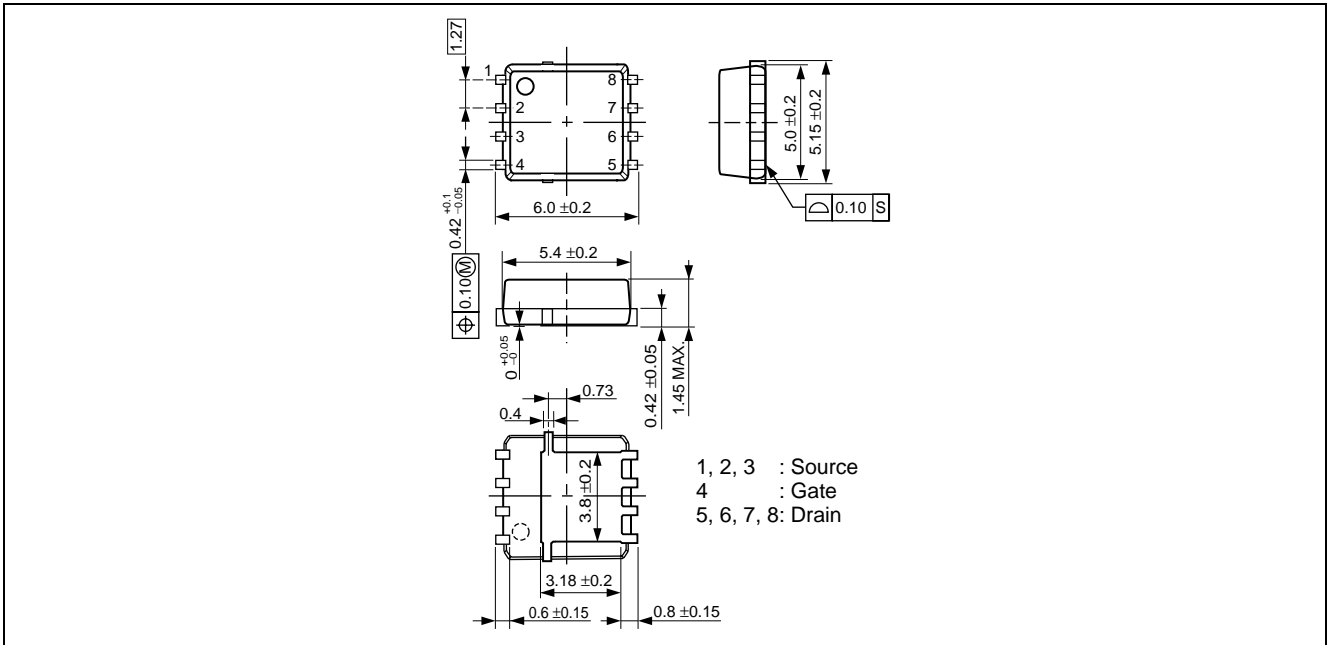


REVERSE RECOVERY TIME vs. DRAIN CURRENT

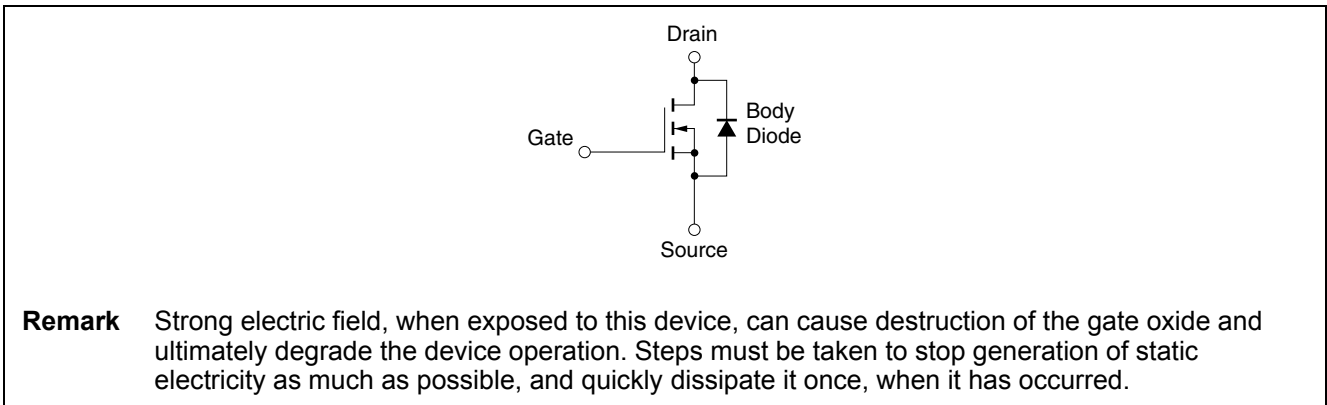


Package Drawings (Unit: mm)

8-pin HSON (Mass: 0.13 g TYP.)



Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History	NP33N075YDF Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	Jun 30, 2011	-	First Edition Issued

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