

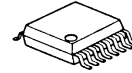
PLL Synthesizer with 3-Wire Bus for TV Tuner

DESCRIPTION

The NJW1503A is a PLL frequency synthesizer especially designed for TV and VCR tuning systems and consists of PLL circuit and a prescaler which operates up to 1.0GHz, built into one chip.

The NJW1503A is controlled through a 3-wire bus.

PACKAGE OUTLINE

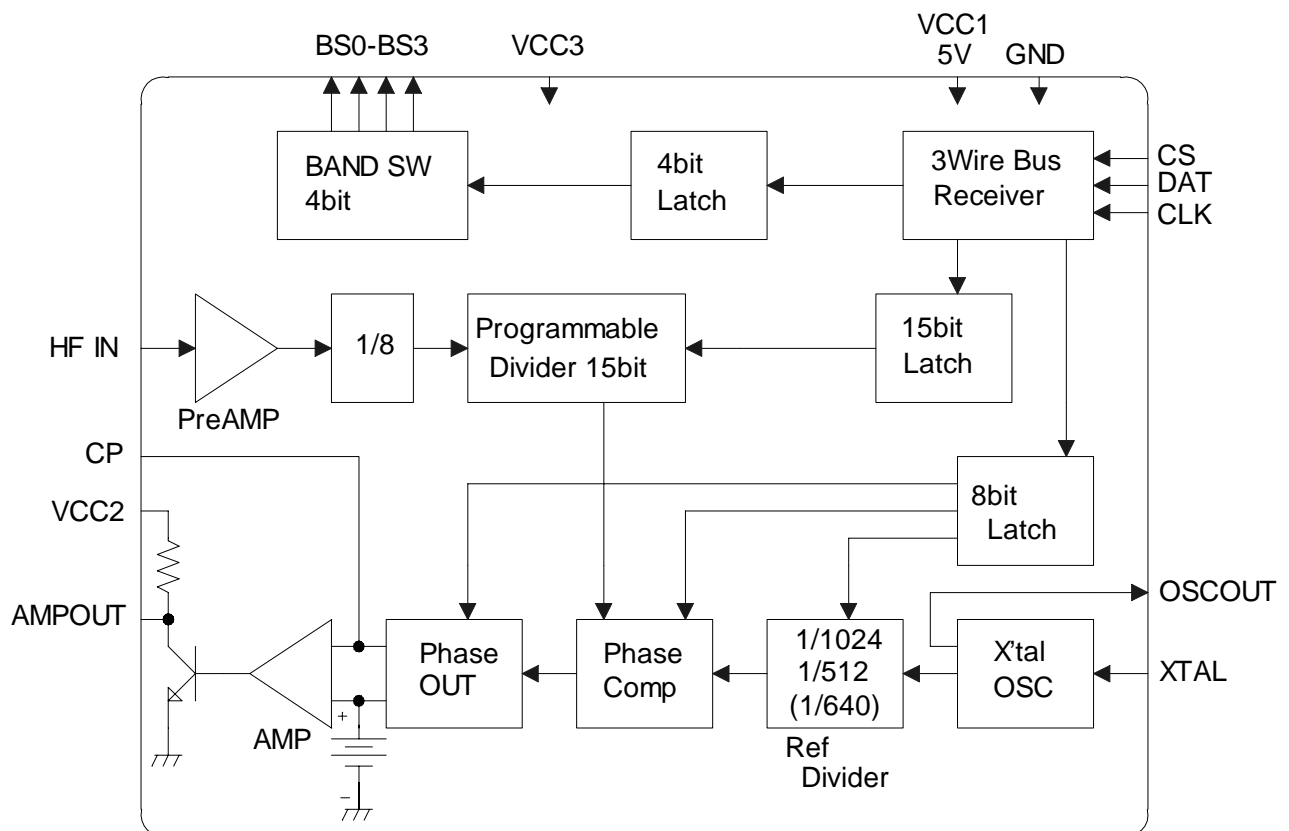


NJW1503AV

FEATURES

- Operating Voltage 5V
- Low Operating Current : 15mA typ. @Vcc=5V
- Prescaler accepts frequencies up to 1GHz on chip
- 3-wire bus controlled
- Reference divider ratio automatic setting (512 or 1024)
- 34V max. tuning voltage output
- Package Outline: SSOP16

BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

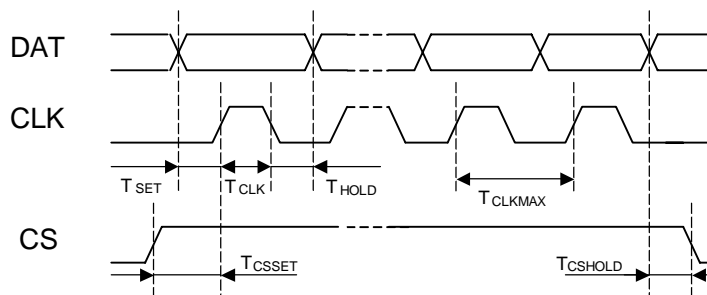
($T_A=25^\circ\text{C}$)

Parameter	Symbol	Ratings	Unit
Supply Voltage (Vcc1,3)	Vcc1,Vcc3	-0.3 to +6.5	V
Supply Voltage (Vcc2)	Vcc2	-0.3 to +34	V
Input Voltage(except 3-wire bus)	V _i	-0.3 to Vcc+0.3	V
Output Voltage (except 3-wire bus)	V _o	-0.3 to Vcc+0.3	V
3-Wire bus Input Voltage	V _{seri}	-0.3 to 6.5	V
Power Dissipation	P _D	300	mW
Operating Temperature Range	T _{opr}	-20 to +75	°C
Storage Temperature Range	T _{stg}	-40 to +125	°C

■ RECOMMENDED OPERATING CONDITION

($T_A=25^\circ\text{C}$)

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Operating Voltage	Vcc1,Vcc3	V ⁺¹ ,V ⁺³	4.5	5	5.5	V
Operating Voltage	Vcc2	V ⁺²	0	32	34	V
X'tal Operating Range		f _{xtal}	3.15	4	4.05	MHz
HF Input Frequency	Input= -20dBm	f _{hf}	80	-	1000	MHz
Data Set-up Time	Refer to 3-Wire bus Timing Chart	t _{SET}	2	-	-	uS
Clock Width Time		t _{CLK}	2	-	-	uS
Data Hold Time		t _{HOLD}	2	-	-	uS
CS Set-up Time		t _{CSSET}	10	-	-	uS
CS Hold Time		t _{CSHLD}	2	-	-	uS
Maximum Clock Frequency		Refer to 3-Wire bus Timing Chart F _{CLKMAX} =1/T _{CLKMAX}	t _{CLKMAX}	-	-	100



3-Wire bus Timing Chart

V_{IHmin}(0.7 Vcc1) and V_{IHmax}(0.3 Vcc1)

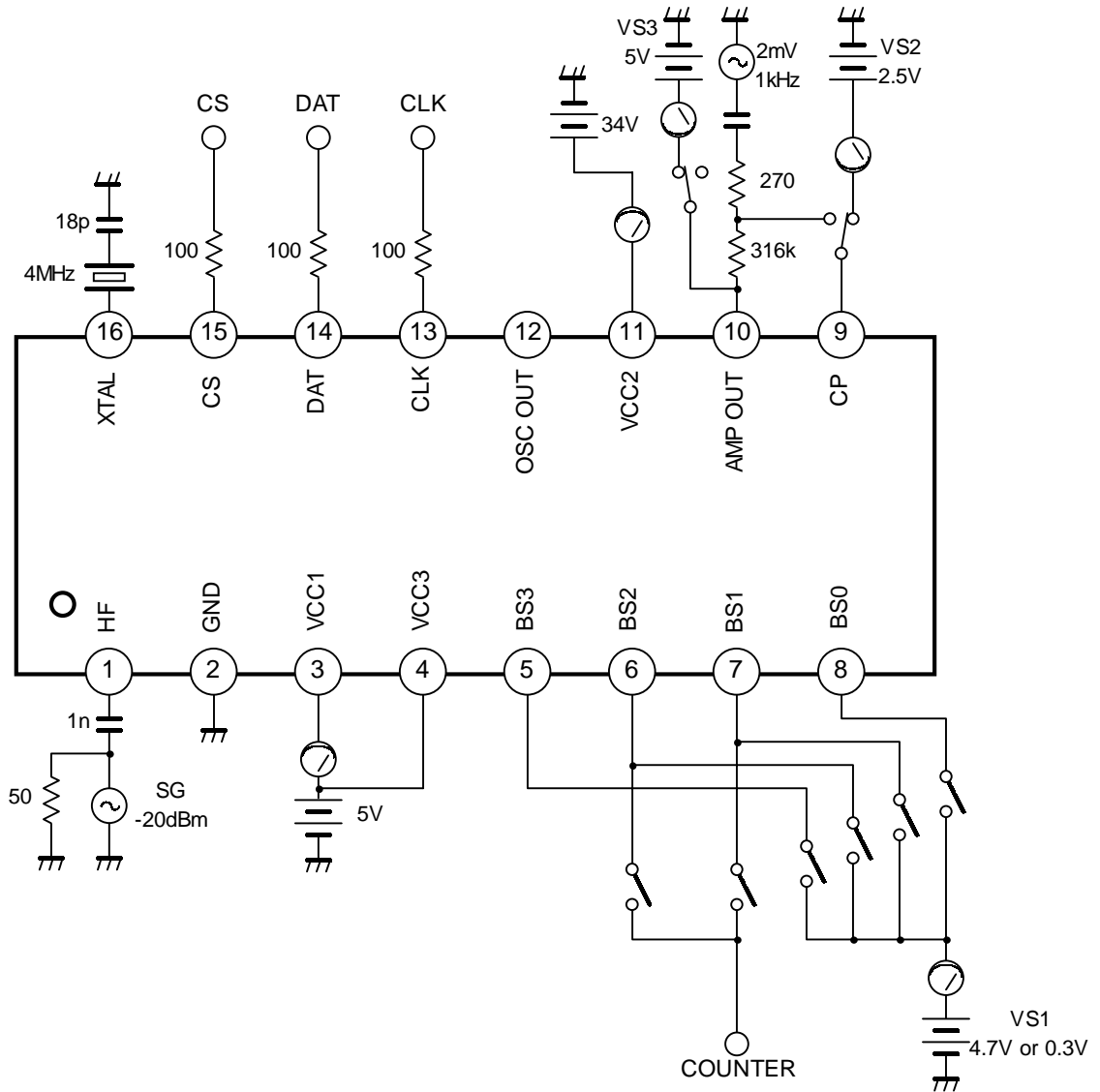
■ ELECTRICAL CHARACTERISTICS

(V_{cc1,3}=5V, V_{cc2}=32V, T_A=25°C)

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Operating Current 1	f _{HF} =100MHz	I _{CC}	6	15	23	mA
Operating Current 2	AMP OUT: Low Level	I _{CC2}	-	1.6	-	mA
AMP Input Current	Phase OUT :High Imp (2.5V)	I _{IN}	(-50)	0.1	(50)	nA
AMP Output Current	AMP OUT : Low Level AMP OUT Input=5V	I _{OUT}	-	-	-2.5	mA
AMP Gain	f=1KHz	AV	40	50	60	dB
Phase Comparator Current	Current Source	I _{source}	190	280	400	uA
Phase Comparator Current	Current Sink	I _{sink}	-400	-280	-190	uA
Band Switch						
"L" Output Current	BS0=BS1=BS2=0.3V	I _{OBS0-2L}	-5.0	-0.5	0.0	mA
"H" Output Current	BS0=BS1=BS2=4.7V	I _{OBS0-2H}	11.0	15.0	-	mA
"L" Output Current	BS=0.3V	I _{OBS3L}	-6.0	-1.0	-0.4	mA
"H" Output Current	BS3=4.7V	I _{OBS3H}	0.7	3.5	-	mA
3-Wire bus						
"H" Input Current	CLK, DAT, CS Terminal	I _{INH}	-5	0	5	uA
"L" Input Current	CLK, DAT, CS Terminal	I _{INL}	-5	0	5	uA
"H" Input Voltage Range	CLK, DAT, CS Terminal	V _{IH}	4.0	-	5.0	V
"L" Input Voltage Range	CLK, DAT, CS Terminal	V _{IL}	0	-	1.0	V

NJW1503A

■ TEST CIRCUIT



■ Serial Bus Data Format (3-Wire bus)

1. Bus protocol for 18bit

B3 B2 B1 B0 N13 N12 N11 N10 N9 N8 N7 N6 N5 N4 N3 N2 N1 N0

Reference divider : $f_{xtal} / 512$

2. Bus protocol for 19bit

B3 B2 B1 B0 N14 N13 N12 N11 N10 N9 N8 N7 N6 N5 N4 N3 N2 N1 N0

Reference divider : $f_{xtal} / 1024$

3. Bus protocol for Test (27bit)

B3 B2 B1 B0 N14 N13 ...N1 N0 T7 T6 T5 T4 T3 T2 T1 T0

B0 to B3 : Control of Band Switch

N0 to N14 : Control of Programmable Divider N14=MSB N0=LSB

Division ratio : $N = 2^{14} \times N14 + 2^{13} \times N13 + \dots + 2^1 \times N1 + N0$

Maximum division ratio 32767

Minimum division ratio 256

T0 to T7 : Control bit of test

Bit T0: Charge Pump Current

T0	Charge Pump Current	Conditions
0	280uA	Normal, Default
1	60uA	Test

Bit T1 and T2: Output function of Phase Comparator

T2	T1	Phase Comparator	Conditions
0	0	Normal Operation	Normal, Default
0	1	Source	Test
1	1	High Impedance	Test
1	0	Sink	Test

Bit T4: Band Switch Test

T4	Band Switch	Conditions
0	Normal Operation	Normal, Default
1	Test	Test

Bit T5 and T6: Reference Divider

T6	T5	Reference Divider	Condition
0	0	1/512	Normal, Default
0	1	1/1024	
1	*	1/640	

* : don't care; 0 or 1

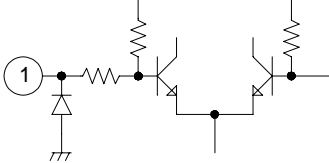
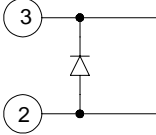
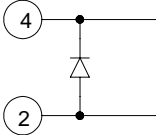
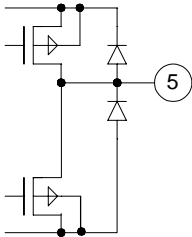
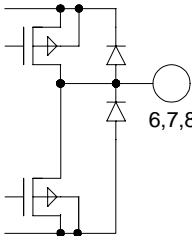
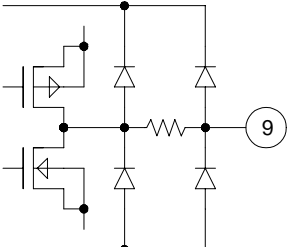
The 18bit and 19bit is automatic selector of the reference divider.

T3: unassigned, undefined

(Note)

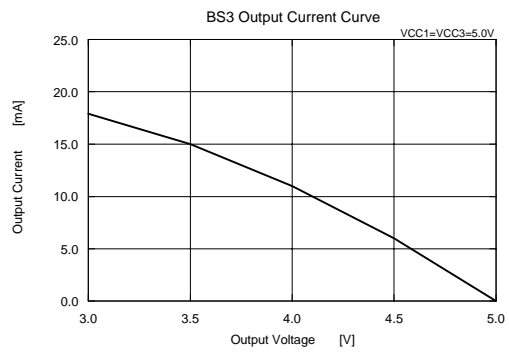
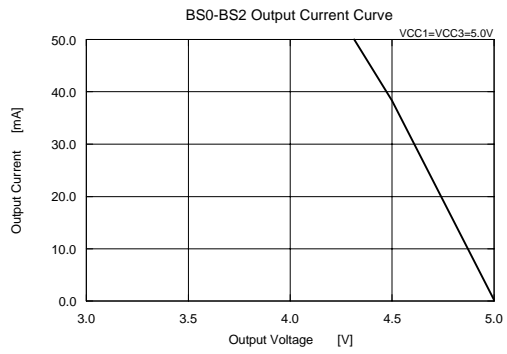
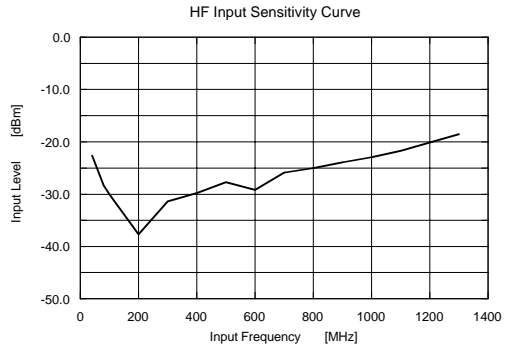
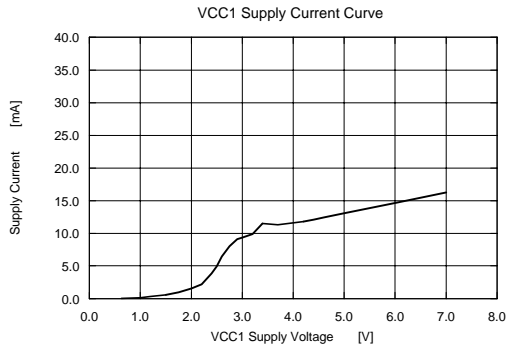
Default : Power on reset

■ TERMINAL CHARACTERISTICS

No.	Symbol	Typ.DC Voltage (V)	Equivalent Circuit	Function
1	HF	3.2		High Frequency Signal Input
2	GND	0		GND
3	VCC1	5		Power Supply
4	VCC3	5		Band Switch Power Supply
5	BS3	0		Band Switch
6 7 8	BS2 BS1 BS0	0		Band Switch
9	CP	-		Charge Pump Output

No.	Symbol	Typ.DC Voltage (V)	Equivalent Circuit	Function
10	AMPOUT	-		Amplifier Output
11	VCC2	32		Amplifier Power Supply
12	OSCOUT	4.1		Reference Oscillator Output
13	CLK	-		Clock Input (3-Wire bus)
14	DAT	-		Data Input (3-Wire bus)
15	CS	-		Enable Input (3-Wire bus)
16	XTAL	3.3		Crystal Input

■ TYPICAL CHARACTERISTICS



MEMO

[CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.