NXP Semiconductors
User's Guide

Document Number: TWRKL82Z72MUG
Rev. 1, 07/2016

TWR-KL82Z72M User's Guide

1. Introduction

The NXP TWR-KL82Z72M Tower System modular development platform module is a low-cost evaluation, demonstration, and development board, which features a 96 MHz Kinetis KL82 low-power MCU.
The TWR-KL82Z72M MCU module can operate either stand-alone or as a part of the NXP Tower System, a modular development platform that enables rapid prototyping and tool re-use through reconfigurable hardware. Take your design to the next level and start building your Tower System today by visiting nxp.com/tower for additional Tower System MCU modules and compatible peripherals.

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1.1. Features

This list summarizes the features of the KL82Z72M Tower System MCU modules:

- Kinetis L Series KL82 family MCU MKL82Z128VMC7 in an 121MAPBGA package
- Tower System compatible processor board
- On-board debug circuit K20DX128VFM5 OpenSDA with a virtual serial port
- 2 × 128 Mbit (16 MB) dual on-board QuadSPI memory
- 5 × user-controlled status LED
- 2 × capacitive touchpad
- 2 × mechanical push-button
- Stand-alone full-speed USB host and device functionality
- Potentiometer
- EMVSIM card interface
- 10 × axis sensor system
- FXOS8700CQ 3D accelerometer + 3D magnetometer
- MPL3115A2 digital pressure sensor
- FXAS21002C 3-axis gyroscope
- Socket for touch keypad plug-in (TWRPI-TOUCH-STR)
- Power selector with 3.3 V and 1.8 V MCU operation modes
- Independent, battery-operated power supply for the Real-Time Clock (RTC) module
- Battery holder for a 20 mm lithium battery (e.g., 2032)

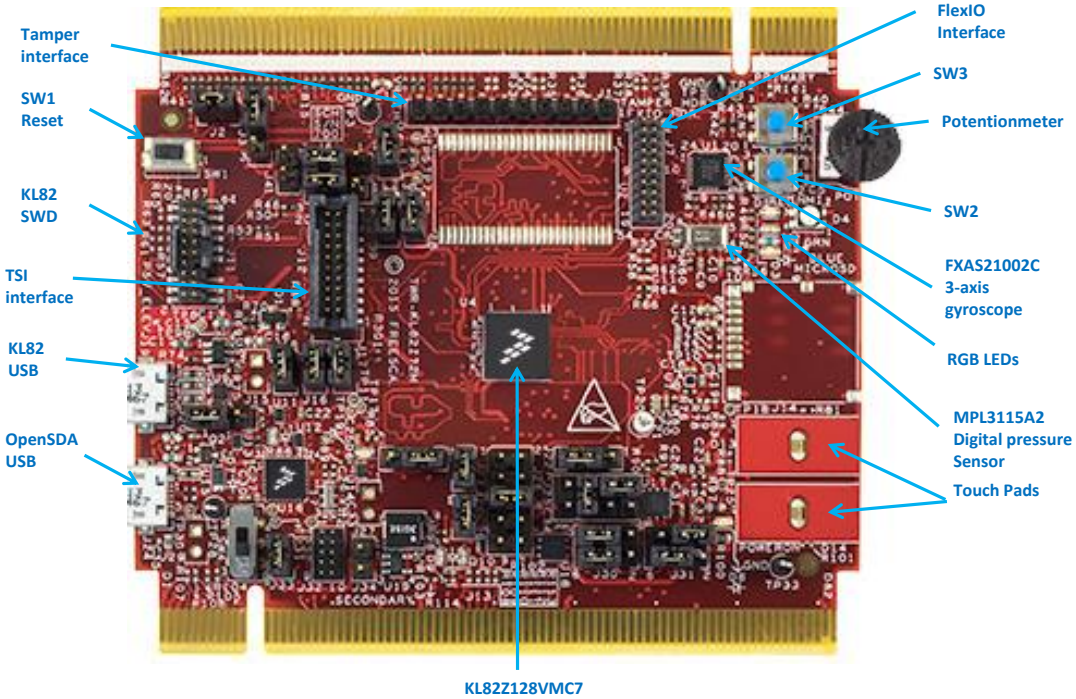

Figure 1. Front side of TWR-KL82Z72M module

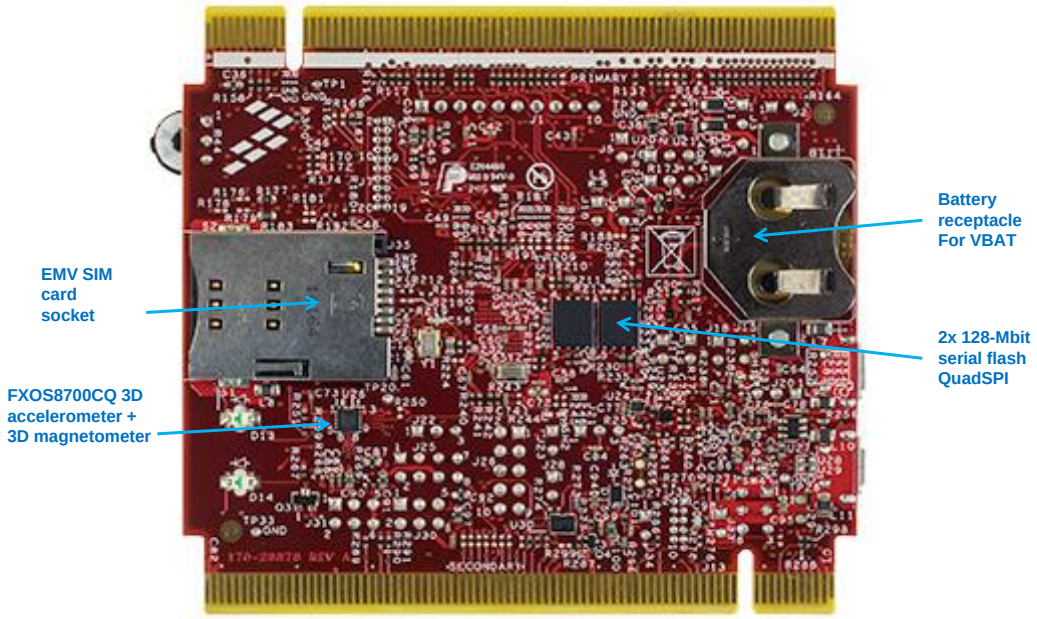

Figure 2. Back side of TWR-KL82Z72M module

1.2. Getting started

In the TWR-KL82Z72M box, there is a printed version of the Quick Start Guide that contains the list of recommended steps for getting started.

2. Contents

The TWR-KL82Z72M package includes:

- TWR-KL82Z72M module for board assembly
- Quick Start Guide
- USB A to micro-B cable for debug interface and power supply
- CR2032 coin-cell battery for VBAT power supply
- USB A to micro-B cable for MKL82Z128VMC7 USB interface

3. Hardware description

The TWR-KL82Z72M Tower System MCU module features the MKL82Z128VMC7—an ARM® Cortex®-M0+ based MCU with 128 KB on-chip flash, 96 KB on-chip SRAM, and USB controllers in a 121-pin MAPBGA package. The MCU has a maximum core frequency of 96 MHz.
The TWR-KL82Z72M module is intended for use in the NXP Tower System, but it can also operate as a stand-alone module. OpenSDA (an on-board debugging circuit) provides the SWD debug interface and power supply input through a single USB micro-AB connector. The following sections describe the hardware in more detail.

This figure shows a block diagram of the TWR-KL82Z72M.

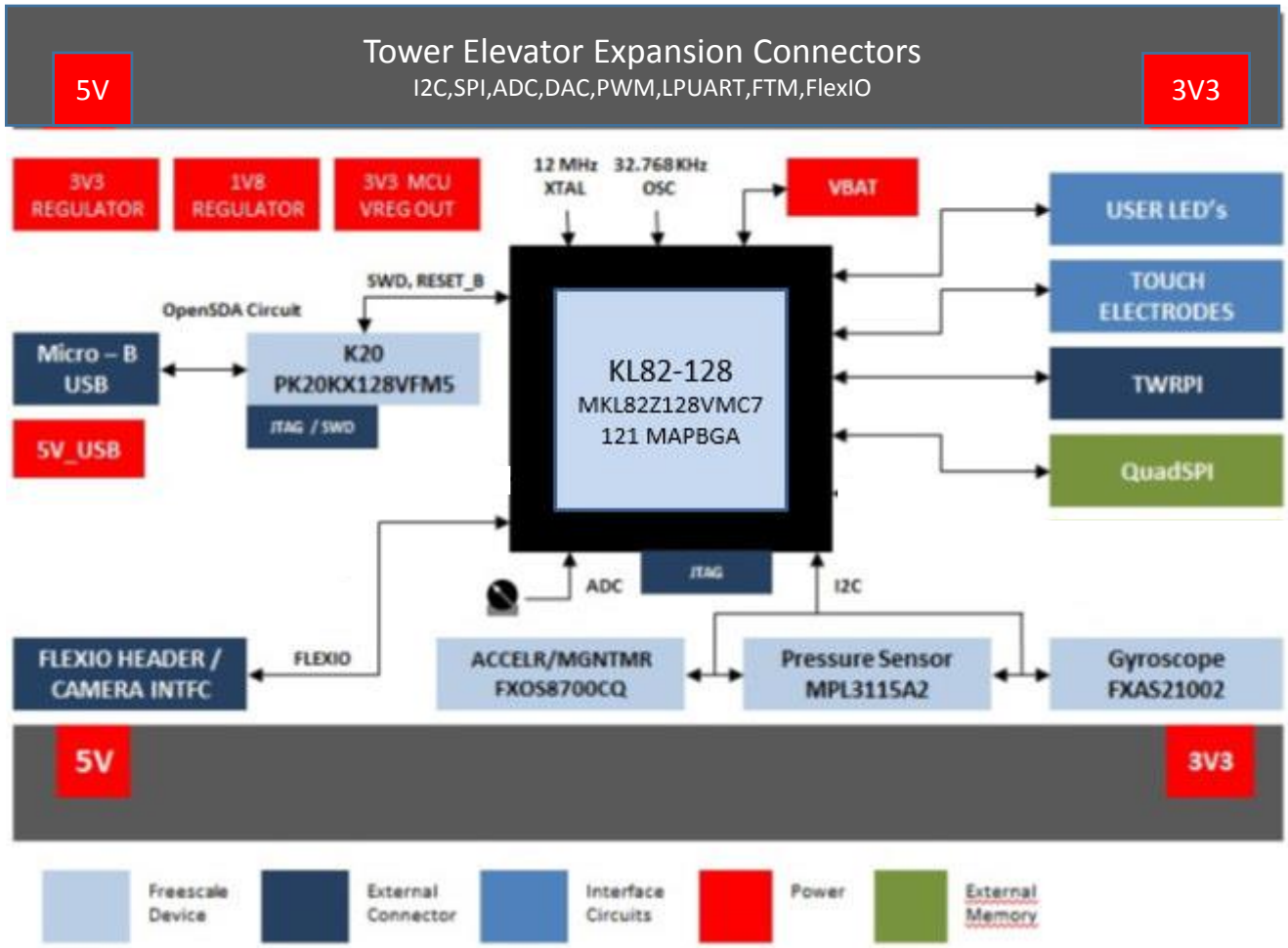

Figure 3. TWR-KL82Z72M block diagram

3.1. KL82Z72M MCU

The TWR-KL82Z72M module features the MKL82Z128VMC7 MCU. The KL82 MCU family is part of the Kinetis portfolio of devices built around the ARM Cortex-M0+ core. See the KL82 family reference manual for detailed information about the MKL82Z128VMC7 MCU. The key features of the MKL82Z128VMC7 MCU are:

Table 1. MKL82Z128VMC7 key features

Feature	Description
Performance	• Up to 96 MHz ARM Cortex-M0+ core
Memory and memory expansion	• 128 KB program flash memory • 96 KB SRAM • 32 KB ROM with built-in bootloader • 32 B backup register • QSPI to expand the program code in the external high-speed serial NOR flash memory

Table 1. MKL82Z128VMC7 key features

Feature	Description
Analog modules	• One 16-bit SAR ADC and One 12-bit DAC • One analog comparator (CMP) containing a 6-bit DAC and a programmable reference input • 1.2 V reference voltage
Communication interfaces	• USB full-speed 2.0 OTG controller supporting crystal-less recovery • Two 16-bit SPI modules • Three low-power UART modules supporting asynchronous operation in low-power modes • Two EMVSIM modules supporting EMV L1-compatible interfaces • Two I^2C modules supporting speed of up to 1 Mbit/s • One FlexIO module
Security	• Unique 128-bit identification number per chip • Advanced flash security and access control • Hardware CRC module • Low-power, trusted crypto engine supporting AES128/256, DES, 3DES, SHA256, RSA, and ECC, with hardware DPA • True random number generator
Timers	• 4-channel periodic interrupt timer • Two low-power timers • One 6-channel general-purpose/PWM timer • Two 2-channel general-purpose timers • Independent real-time clock
Human machine interface	• Low-power hardware Touch Sensor Interface (TSI) • General-purpose input/output

3.2. Clocking

Kinetis MCUs start up from an internal Digitally-Controlled Oscillator (DCO). The software can enable one or two external oscillators (if required). The external oscillator for the Multi-purpose Clock Generator (MCG) module ranges from 32.768 kHz up to a 32 MHz crystal or ceramic resonator. The external oscillator for the Real-Time Clock (RTC) module accepts a 32.768 kHz crystal.

Two on-board crystals are provided to clock the KL82Z72M device: a 12 MHz crystal as the main oscillator to clock the MCG module, and a 32.768 kHz crystal to clock the RTC module.

3.3. System power

The TWR-KL82Z72M module offers a design with multiple power-supply options. Power the module from the elevator 5 V input, USB OpenSDA, or the 5 V input at the KL82 on-board USB port.

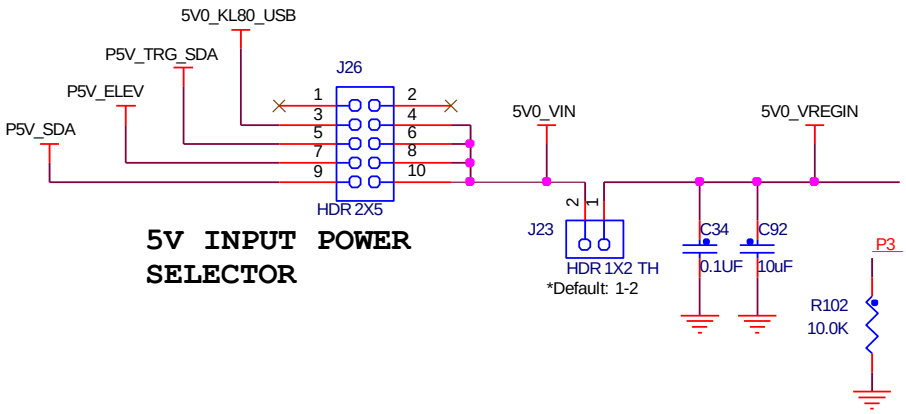

Figure 4. TWR-KL82Z72M power supply

This table provides operational details of the power supplies:

Table 2. TWR-KL82Z72M power supplies

J26 setting	Description
3-4 shunt	Raw 5 V input from the KL82 on-board USB port
5-6 shunt	Regulated 5 V output from the OpenSDA 5 V input (default setting)
7-8 shunt	Power from the P5V_ELEV input
9-10 shunt	Raw 5 V input from the USB OpenSDA

The 5 V input is converted to a 3.3 V output by the on-board regulator; it also regulates the 1.8 V output, and provides the power selection for KL82 (3.3 V or 1.8 V) using J25.

See this table for details:

Table 3. Power selection for KL82

J31 setting	VDD for KL82	VDDIO_E for KL82
1-3 shunt 4-6 shunt	3.3 V	1.8 V
1-3 shunt 2-4 shunt	3.3 V	3.3 V
3-5 shunt 4-6 shunt	1.8 V	1.8 V
3-5 shunt 2-4 shunt	1.8 V	3.3 V

NOTE

The on-board QSPI flash supports only 3.3 V. Check the default jumper setting for J31 (short 1-3 and 2-4).

The 3.3 V and 1.8 V MCU power supplies are routed through the J9 jumper. Remove the jumper shunt to enable the measurement of power consumed by the MCU.

3.4. Real-Time Clock supply

The Real-Time Clock (RTC) module on the MKL82Z128VMC7 MCU has two modes of operation: system power up and system power down. During system power down, the tamper-detection module and the RTC are powered from the backup power supply (VBAT) and electrically isolated from the rest of

the MCU. The TWR-KL82Z72M module provides a battery receptacle for a coin-cell battery that can be used as the VBAT supply. The receptacle uses standard 20 mm diameter 3 V lithium coin-cell batteries.

3.5. Serial and Debug Adapter version 2 (OpenSDAv2)

OpenSDAv2 is a serial and debug adapter circuit which includes open-source hardware design, open-source bootloader, and debug interface software. It bridges the serial and debug communications between a USB host and an embedded target processor (as shown in Figure 5). The hardware circuit is based on a Kinetis K20 family MCU with 128 KB of embedded flash and an integrated USB controller. OpenSDAv2 comes preloaded with the CMSIS-DAP bootloader (an open-source Mass Storage Device (MSD) bootloader) and the CMSIS-DAP interface firmware (also known as the mbed interface), which provides an MSD flash-programming interface, a virtual serial port interface, and a CMSIS-DAP debug protocol interface. For more information about the OpenSDAv2 software, see mbed.org and github.com/mbedmicro/CMSIS-DAP.

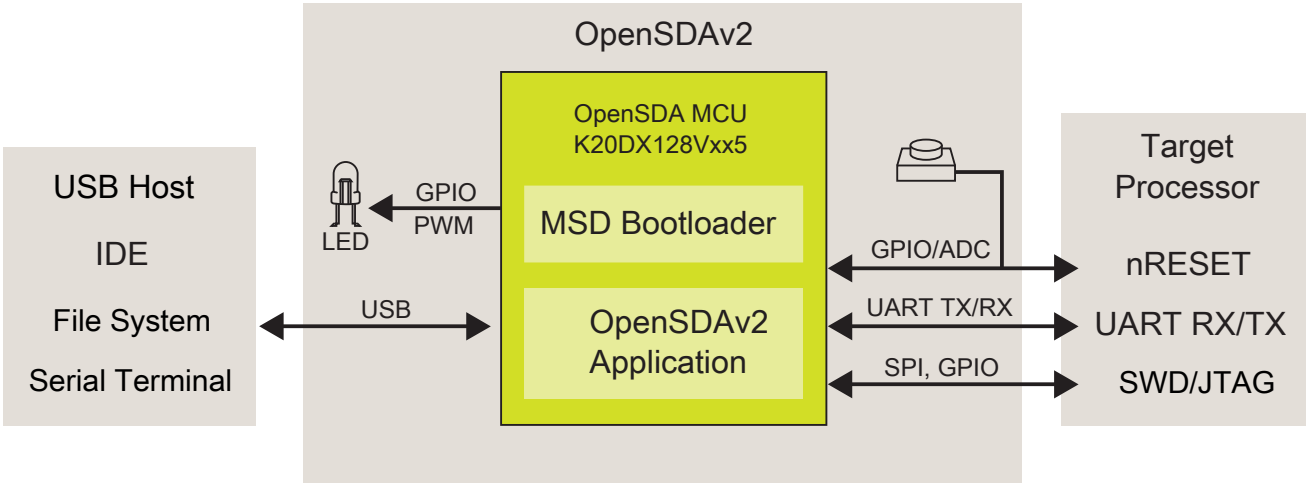

Figure 5. OpenSDAv2 high-level block diagram

OpenSDAv2 is managed by a Kinetis K20 MCU built around the ARM Cortex-M4 core.
The OpenSDAv2 circuit includes a status LED (D5) and a push-button (SW1). The push-button asserts the RESET signal to the KL82 target MCU. Use it to place the OpenSDAv2 circuit into the bootloader mode. The SPI and GPIO signals provide an interface to either the SWD debug port or the K20.
There are signal connections available to implement a UART serial channel. The OpenSDAv2 circuit receives power when the USB connector J24 is plugged into the USB host.

3.6. Cortex Debug connector

The Cortex Debug connector is a 20-pin (0.05 in.) connector providing access to the SWD signals available on the KL82 device. The KL82 pin connections on the Cortex Debug connector (J11) are shown in this table:

Table 4. Cortex Debug connector pinout

Pin	Function	TWR-KL82Z72M connection
1	VTref	3.3 V MCU supply (V_BRD)
2	TMS/SWDIO	TSI0_CH4/PTA3/LPUART0_RTS_B/TPM0_CH0/FXIO0_D13/EMVSIM0_RST/SWD_DIO
3	GND	GND
4	TCK/SWCLK	TSI0_CH1/PTA0/LPUART0_CTS_B/TPM0_CH5/FXIO0_D10/EMVSIM0_CLK/SWD_CLK
5	GND	GND
6	TDO/SWO	NC
7	Key	_
8	TDI	NC
9	GNDDETECT	NC
10	nReset	RESET_b
11	Target Power	5 V supply (via J21)
12	TRACECLK	NC
13	Target Power	5 V supply (via J21)
14	TRACEDATA[0]	NC
15	GND	GND
16	TRACEDATA[1]	NC
17	GND	GND
18	TRACEDATA[2]	NC
19	GND	GND
20	TRACEDATA[3]	NC

3.7. Serial port

The serial-port interface signals used with the OpenSDA are LPUART1 pins PTC4 (TXD) and PTC3 (RXD).

3.8. Reset

The RESET signal on the KL82Z is externally connected to the SW1 push-button. Use the “Reset” button to force an external reset event in the target MCU. Use the “Reset” button also to force the OpenSDA circuit into the bootloader mode when plugging the USB cable to J24. See Section 3.5, “Serial and Debug Adapter version 2 (OpenSDAv2)” for more details.

3.9. Sensors

FXOS87000CQ (accelerometer + magnetometer) is connected to the KL82Z MCU through an I^2C interface (I^2C0) and two GPIO/IRQ signals (PTA17 and PTA29). See Table 5 for connection details.

If you use Kinetis Bootloader to update the KL82 MCU flash firmware through an I^2C interface, see the information about Kinetis Bootloader (nxp.com/kboot).

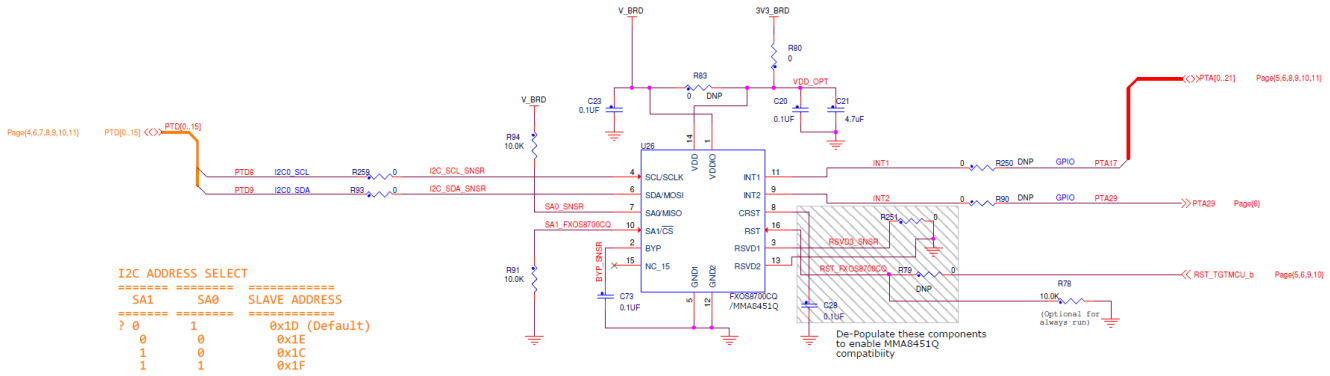

Figure 6. Accelerometer connection

The 3-axis gyroscope (FXAS21002C) is connected to the I²C interface (I2C0) and two GPIO/IRQ signals (PTA17 and PTA29).

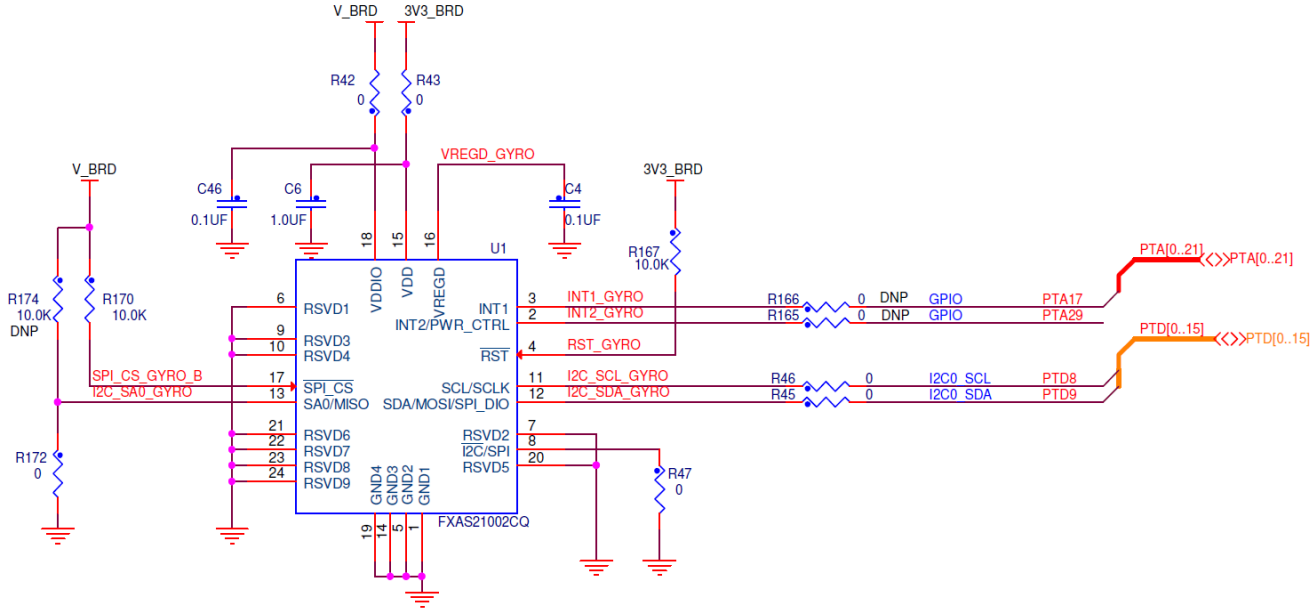

Figure 7. Gyroscope sensor connection

The Digital Pressure Sensor (MPL3115A2) is also connected to the I²C interface (I2C0) and two GPIO/IRQ signals (PTA17 and PTA29).

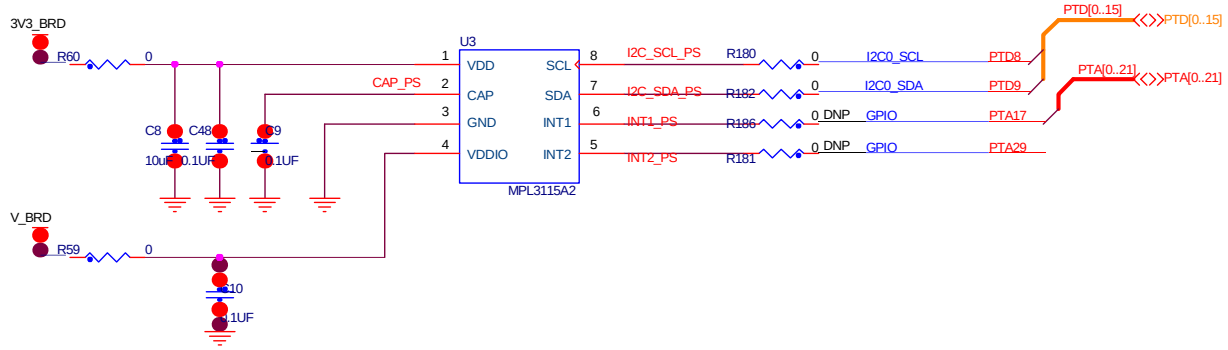

Figure 8. Pressure sensor connection

3.10. Potentiometer, push-buttons, and LEDs

The TWR-KL82Z72M features:

- A potentiometer connected to the ADC input signal (ADC1_SE7b/PTD6)
- Two push-button switches (SW2 and SW3 connected to PTA4 and PTD2)
- User-controllable LEDs connected to the GPIO signals:
  - Red LED D1 is connected to PTD11
  - Green LED D2 is connected to PTD12
  - Blue LED D3 is connected to PTD13
  - LED D13 is connected to PTD14
  - LED D14 is connected to PTD15

3.11. General-purpose Tower System plug-in (TWRPI) socket

The TWR-KL82Z72M module features a socket compatible with the TSI Tower System plug-in modules (J12). See this table for detailed connection information:

Table 5. TWRPI socket pin description

2x10 connector			
Pin	**Description**	**Pin**	**Description**
1	5 V VCC	2	V_BRD (3.3 V or 1.8 V)
3	PTA4 (TSI0_CH5/)	4	VDDA (3.3 V or 1.8 V)
5	PTB0 (TSI0_CH0)	6	GND
7	PTB1 (TSI0_CH6)	8	PTB2 (TSI0_CH7)
9	PTB3 (TSI0_CH8)	10	PTB16 (TSI0_CH9)
11	PTB17 (TSI0_CH10)	12	PTB18 (TSI0_CH11)
13	PTB19 (TSI0_CH12)	14	PTC0 (TSI0_CH13)
15	PTC1 (TSI0_CH14)	16	PTC2 (TSI0_CH15)
17	ADC0_DP0	18	ADC0_DM0
19	GND	20	Reset_b

The TWR-KL82Z72M module also features a header for the FlexIO interface (J7), which can flexibly simulate different interfaces, such as UART, I^2C, SPI, Camera, LCD, and other.

Table 6. FlexIO pin description

2x10 connector			
Pin	**Description**	**Pin**	**Description**
1	PTB0 (FlexIO_D0)	2	PTB1 (FlexIO_D1)
3	PTB2 (FlexIO_D2)	4	PTB3 (FlexIO_D3)
5	PTB10 (FlexIO_D4)	6	PTB11 (FlexIO_D5)
7	PTB18 (FlexIO_D6)	8	PTB19 (FlexIO_D7)
9	PTB20 (FlexIO_D8)	10	PTB21 (FlexIO_D9)

11	PTA0 (FlexIO_D10)	12	PTA1 (FlexIO_D11)
13	PTA2 (FlexIO_D12)	14	PTC1 (FlexIO_D13)
15	PTC6 (FlexIO_D14)	16	PTC7 (FlexIO_D15)
17	PTA10 (FlexIO_D16)	18	PTA11 (FlexIO_D17)
19	PTA12 (FlexIO_D18)	20	PTA13 (FlexIO_D19)

3.12. Touch interface

The Touch-Sensing Input (TSI) module on Kinetis MCUs provides capacitive touch-sensing detection with high sensitivity and enhanced robustness. Each TSI pin implements capacitive measurement of an electrode. There are two individual electrodes on the TWR-KL82Z72M module that simulate push-buttons.

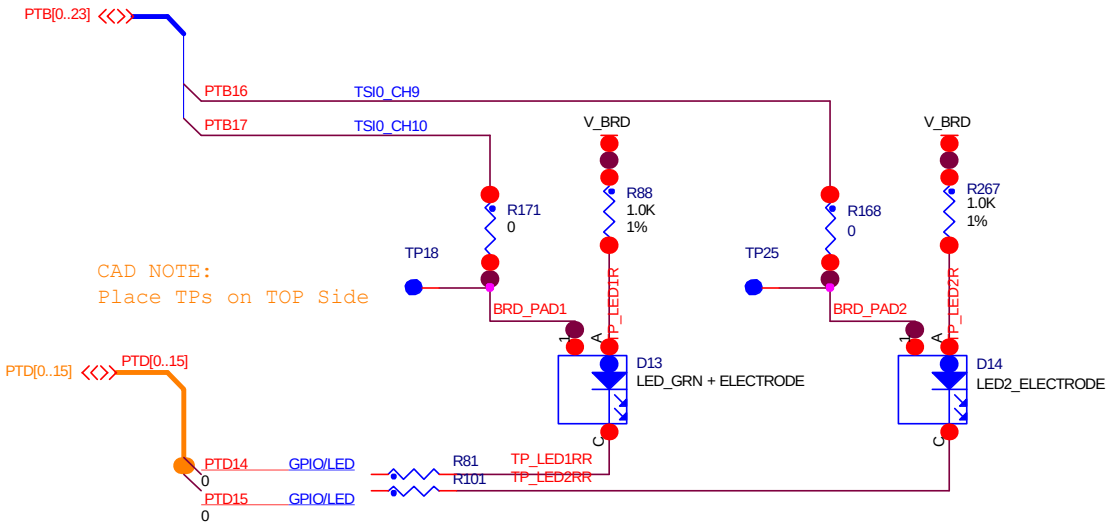

Figure 9. Touch pad circuitry

3.13. USB interface

The MKL82Z128VMC7 MCU features full- and low-speed USB controllers with on-chip USB PHY. The TWR-KL82Z72M module enables the USB to act as a host or device. Jumper J20 is used to select whether the USB signals are connected to the on-board micro-B connector J19 (default), or sent down the elevator to be used in connection with the TWR-SER1 board or other peripheral board in a complete Tower System kit.

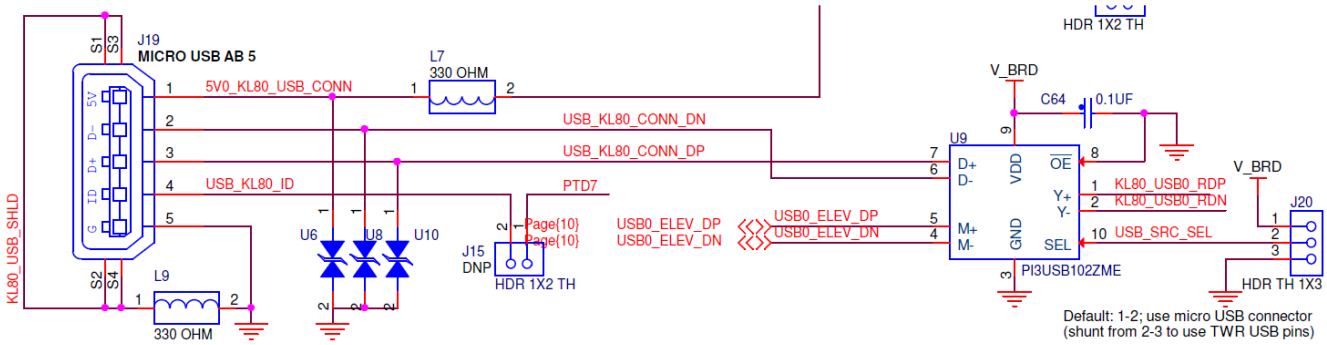

Figure 10. USB signal switching

4. Jumper table

There are several jumpers provided for isolation, configuration, and feature selection. See this table for details (default settings are highlighted in gray):

Table 7. Jumper table

Jumper	Option	Setting	Description
J2	MCU reset connection on the JTAG connector	ON	Connects the MCU reset to pin10 of JTAG connector J11.
		OFF	Disconnects the MCU reset from pin10 of JTAG connector J11.
J3	VBAT power selection	1-2	Connects VBAT to the on-board MCU supply from MCU_PWR.
		2-3	Connects VBAT to the higher voltage between the on-board MCU_PWR supply or coin-cell supply.
J4	JTAG power connection	ON	Connects the on-board 5 V supply to the JTAG port (supports powering the board from an external JTAG probe).
		OFF	Disconnects the on-board 5 V supply from the JTAG port.
J5	QuadSPI power enable	ON	Connects the VDDIO_E domain to power the QuadSPI flash.
		OFF	Disconnect the VDDIO_E domain from the QuadSPI flash.
J6	UART receiver connection	1-2	Connects UART1_RX to the elevator.
		2-3	Connects UART1_RX to the OpenSDA UART receiver.
J8	UART transmitter connection	1-2	Connects UART1_TX to the elevator.
		2-3	Connects UART1_TX to the OpenSDA UART transmitter.
J9	MCU power connection	ON	Connects V_BRD and MCU_PWR to MCU_VDD.
		OFF	Disconnects V_BRD and MCU_PWR from MCU_VDD.
J10	VDD and VDDA connection	ON	Connects VDD to VDDA.
		OFF	Disconnects VDD from VDDA.
J15	USB ID connection	ON	Connects PTD7 to the USB ID pin on micro-USB connector J19.
		OFF	Disconnect PTD7 from the USB ID pin on micro-USB connector J19.
J16	SWD DIO OpenSDA connection	ON	Connects SWD_DIO from the OpenSDA circuit to the KL82 MCU to enable OpenSDA debugging.
		OFF	Disconnects SWD_CLK from the OpenSDA circuit to the KL82 MCU to enable J-Link or U-Link debugging.
J17	SWD clock OpenSDA connection	ON	Connects SWD_CLK from the OpenSDA circuit to the KL82 MCU to enable OpenSDA debugging.
		OFF	Disconnects SWD_CLK from the OpenSDA circuit to the KL82 MCU to enable J-Link or U-Link debugging.
J18	USB overcurrent flag connection	ON	Connects PTC18 to USB over-current flag for MIC2005.
		OFF	Disconnects PTC18 from USB over-current flag for MIC2005.
J20	USB switch selection	1-2	Uses the on-board micro-USB connector J19.
		2-3	USB signals come from the elevator.
J21	“Reset” button connection	1-2	When powering the OpenSDA MCU, bootloader mode can be selected.
		2-3	When the OpenSDA MCU is not powered, “Reset” button can be used.

Table 7. Jumper table

Jumper	Option	Setting	Description
J22	USB_VDD selection	2-3	USB_VDD comes from 3V3_BRD.
		1-2	USB_VDD comes from MCU_VDD.
J23	5 V connection	ON	Connects 5 V IN to the 3.3 V regulator.
		OFF	Disconnects 5 V IN from the 3.3 V regulator.
J25	Board power and regulator selection	1-3	3V3_BRD is connected to the output of the 3.3 V regulator.
		2-4	Invalid configuration. Do not use.
		3-4	Invalid configuration. Do not use.
		4-6	1.8 V regulator uses the output of the Li-Ion battery domain.
		5-6	1.8 V regulator uses the output of the 3.3 V regulator.
		6-8	1.8 V regulator uses the 5 V IN directory.
J26	5 V input power selection	3-4	Raw 5 V input from the KL82 USB.
		5-6	Regulated 5 V output from the OpenSDA 5 V input.
		7-8	Power from the P5V_ELEV input.
		9-10	Raw 5 V input from the OpenSDA USB port J24.
J27	OpenSDA reset	ON	Connects the OpenSDA reset signal to the board reset. There is a board trace that ensures this connection even if the jumper is not populated.
		OFF	Disconnects the OpenSDA reset signal from the board reset. By default, there is a board trace connecting this signal even if the jumper is not populated.
J28	USB power enable connection	ON	Connects PTC19 to the USB power enable for MIC2005.
		OFF	Disconnects PTC19 from the USB power enable for MIC2005.
J30	3.3 V and 1.8 V sequencing	1-2	Invalid configuration. Do not use.
		1-3	Option 2: 1.8 V comes up before 3.3 V. The 3.3 V regulator is enabled by the output of the 1.8 V regulator. Only used if VDD=1.8 V and VDDIO_E=3.3 V.
		2-4	Option 2: 1.8 V comes up before 3.3 V. The 1.8 V regulator is enabled by the input to the regulator. Only used if VDD=1.8 V and VDDIO_E=3.3 V.
		3-5	Option 1: 3.3 V comes up before 1.8 V. The 3.3 V regulator is enabled by the input to the regulator.
		4-6	Option 1: 3.3 V comes up before 1.8 V. The 1.8 V regulator enabled by the 3.3 V board supply.
		5-6	Invalid configuration. Do not use.
J31	VDDIO_E and VDD selection	1-3	V_BRD/MCU_VDD is 3.3 V.
		2-4	VDDIO_E is 3.3 V.
		3-5	V_BRD/MCU_VDD is 1.8 V.
		4-6	VDDIO_E is 1.8 V.
J33	Battery voltage monitoring	ON	Connects ADC0_SE6B to the battery voltage.
		OFF	Enables the 5 V boost.
J34	Battery boost regulator input	ON	Enables the 5 V boost.
		OFF	Disconnects boost enable.

5. References

The list below provides references for more information about the Kinetis family, Tower System, and the MCU modules. Find these resources in the documentation section at nxp.com/TWR-KL82Z72M or nxp.com/kinetis.

- *TWR-KL82Z72M Quick Start Guide* (document TWR-KL82Z72M-QSG)
- *TWR-KL82Z72M Schematics* (document TWR-KL82Z72M-SCH)
- KL82 family data sheet
- KL82 family reference manual
- *Kinetis Quick Reference User's Guide* (document KQRUG)

6. Revision history

This table summarizes the changes made to this document since the initial release:

Table 8. Revision history

Revision Number	Date	Substantive changes
0	01/2016	Initial release
1	07/2016	Updated links in references

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Rev. 1
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