NLSV1T34

1-Bit Dual-Supply Non-Inverting Level Translator

The NLSV1T34 is a 1−bit configurable dual−supply voltage level translator. The input A_n and output B_n ports are designed to track two different power supply rails, V_{CCA} and V_{CCB} respectively. Both supply rails are configurable from 0.9 V to 4.5 V allowing universal low−voltage translation from the input A_n to the output B_n port.

Features

- Wide V_{CCA} and V_{CCB} Operating Range: 0.9 V to 4.5 V
- High−Speed w/ Balanced Propagation Delay
- Inputs and Outputs have OVT Protection to 4.5 V
- Non−preferential V_{CCA} and V_{CCB} Sequencing
- Power−Off Protection
- Power−Off High Impedance Inputs and Outputs
- Ultra−Small Packaging: 1.45 mm x 1.0 mm ULLGA6
  2.0 mm x 2.1 mm SC−88A
  1.2 mm x 1.0 mm UDFN6
  1.45 mm x 1.0 mm UDFN6
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

Typical Applications

- Mobile Phones, PDAs, Other Portable Devices

Important Information

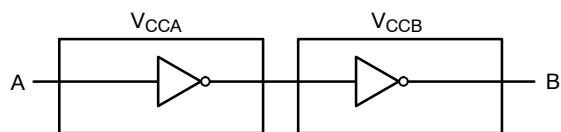- ESD Protection for All Pins:
  HBM (Human Body Model) > 3000 V

Figure 1. Logic Diagram
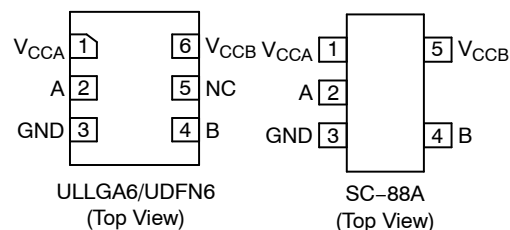
ON Semiconductor®

MARKING DIAGRAMS

UDFN6
MU SUFFIX
CASE 517AA

UDFN6
MU SUFFIX
CASE 517AQ

ULLGA6
MX1 SUFFIX
CASE 613AF

SC−88A
(SOT−353/SC−70)
DF SUFFIX
CASE 419A

Q, A	= Device Code
M	= Date Code*
▪	= Pb−Free Package

(Note: Microdot may be in either location)
*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN ASSIGNMENT

V_{CCA}	1	6	V_{CCB}
A	2	5	NC
GND	3	4	B

ULLGA6/UDFN6
(Top View)

V_{CCA}	1	5	V_{CCB}
A	2		
GND	3	4	B

SC−88A
(Top View)

ORDERING INFORMATION

May, 2012 – Rev. 9

Publication Order Number:
NLSV1T34/D

PIN ASSIGNMENT

PIN	FUNCTION
V_{CCA}	Input Port DC Power Supply
V_{CCB}	Output Port DC Power Supply
GND	Ground
A	Input Port
B	Output Port

TRUTH TABLE

INPUTS	OUTPUTS
A	B
L	L
H	H

MAXIMUM RATINGS

Symbol	Rating		Value	Condition	Unit
V_{CCA}, V_{CCB}	DC Supply Voltage		−0.5 to +5.5		V
V_I	DC Input Voltage	A	−0.5 to +5.5		V
V_O	DC Output Voltage (Power Down)	B	−0.5 to +5.5	V_{CCA} = V_{CCB} = 0	V
	(Active Mode)	B	−0.5 to +5.5		V
I_{IK}	DC Input Diode Current		−20	V_I < GND	mA
I_{OK}	DC Output Diode Current		−50	V_O < GND	mA
I_O	DC Output Source/Sink Current		±50		mA
I_{CCA}, I_{CCB}	DC Supply Current Per Supply Pin		±100		mA
I_{GND}	DC Ground Current per Ground Pin		±100		mA
T_{STG}	Storage Temperature		−65 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CCA}, V_{CCB}	Positive DC Supply Voltage		0.9	4.5	V
V_I	Bus Input Voltage		GND	4.5	V
V_{IO}	Bus Output Voltage (Power Down Mode)	B	GND	4.5	V
	(Active Mode)	B	GND	V_{CCB}	V
T_A	Operating Temperature Range		−40	+85	°C
$\Delta t / \Delta V$	Input Transition Rise or Rate V_I, from 30% to 70% of V_{CC}; V_{CC} = 3.3 V ±0.3 V		0	10	nS

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CCA} (V)	V_{CCB} (V)	−40°C to +85°C		Unit
					Min	Max	
V_{IH}	Input HIGH Voltage		3.6 − 4.5	0.9 − 4.5	2.2	−	V
			2.7 − 3.6		2.0	−	
			2.3 − 2.7		1.6	−	
			1.4 − 2.3		$0.65 * V_{CCA}$	−	
			0.9 − 1.4		$0.9 * V_{CCA}$	−	
V_{IL}	Input LOW Voltage		3.6 − 4.5	0.9 − 4.5	−	0.8	V
			2.7 − 3.6		−	0.8	
			2.3 − 2.7		−	0.7	
			1.4 − 2.3		−	$0.35 * V_{CCA}$	
			0.9 − 1.4		−	$0.1 * V_{CCA}$	
V_{OH}	Output HIGH Voltage	I_{OH} = −100 μA; $V_I = V_{IH}$	0.9 − 4.5	0.9 − 4.5	$V_{CCB} − 0.2$	−	V
		I_{OH} = −0.5 mA; $V_I = V_{IH}$	0.9	0.9	$0.75 * V_{CCB}$	−	
		I_{OH} = −2 mA; $V_I = V_{IH}$	1.4	1.4	1.05	−	
		I_{OH} = −6 mA; $V_I = V_{IH}$	1.65	1.65	1.25	−	
			2.3	2.3	2.0	−	
		I_{OH} = −12 mA; $V_I = V_{IH}$	2.3	2.3	1.8	−	
			2.7	2.7	2.2	−	
		I_{OH} = −18 mA; $V_I = V_{IH}$	2.3	2.3	1.7	−	
			3.0	3.0	2.4	−	
		I_{OH} = −24 mA; $V_I = V_{IH}$	3.0	3.0	2.2	−	
V_{OL}	Output LOW Voltage	I_{OL} = 100 μA; $V_I = V_{IL}$	0.9 − 4.5	0.9 − 4.5	−	0.2	V
		I_{OL} = 0.5 mA; $V_I = V_{IH}$	1.1	1.1	−	0.3	
		I_{OL} = 2 mA; $V_I = V_{IH}$	1.4	1.4	−	0.35	
		I_{OL} = 6 mA; $V_I = V_{IL}$	1.65	1.65	−	0.3	
		I_{OL} = 12 mA; $V_I = V_{IL}$	2.3	2.3	−	0.4	
			2.7	2.7	−	0.4	
		I_{OL} = 18 mA; $V_I = V_{IL}$	2.3	2.3	−	0.6	
			3.0	3.0	−	0.4	
		I_{OL} = 24 mA; $V_I = V_{IL}$	3.0	3.0	−	0.55	
I_I	Input Leakage Current	$V_I = V_{CCA}$ or GND	0.9 − 4.5	0.9 − 4.5	−1.0	1.0	μA
I_{CCA}	Quiescent Supply Current	$V_I = V_{CCA}$ or GND; $I_O = 0$, $V_{CCA} = V_{CCB}$	0.9 − 4.5	0.9 − 4.5	−	2.0	μA
I_{CCB}	Quiescent Supply Current	$V_I = V_{CCA}$ or GND; $I_O = 0$, $V_{CCA} = V_{CCB}$	0.9 − 4.5	0.9 − 4.5	−	2.0	μA
$I_{CCA} + I_{CCB}$	Quiescent Supply Current	$V_I = V_{CCA}$ or GND; $I_O = 0$, $V_{CCA} = V_{CCB}$	0.9 − 4.5	0.9 − 4.5	−	4.0	μA
I_{OFF}	Power OFF Leakage Current	$V_I = 4.5$ V	0	0	−	5.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TOTAL STATIC POWER CONSUMPTION (I$_{CCA}$ + I$_{CCB}$)

	−40°C to +85°C										Unit
	V$_{CCB}$ (V)										
	4.5		3.3		2.8		1.8		0.9		
V$_{CCA}$ (V)	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
4.5		2		2		2		2		< 1.5	µA
3.3		2		2		2		2		< 1.5	µA
2.8		< 2		< 1		< 1		< 0.5		< 0.5	µA
1.8		< 1		< 1		< 0.5		< 0.5		< 0.5	µA
0.9		< 0.5		< 0.5		< 0.5		< 0.5		< 0.5	µA

NOTE: Connect ground before applying supply voltage V$_{CCA}$ or V$_{CCB}$. This device is designed with the feature that the power−up sequence of V$_{CCA}$ and V$_{CCB}$ will not damage the IC.

AC ELECTRICAL CHARACTERISTICS

			−40°C to +85°C										Unit
			V$_{CCB}$ (V)										
			4.5		3.3		2.8		1.8		1.2		
Symbol	Parameter	V$_{CCA}$ (V)	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t$_{PLH}$, t$_{PHL}$ (Note 1)	Propagation Delay, A to B	4.5		1.6		1.8		2.0		2.1		2.3	nS
		3.3		1.7		1.9		2.1		2.3		2.6	
		2.8		1.9		2.1		2.3		2.5		2.8	
		1.8		2.1		2.4		2.5		2.7		3.0	
		1.2		2.4		2.7		2.8		3.0		3.3	

1. Propagation delays defined per Figure 2.

CAPACITANCE

Symbol	Parameter	Test Conditions	Typ (Note 2)	Unit
C$_{I/O}$	I/O Pin Input Capacitance	V$_{CCA}$ = V$_{CCB}$ = 3.3 V, V$_I$ = 0 V or V$_{CCA/B}$	5.0	pF
C$_{PD}$	Power Dissipation Capacitance	V$_{CCA}$ = V$_{CCB}$ = 3.3 V, V$_I$ = 0 V or V$_{CCA}$, f = 10 MHz	5.0	pF

2. Typical values are at T$_A$ = +25°C.
3. C$_{PD}$ is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from:
   $I_{CC(operating)} \cong C_{PD} \times V_{CC} \times f_{IN}$ where $I_{CC} = I_{CCA} + I_{CCB}$.
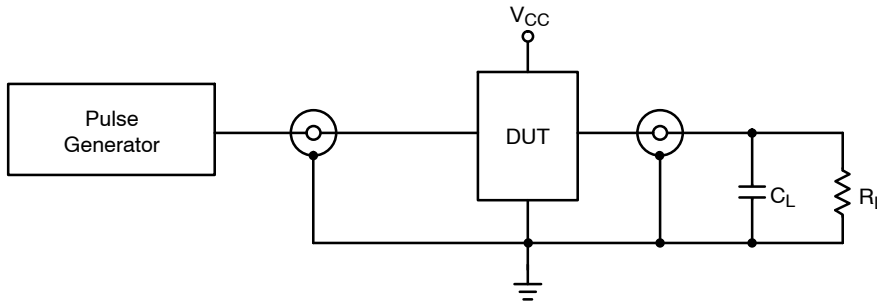
Figure 2. AC (Propagation Delay) Test Circuit

Test	Switch
C_L = 15 pF or equivalent (includes probe and jig capacitance) R_L = 2 kΩ or equivalent Z_{OUT} of pulse generator = 50 Ω	
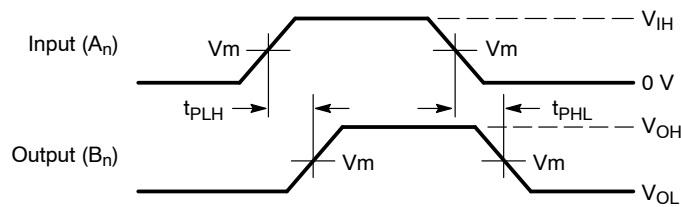
Waveform 1 – Propagation Delays
$t_R = t_F$ = 2.0 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns

Figure 3. AC (Propagation Delay) Test Circuit Waveforms

	V_{CC}
Symbol	**0.9 V – 4.5 V**
V_{mA}	$V_{CCA}/2$
V_{mB}	$V_{CCB}/2$

ORDERING INFORMATION

Device	Package	Shipping[†]
NLSV1T34MUTBG	UDFN6, 1.2 x 1.0, 0.4P (Pb−Free)	3000 / Tape & Reel
NLSV1T34AMUTCG	UDFN6, 1.45 x 1.0, 0.5P (Pb−Free)	3000 / Tape & Reel
NLSV1T34AMX1TCG	ULLGA6 (Pb−Free)	3000 / Tape & Reel
NLSV1T34DFT2G	SC−88A (Pb−Free)	3000 / Tape & Reel
NLVSV1T34DFT2G*		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

NLSV1T34

PACKAGE DIMENSIONS

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L
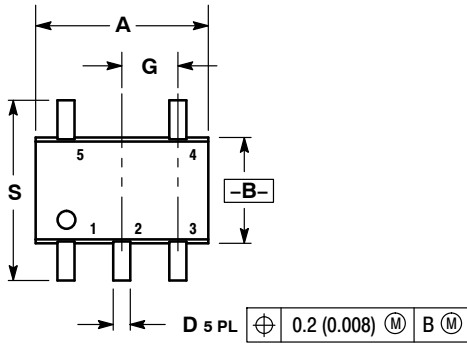
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

D 5 PL | ⊕ | 0.2 (0.008) Ⓜ | B Ⓜ

SOLDER FOOTPRINT

0.50 / 0.0197
0.65 / 0.025
0.65 / 0.025
0.40 / 0.0157
1.9 / 0.0748

SCALE 20:1   (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

UDFN6, 1.2x1.0, 0.4P
CASE 517AA
ISSUE D
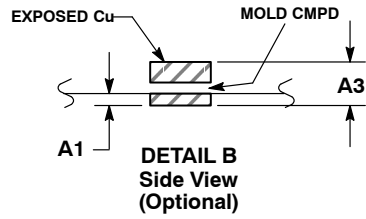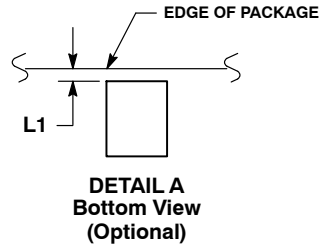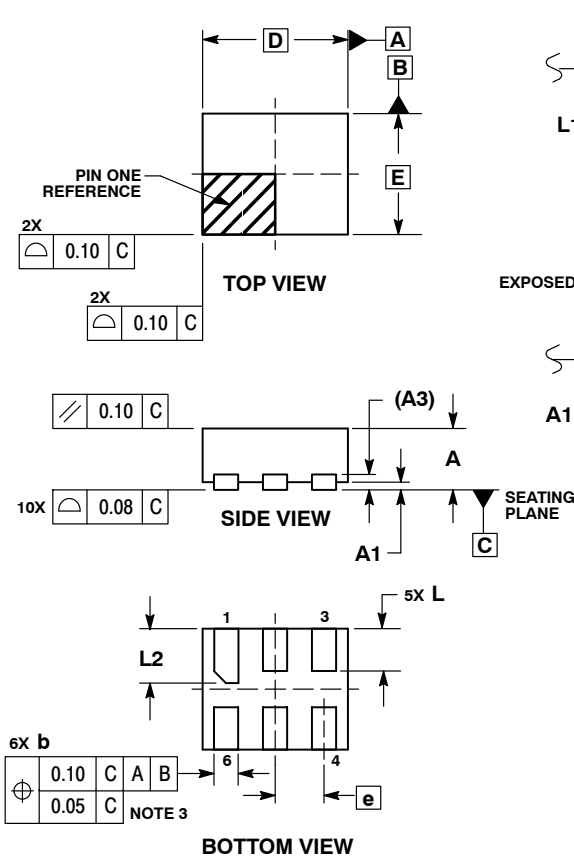
TOP VIEW

DETAIL A
Bottom View
(Optional)
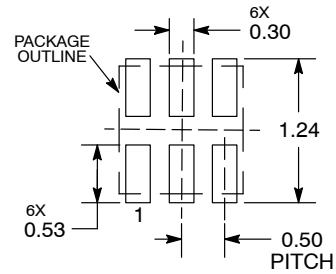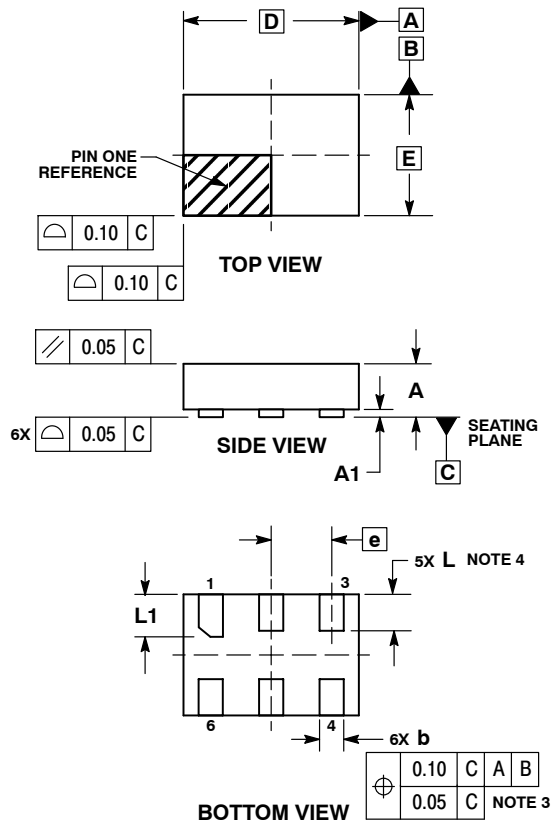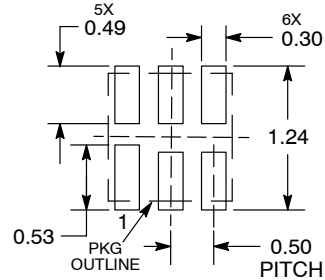
DETAIL B
Side View
(Optional)

SIDE VIEW

BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.20 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.30	0.40
L1	0.00	0.15
L2	0.40	0.50

MOUNTING FOOTPRINT*
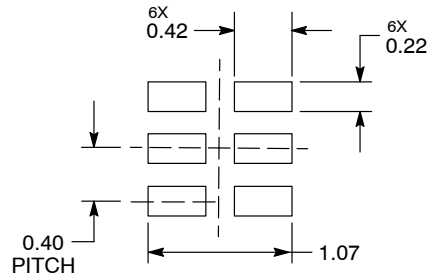
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NLSV1T34

PACKAGE DIMENSIONS

UDFN6, 1.45x1.0, 0.5P
CASE 517AQ
ISSUE O
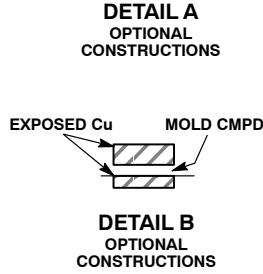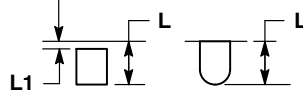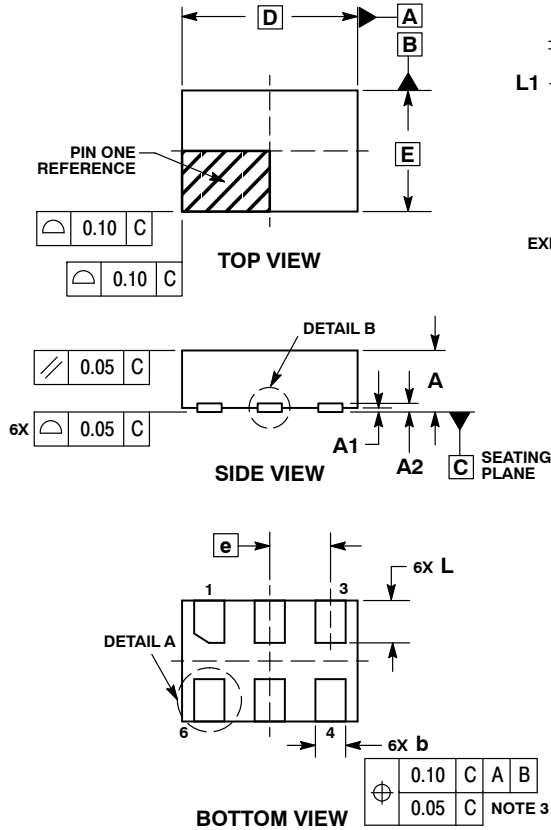
TOP VIEW

PIN ONE
REFERENCE

| 0.10 | C |
| 0.10 | C |

D

A
B

E

SIDE VIEW

DETAIL B

| 0.05 | C |
6X | 0.05 | C |

A
A1
A2

C SEATING PLANE

BOTTOM VIEW

DETAIL A

e
6X L

1
3

6
4

6X b

| ⊕ | 0.10 | C | A | B |
| | 0.05 | C | NOTE 3 |

DETAIL A
OPTIONAL
CONSTRUCTIONS

L
L1
L

DETAIL B
OPTIONAL
CONSTRUCTIONS

EXPOSED Cu   MOLD CMPD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07 REF	
b	0.20	0.30
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.30	0.40
L1	---	0.15

MOUNTING FOOTPRINT

PACKAGE
OUTLINE

6X
0.30

1.24

6X
0.53

1

0.50
PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

ULLGA6 1.45x1.0, 0.5P
CASE 613AF
ISSUE A

TOP VIEW

SIDE VIEW

SEATING PLANE

BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

| DIM | MILLIMETERS | |
	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT
SOLDERMASK DEFINED*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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