

## I<sup>2</sup>C LCD Module Calibrator

The ISL45045 is specifically designed to work in notebook applications where the system's EEPROM is powered up before the rest of the devices on the I<sup>2</sup>C bus. This enables data to be downloaded to a graphics card. The ESD protection scheme on the SDA, SCL and SCL\_S pins prevent the loading of the I<sup>2</sup>C bus during the initialization period prior to full power-up of the notebook.

The VCOM voltage of an LCD panel needs to be adjusted to remove flicker. This part provides a digital interface to control the sink-current output that attaches to an external voltage divider. The increase in output sink current lowers the voltage on the external divider, which is applied to an external VCOM buffer amplifier. The desired VCOM setting is loaded from an external source via a standard two-wire I<sup>2</sup>C serial interface. At power-up, the part automatically comes up at the last programmed setting in an on-board 7-bit EEPROM.

An external resistor attaches to the SET pin and sets the full-scale sink current that determines the lowest voltage of the external voltage divider.

The ISL45045 is available in an 10 Ld 3mmx3mm TDFN package with a maximum thickness of 0.8mm for ultra thin LCD panel design.

## Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL45045IRZ	045Z	0 to +85	10 Ld 3x3 TDFN	L10.3x3A
ISL45045IRZ-T*	045Z	0 to +85	10 Ld 3x3 TDFN	L10.3x3A

\*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Features

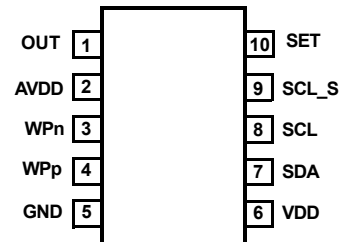
- 128-Step Adjustable Sink Current Output
- 2.25V to 3.6V Logic Supply Voltage Operating Range (2.6V Minimum Programming Voltage)
- Analog Supply Voltage Range 4.5V to 18V for VDD from 2.6V to 3.6V; 4.5V to 13V for VDD from 2.25V to 3.6V
- SDA, SCL, SCL\_S pins tolerant to system power-up sequences (i.e will not alter I<sup>2</sup>C bus state)
- I<sup>2</sup>C Interface (Slave and Transmitter) -- Address: 1001111
- On-board 7-bit EEPROM
- Output adjustment SET Pin
- Output Guaranteed Monotonic Over-Temperature
- Thin 10 Ld 3mmx3mm DFN (0.8mm max)
- Pb-Free (RoHS Compliant)

## Applications

- LCD Panels

## Pinout

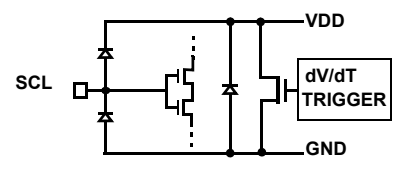
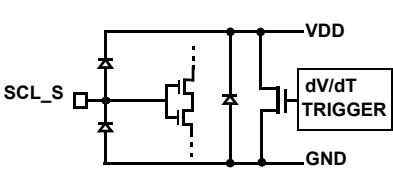
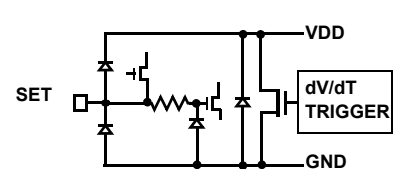
**ISL45045**  
**(10 LD TDFN)**  
TOP VIEW



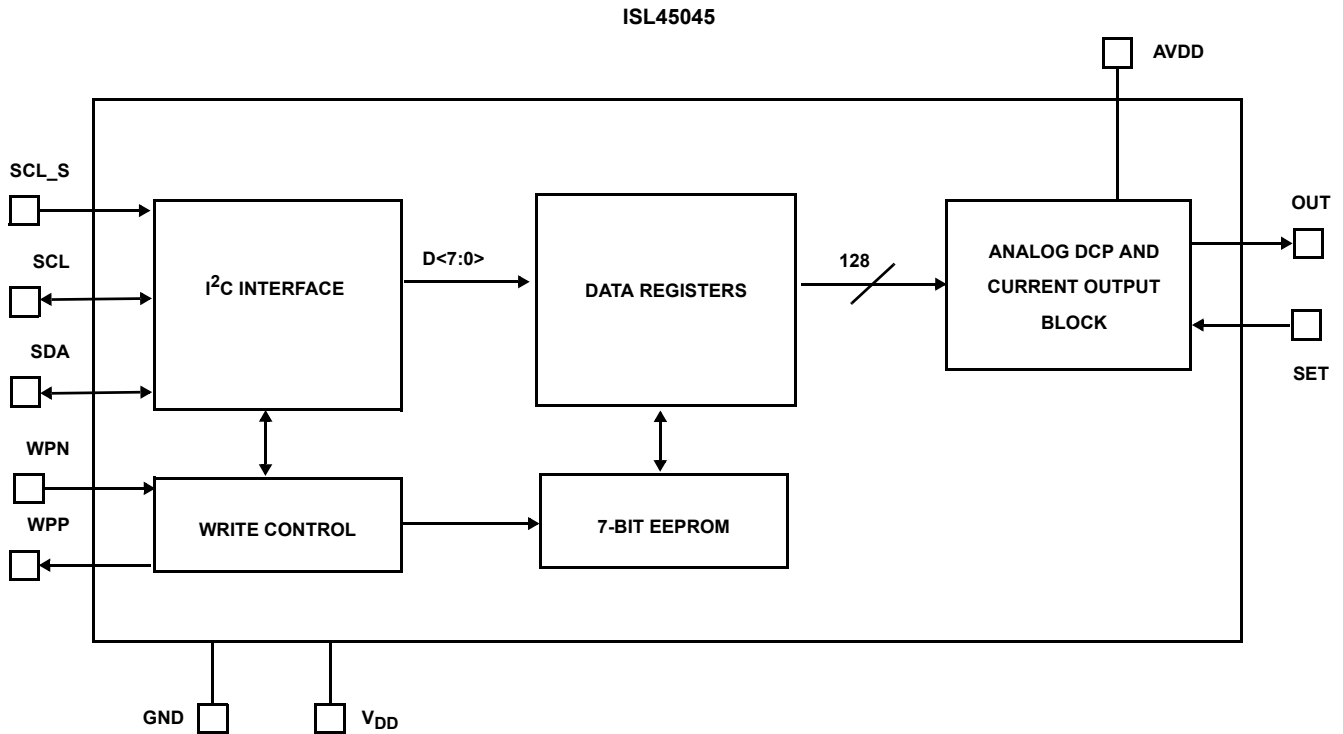
**Pin Descriptions**

PIN	TYPE	PULL U/D	FUNCTION	EQUIVALENT CIRCUIT
OUT	Output		Adjustable Sink Current Output Pin. The Current sinks into the OUT pin is equal to the DAC setting times the maximum adjustable sink current divided by 128. See SET pin function description for the maximum adjustable sink current setting.	
AV <sub>DD</sub>	Supply		High-Voltage Analog Supply. Bypass to GND with 0.1μF Capacitor.	
WP <sub>n</sub>	Input	Pull-Down	Write Protection Active Low. CMOS Level.	
WP <sub>p</sub>	Output		Output Pin. Opposite Logic Level of WP <sub>n</sub> Pin.	
GND	Supply		Ground.	
VDD	Supply		System Power Supply Input. Bypass to GND With 0.1μF Capacitor.	
SDA	In/Out	Open Drain Output	I <sup>2</sup> C Serial Data Input/Output.	

**Pin Descriptions** (Continued)

PIN	TYPE	PULL U/D	FUNCTION	EQUIVALENT CIRCUIT
SCL	In/Out	Open Drain Output	Serial Clock Input for Internal and Inter-IC Use.	
SCL_S	Input		Serial Clock Input.	
SET	Analog		Maximum Sink Current Adjustment Point. Connect a resistor from SET to GND to set the maximum adjustable sink current of the OUT pin. The maximum adjustable sink current is equal to $(AV_{DD}/20)$ divided by RSET.	

**Block Diagram**



**Absolute Maximum Ratings**

V <sub>DD</sub> to Ground	+4V
Input Voltages to GND	
SET	-0.3V to +4V
AVDD	-0.3V to +20V
Output Voltages to GND	
OUT	-0.3V to +20V
ESD Rating	
Human Body Model	.2kV

**Operating Conditions**

Temperature Range	0°C to +85°C
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**Thermal Information**

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (°C/W)
10 Ld TDFN Package	90
Moisture Sensitivity (see Technical Brief TB363)	
All Packages	Level 1
Maximum Junction Temperature (Plastic Package)	+150°C
Maximum Storage Temperature Range	-65°C to +150°C
Pb-free Reflow Profile	see link below
<a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>	
Erase/Write Cycles	10,000
Data Retention	10 years @ +85°C

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTE:

1.  $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

**Electrical Specifications**

Test Conditions: V<sub>DD</sub> = 3V, AVDD = 10V, OUT = 5V, R<sub>SET</sub> = 24.9k $\Omega$ ; Unless Otherwise Specified.  
Typicals are at T<sub>A</sub> = +25°C

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
<b>DC CHARACTERISTICS</b>							
V <sub>DD</sub> Supply Range -- Operating	V <sub>DD</sub>		Full	2.25	-	3.6	V
V <sub>DD</sub> Supply Range -- EEPROM Programming	V <sub>DD</sub>		Full	2.6	-	3.6	V
V <sub>DD</sub> Supply Current	I <sub>DD</sub>	(Note 4)	Full	-	-	50	$\mu$ A
AVDD Supply Range	AVDD	VDD range 2.6V to 3.6V	Full	4.5	-	18	V
		VDD range 2.25V to 3.6V		4.5	-	13	V
AVDD Supply Current	I <sub>AVDD</sub>	(Note 2)	Full	-	-	25	$\mu$ A
SET Voltage Resolution	SET <sub>VR</sub>		Full	7			Bits
SET Differential Nonlinearity	SET <sub>DN</sub>	Monotonic Over-Temperature	Full	-	-	$\pm$ 1	LSB
SET Zero-Scale Error	SET <sub>ZSE</sub>		Full	-	-	$\pm$ 2	LSB
SET Full-Scale Error	SET <sub>FSE</sub>		Full	-	-	$\pm$ 8	LSB
SET Current	I <sub>SET</sub>	Through R <sub>SET</sub> (Note 5)	Full	-	20	-	$\mu$ A
SET External Resistance	SET <sub>ER</sub>	To GND, AVDD = 20V	Full	10	-	200	k $\Omega$
		To GND, AVDD = 4.5V	Full	2.25	-	45	k $\Omega$
AVDD to SET Voltage Attenuation	AVDD to SET	(Note 3)	Full	-	1:20	-	V/V
OUT Settling Time	OUT <sub>ST</sub>	to $\pm$ 0.5 LSB Error Band (Note 3)	Full	-	8	-	$\mu$ s
OUT Voltage Range	V <sub>OUT</sub>		Full	VSET + 0.5V	-	13	V
SET Voltage Drift	SET <sub>VD</sub>	(Note 3)	25 to 55	-	<10	-	mV
SDA, SCL, SCL_S, WPn Input Logic High	V <sub>IH</sub>		Full	0.7*VDD	-	-	V
SDA, SCL, SCL_S, WPn Input Logic Low	V <sub>IL</sub>		Full	-	-	0.3*VDD	V
SDA, SCL, SCL_S, WPn Hysteresis		(Note 3)	Full	-	0.22*VDD	-	V

# ISL45045

**Electrical Specifications** Test Conditions:  $V_{DD} = 3V$ ,  $AVDD = 10V$ ,  $OUT = 5V$ ,  $R_{SET} = 24.9k\Omega$ ; Unless Otherwise Specified.  
Typicals are at  $T_A = +25^\circ C$  (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
WPn IL	$I_{LWPn}$		Full	15	25	35	$\mu A$
SDA, SCL Output Logic High	$VOH_S$	@ 3mA	Full	0.4	-	-	V
SDA, SCL Output Logic Low	$VOL_S$	@ 3mA	Full	-	-	0.4	V
WPP Output Logic High	$VOH_{WPP}$	@ 3mA	Full	$V_{DD} - 0.4$	-	-	V
WPP Output Logic Low	$VOL_{WPP}$	@ 3mA	Full	0.4	-	-	V
WPP Delay	$t_{DWPP}$		Full	-	-	100	ns
SCL_S to SCL On Resistance			Full	-	-	75	$\Omega$
Delay From SCL_S to SCL	$t_S$		Full	-	-	60	ns
<b>I<sup>2</sup>C</b>							
SCL Clock Frequency	$F_{SCL}$		Full	0	-	400	kHz
I <sup>2</sup> C Clock High Time	$t_{SCH}$		Full	0.6	-	-	$\mu s$
I <sup>2</sup> C Clock Low Time	$t_{SCL}$		Full	1.3	-	-	$\mu s$
I <sup>2</sup> C Spike Rejection Filter Pulse Width	$t_{DSP}$		Full	0	-	50	ns
I <sup>2</sup> C Data Set-up Time	$t_{SDS}$		Full	100	-	-	ns
I <sup>2</sup> C Data Hold Time	$t_{SDH}$		Full	0	-	900	ns
I <sup>2</sup> C SDA, SCL Input Rise Time	$t_{ICR}$	Dependent on Load (Note 6)	Full	-	$20 + 0.1 \cdot C_b$	1000	ns
I <sup>2</sup> C SDA, SCL Input Fall Time	$t_{ICF}$	(Note 6)	Full	-	$20 + 0.1 \cdot C_b$	300	ns
I <sup>2</sup> C Bus Free Time Between Stop and Start	$t_{BUF}$		Full	1.3	-	-	$\mu s$
I <sup>2</sup> C Repeated Start Condition Set-up	$t_{STS}$		Full	0.6	-	-	$\mu s$
I <sup>2</sup> C Repeated Start Condition Hold	$t_{STH}$		Full	0.6	-	-	$\mu s$
I <sup>2</sup> C Stop Condition Set-up	$t_{SPS}$		Full	0.6	-	-	$\mu s$
I <sup>2</sup> C Bus Capacitive Load	$C_b$		Full	-	-	400	pF
Capacitance on SDA	$C_{SDA}$		Full	-	-	10	pF
Capacitance on SCL, SCL_S	$C_S$	WPn = 0	Full	-	-	10	pF
		WPn = 1		-	-	22	pF
Write Cycle Time	$t_W$		Full	-	-	100	ms

**NOTES:**

2. Tested at  $AVDD = 18V$ .
3. Simulated and Determined via Design and NOT Directly Tested.
4. Simulated Maximum Current Draw when Programming EEPROM is 23mA, should be considered when designing Power Supply.
5. A Typical Current of 20 $\mu A$  is Calculated using the  $AVDD = 10V$  and  $R_{SET} = 24.9k\Omega$ . The maximum suggested SET Current should be 120 $\mu A$ .
6. Simulated and Designed According to I<sup>2</sup>C Specifications.
7. Parameters with MIN and/or MAX limits are 100% tested at +25 $^\circ C$ , unless otherwise specified. Temperature limits established by characterization and are not production tested.

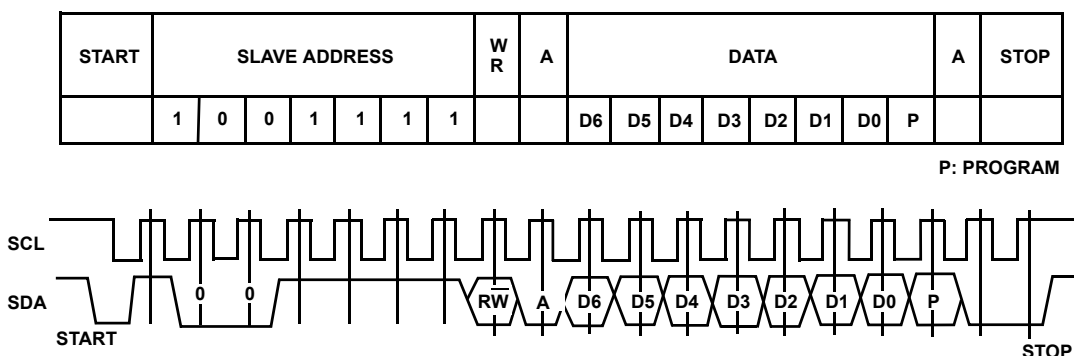
**Truth Tables**

TABLE 1. DVR WRITE PROTECTION TRUTH TABLE

INPUT			OUTPUT		
WPn	SCL_S	SCL	WPp	REGISTER	EEPROM
LOW	UNUSED	INPUT	HIGH	Write Protect	Write Protect
HIGH	CONNECTED TO SCL	CONNECTED TO SCL_S	LOW	Writeable	Writeable
HIGH to LOW	DISCONNECTS FROM SCL	DISCONNECTS FROM SCL_S	LOW to HIGH	EEPROM is Read into Register	EEPROM is Read into Register
FLOAT (Pull-Down Resistor Included)	UNUSED	INPUT	HIGH	Write Protect	Write Protect

NOTE: When the device is not write-protected SCL\_S and SCL signals should not be driven at the same time. When SCL\_S signal is "Unused" should be left floating.

**I<sup>2</sup>C Bus Format**



When Read Operation, don't care P.  
 P = 1: Register Writing  
 P = 0: EEPROM Writing (Program)

**Application Information**

This device provides the ability to reduce the flicker of an LCD panel by adjustment of the VCOM voltage during production test and alignment. A 128-step resolution is provided under digital control, which adjusts the sink current of the output. The output is connected to an external voltage divider, so that the device will have the capability to reduce the voltage on the output by increasing the output sink current.

The adjustment of the output is provided by the two-wire I<sup>2</sup>C serial interface.

**Adjustable Sink Current Output**

The device provides an output sink current which lowers the voltage on the external voltage divider. Equations 1 and 2 control the output. See Figure 1.

$$I_{OUT} = \frac{\text{Setting}}{128} \times \frac{AVDD}{20(R_{SET})} \quad (\text{EQ. 1})$$

$$V_{OUT} = \left( \frac{R_2}{R_1 + R_2} \right) VA_{VDD} \left( 1 - \frac{\text{Setting}}{128} \times \frac{R_1}{20(R_{SET})} \right) \quad (\text{EQ. 2})$$

Note: Where (Setting) is indicated, must be an integer between 1 and 128.

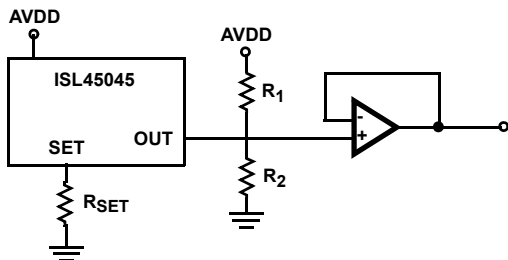
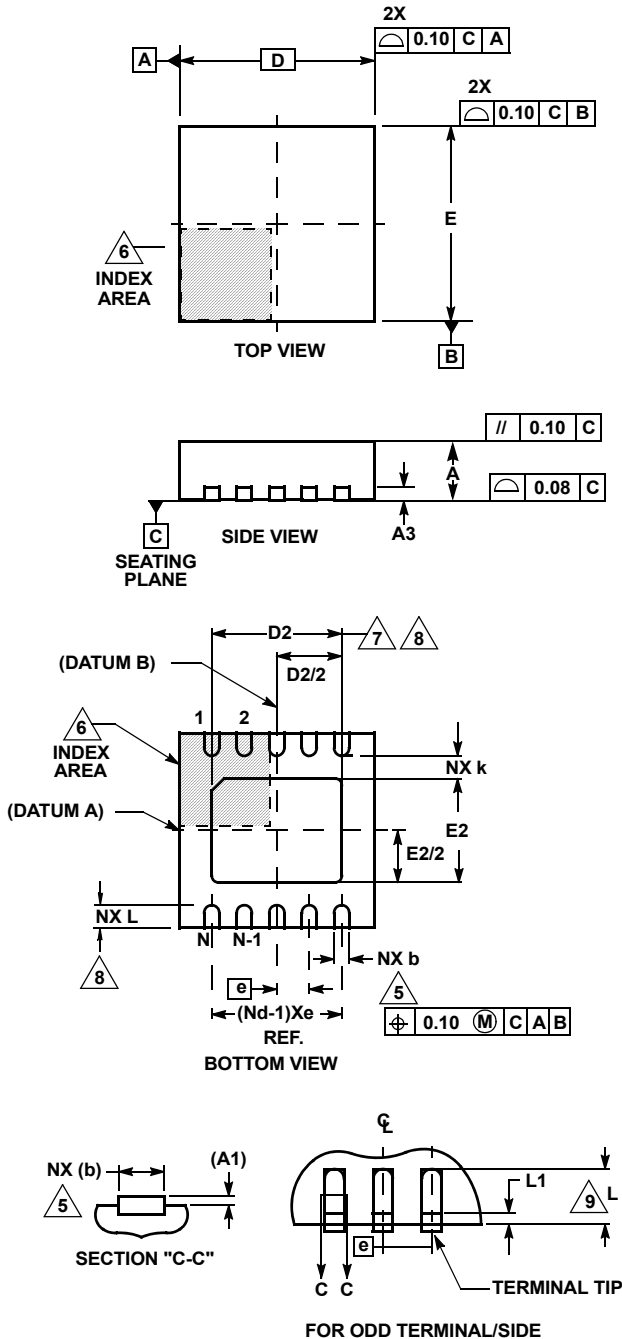


FIGURE 1. OUTPUT CONNECTION CIRCUIT EXAMPLE

**Ramp-up of the VDD Power Supply**

It is required that the ramp-up from 10% VDD to 90% VDD achieved in less than or equal to 10ms to assure that the EEPROM and Power-on-reset circuits are synchronized and the correct value is read from the EEPROM Memory.

Thin Dual Flat No-Lead Plastic Package (TDFN)



L10.3x3A

10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A3	0.20 REF			-
b	0.20	0.25	0.30	5, 8
D	2.95	3.0	3.05	-
D2	2.25	2.30	2.35	7, 8
E	2.95	3.0	3.05	-
E2	1.45	1.50	1.55	7, 8
e	0.50 BSC			-
k	0.25	-	-	-
L	0.25	0.30	0.35	8
N	10			2
Nd	5			3

Rev. 3 3/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Compliant to JEDEC MO-229-WEED-3 except for D2 dimensions.

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