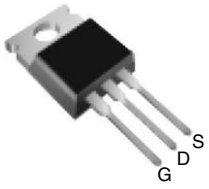
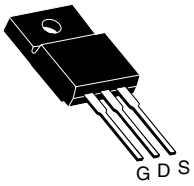
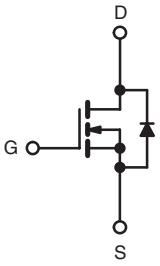
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	560	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.225
Q_g (Max.) (nC)	76	
Q_{gs} (nC)	21	
Q_{gd} (nC)	29	
Configuration	Single	

TO-220 TO-220 FULLPAK







N-Channel MOSFET

FEATURES

- Low Figure-of-Merit R_{on} x Q_g
- 100 % Avalanche Tested
- High Peak Current Capability
- dV/dt Ruggedness
- Improved t_{rr}/Q_{rr}
- Improved Gate Charge
- High Power Dissipations Capability
- Compliant to RoHS Directive 2002/95/EC

Available
RoHS* COMPLIANT

ORDERING INFORMATION		
Package	TO-220	TO-220 FULLPAK
Lead (Pb)-free	SiHP18N50C-E3	SiHF18N50C-E3

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted					
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage			V_{DS}	500	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current (T_J = 150 °C)[a]	V_{GS} at 10 V	T_C = 25 °C	I_D	18	A
		T_C = 100 °C		11	
Pulsed Drain Current[b]			I_{DM}	72	
Linear Derating Factor		TO-220		1.8	W/°C
		FULLPAK		0.3	
Single Pulse Avalanche Energy[c]			E_{AS}	361	mJ
Maximum Power Dissipation		TO-220	P_D	223	W
		FULLPAK		38	
Peak Diode Recovery dV/dt[d]			dV/dt	5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)[d]	for 10 s			300	

Notes

a. Drain current limited by maximum junction temperature.
b. Repetitive rating; pulse width limited by maximum junction temperature.
c. V_{DD} = 50 V, starting T_J = 25 °C, L = 2.5 mH, R_g = 25 Ω, I_{AS} = 17 A.
d. $I_{SD} \leq$ 18 A, dI/dt ≤ 380 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C.
e. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS					
PARAMETER		**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	TO-220	R_{thJA}	-	62	°C/W
	FULLPAK		-	65	
Maximum Junction-to-Case (Drain)	TO-220	R_{thJC}	-	0.56	
	FULLPAK		-	3.29	

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.6	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 30 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	-	-	25	µA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A	-	0.225	0.270	Ω
Forward Transconductance[a]	g_{fs}	V_{DS} = 50 V, I_D = 10 A	-	6.4	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz	-	2451	2942	pF
Output Capacitance	C_{oss}		-	300	360	
Reverse Transfer Capacitance	C_{rss}		-	26	32	
Internal Gate Resistance	R_g	f = 1.0 MHz, open drain	-	1.1	-	Ω
Total Gate Charge	Q_g	V_{GS} = 10 V, I_D = 18 A, V_{DS} = 400 V	-	65	76	nC
Gate-Source Charge	Q_{gs}		-	21	-	
Gate-Drain Charge	Q_{gd}		-	29	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 250 V, I_D = 18 A, R_g = 7.5 Ω, V_{GS} = 10 V	-	80	-	ns
Rise Time	t_r		-	27	-	
Turn-Off Delay Time	$t_{d(off)}$		-	32	-	
Fall Time	t_f		-	44	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	18	A
Pulsed Diode Forward Current	I_{SM}		-	-	72	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 18 A, V_{GS} = 0 V	-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = I_S, dI/dt = 100 A/µs, V_R = 35 V	-	503	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	6.7	-	µC
Reverse Recovery Current	I_{RRM}		-	30	-	A

Note

a. Repetitive rating; pulse width limited by maximum junction temperature.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

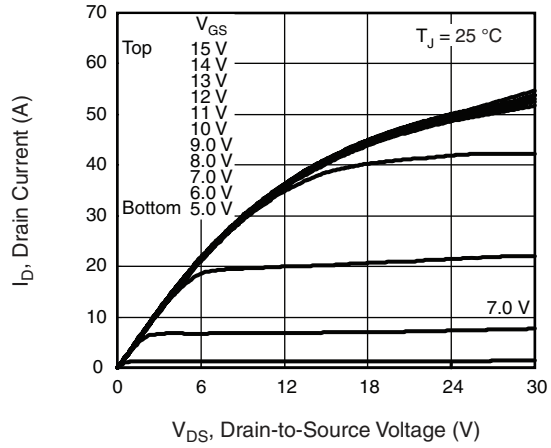


Fig. 1 - Typical Output Characteristics, T_C = 150 °C (TO-220)

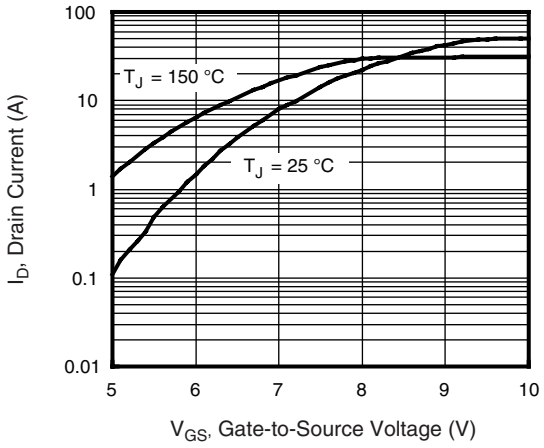


Fig. 3 - Typical Transfer Characteristics

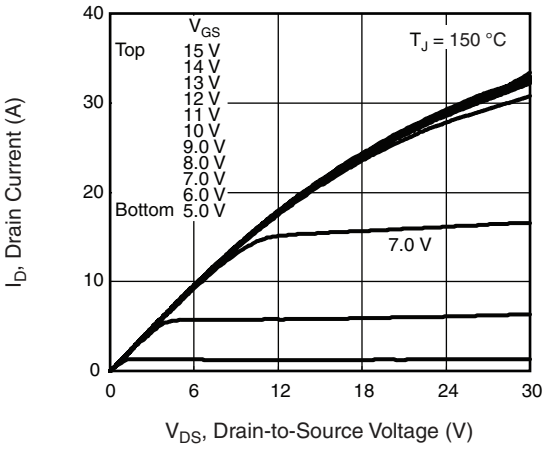


Fig. 2 - Typical Output Characteristics, T_C = 150 °C (TO-220)

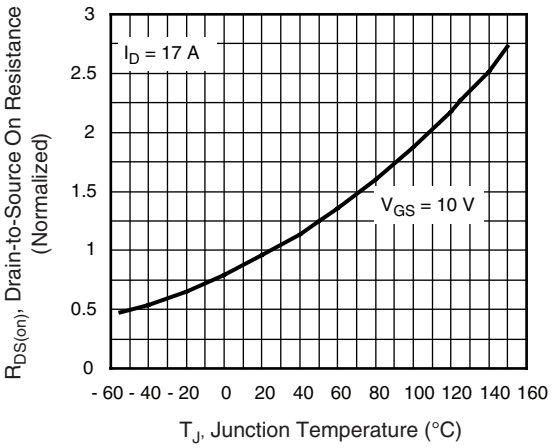


Fig. 4 - Normalized On-Resistance vs. Temperature

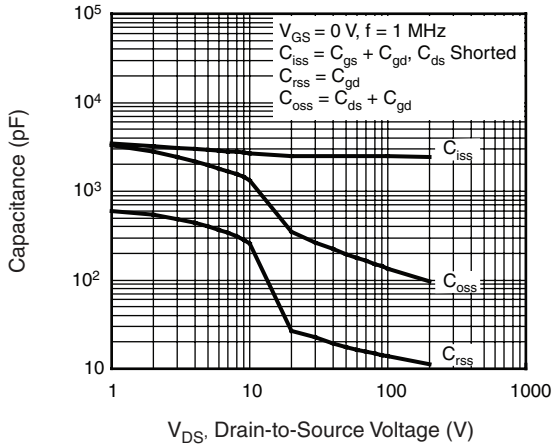


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

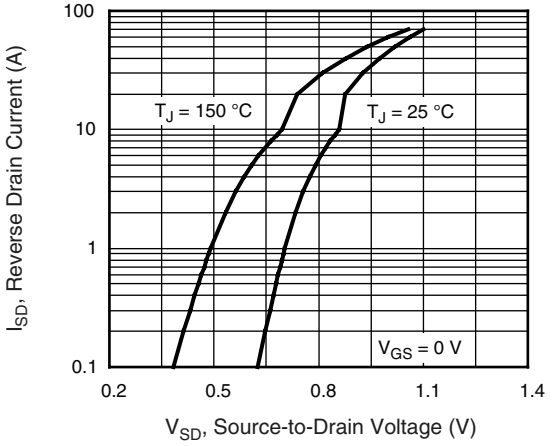


Fig. 7 - Typical Source-Drain Diode Forward Voltage

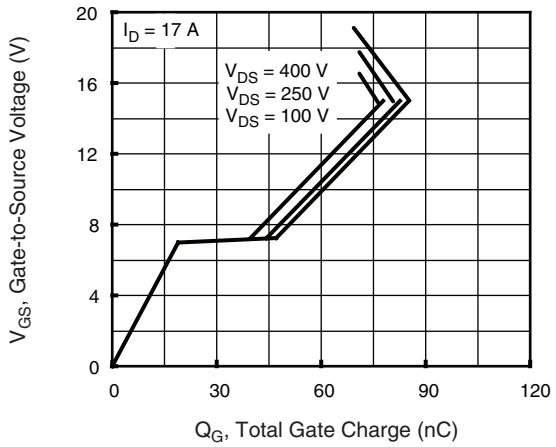


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

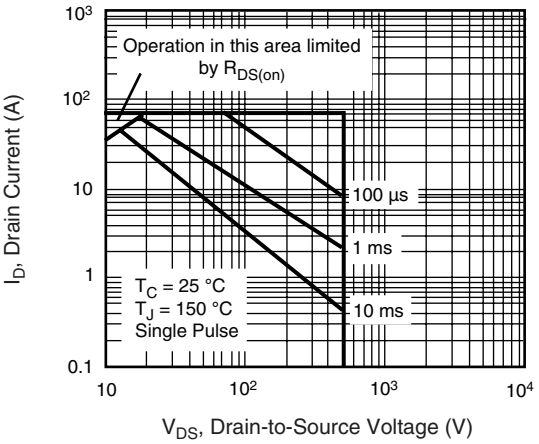


Fig. 8 - Maximum Safe Operating Area

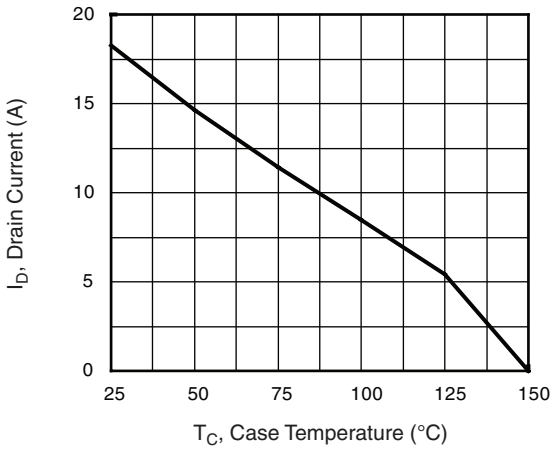


Fig. 9 - Maximum Drain Current vs. Case Temperature (TO-220)

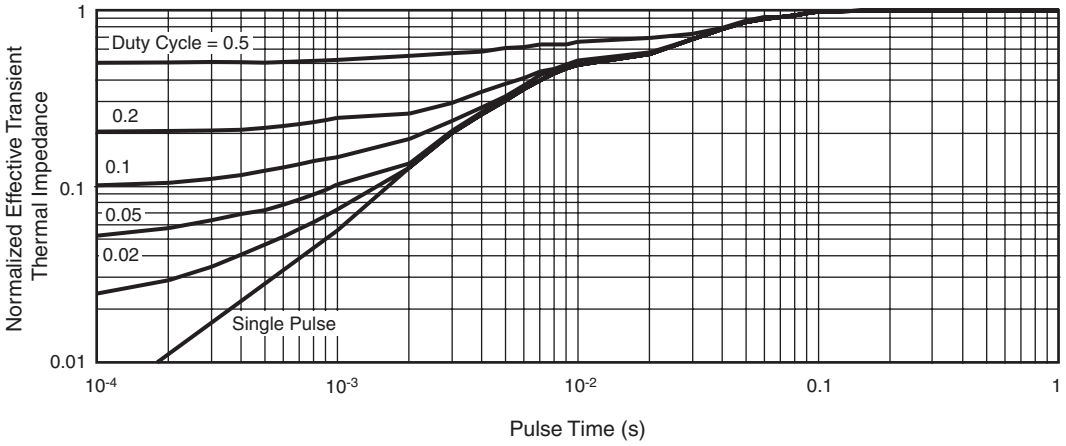


Fig. 10 - Normalized Thermal Transient Impedance, Junction-to-Case (TO-220)

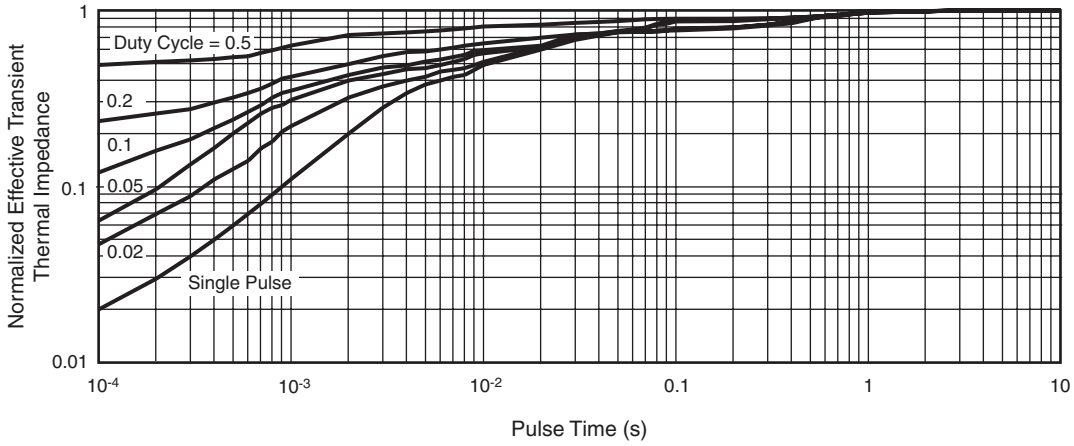


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case (TO-220FP)

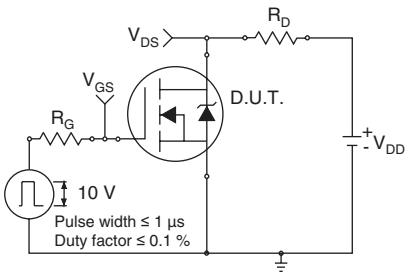


Fig. 12a - Switching Time Test Circuit

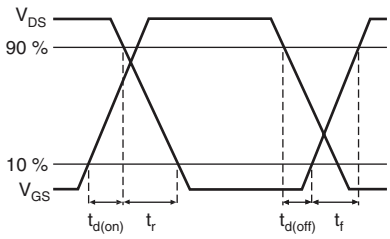


Fig. 12b - Switching Time Waveforms

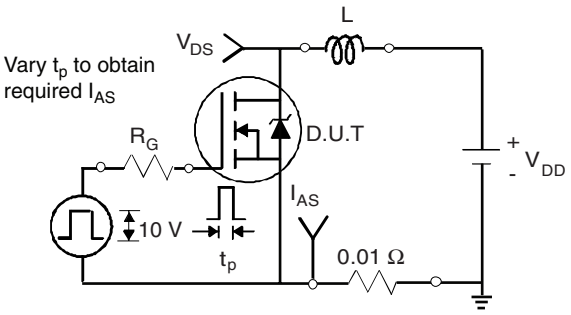


Fig. 13a - Unclamped Inductive Test Circuit

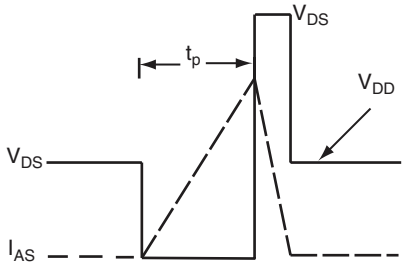


Fig. 13b - Unclamped Inductive Waveforms

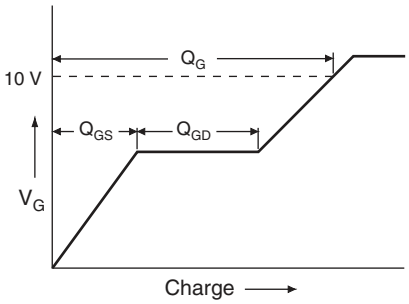


Fig. 14a - Basic Gate Charge Waveform

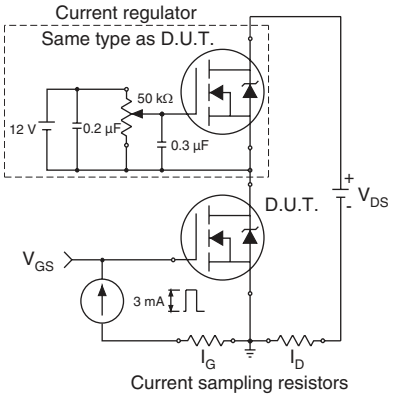
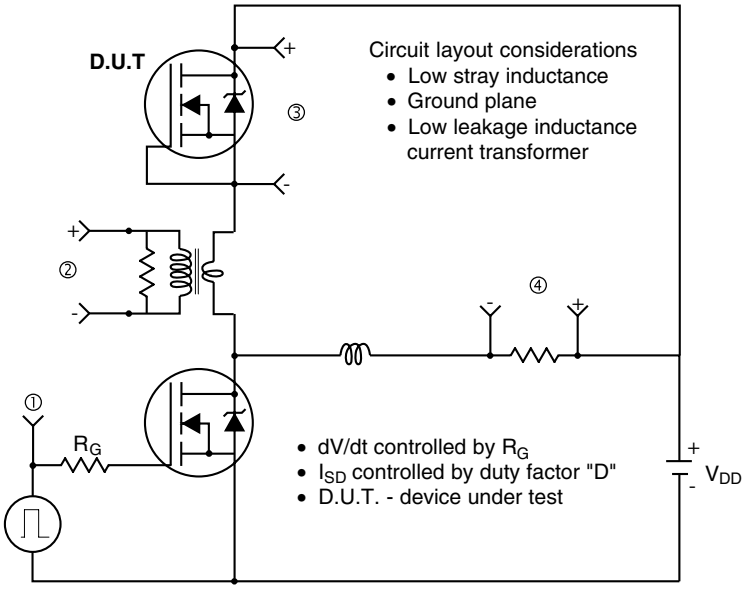
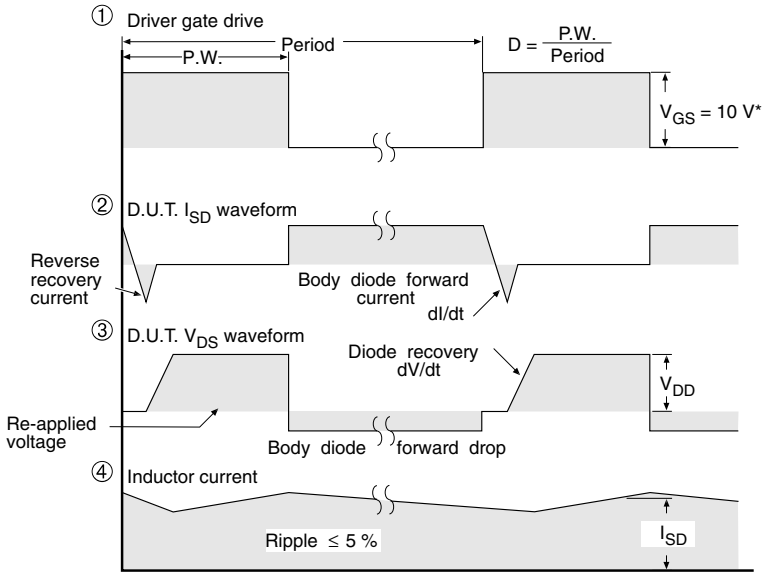


Fig. 14b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





* V_{GS} = 5 V for logic level and 3 V drive devices

Fig. 15 - For N-Channel

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