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# FDC637BNZ

## N-Channel 2.5V Specified PowerTrench® MOSFET

### 20V, 6.2A, 24mΩ

#### Features

- Max  $r_{DS(on)}$  = 24mΩ at  $V_{GS} = 4.5V$ ,  $I_D = 6.2A$
- Max  $r_{DS(on)}$  = 32mΩ at  $V_{GS} = 2.5V$ ,  $I_D = 5.2A$
- Fast switching speed
- Low gate charge (8nC typical)
- High performance trench technology for extremely low  $r_{DS(on)}$
- SuperSOT™-6 package: small footprint (72% smaller than standard SO-8; low profile (1mm thick)
- HBM ESD protection level > 2kV typical (Note 3)
- Manufactured using green packaging material
- Halide-Free
- RoHS Compliant



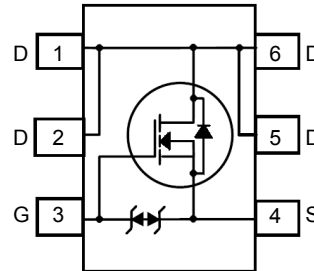
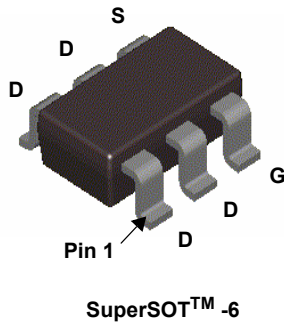
#### General Description

This N-Channel 2.5V specified MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

These devices have been designed to offer exceptional power dissipation in a very small footprint compared with bigger SO-8 and TSSOP-8 packages.

#### Applications

- DC - DC Conversion
- Load switch
- Battery Protection



#### MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	20	V
$V_{GS}$	Gate to Source Voltage	±12	V
$I_D$	Drain Current -Continuous $T_A = 25^\circ C$ (Note 1a)	6.2	A
	-Pulsed	20	
$P_D$	Power Dissipation $T_A = 25^\circ C$ (Note 1a)	1.6	W
	Power Dissipation $T_A = 25^\circ C$ (Note 1b)	0.8	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

#### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	78	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	156	

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.637Z	FDC637BNZ	SSOT6	7"	8mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		10		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{V}, V_{GS} = 0\text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{V}, V_{DS} = 0\text{V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	0.6	0.8	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-3		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 4.5\text{V}, I_D = 6.2\text{A}$		21	24	m $\Omega$
		$V_{GS} = 2.5\text{V}, I_D = 5.2\text{A}$		26	32	
		$V_{GS} = 4.5\text{V}, I_D = 6.2\text{A}, T_J = 125^\circ\text{C}$		30	41	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\text{V}, I_D = 6.2\text{A}$		27		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		670	895	pF
$C_{oss}$	Output Capacitance			160	215	pF
$C_{rss}$	Reverse Transfer Capacitance			115	175	pF
$R_g$	Gate Resistance	$f = 1\text{MHz}$		2.1		$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 10\text{V}, I_D = 6.2\text{A}, V_{GS} = 4.5\text{V}, R_{GEN} = 6\Omega$		8	16	ns
$t_r$	Rise Time			6	12	ns
$t_{d(off)}$	Turn-Off Delay Time			22	36	ns
$t_f$	Fall Time			6	12	ns
$Q_g$	Total Gate Charge	$V_{GS} = 4.5\text{V}, V_{DD} = 10\text{V}, I_D = 6.2\text{A}$		8	12	nC
$Q_{gs}$	Gate to Source Gate Charge			1.3		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			2.2		nC

### Drain-Source Diode Characteristics

$I_S$	Maximum Continuous Drain-Source Diode Forward Current			1.3	A	
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 1.3\text{A}$ (Note 2)		0.7	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 6.2\text{A}, di/dt = 100\text{A}/\mu\text{s}$		15	27	ns
$Q_{rr}$	Reverse Recovery Charge			5	10	nC

#### Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



a.  $78^\circ\text{C/W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper.

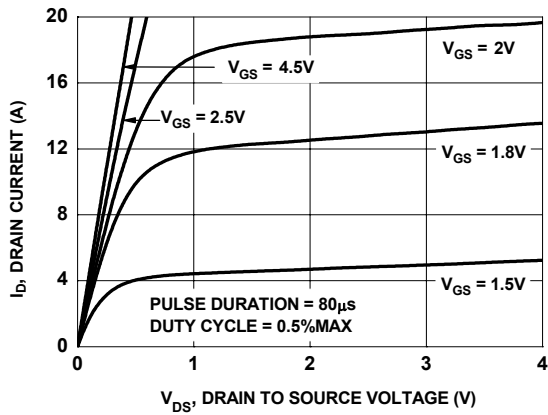


b.  $156^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

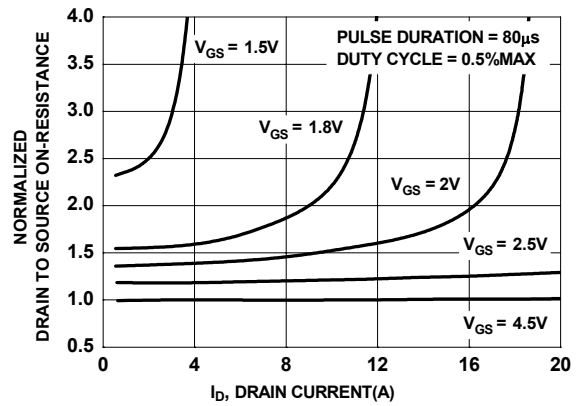
2. Pulse Test: Pulse Width  $< 300\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

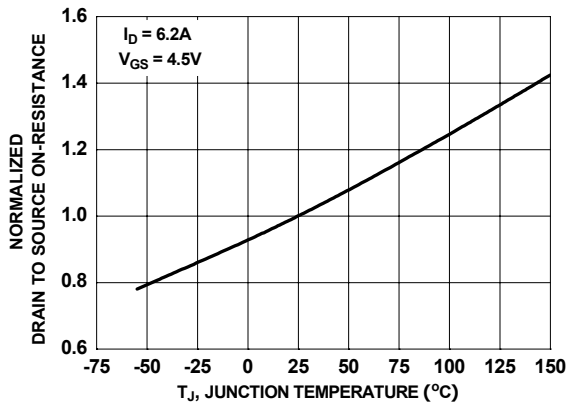
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



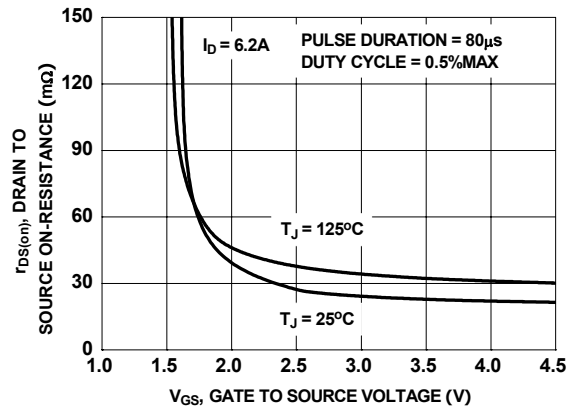
**Figure 1. On-Region Characteristics**



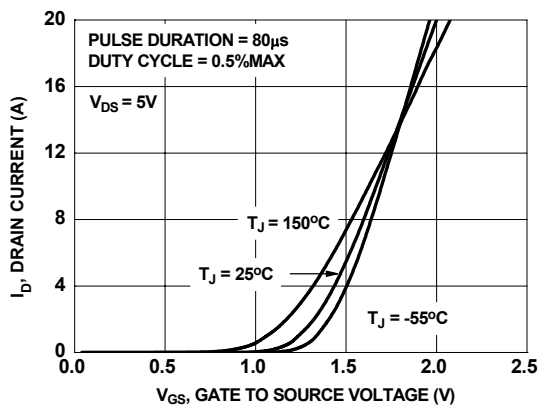
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



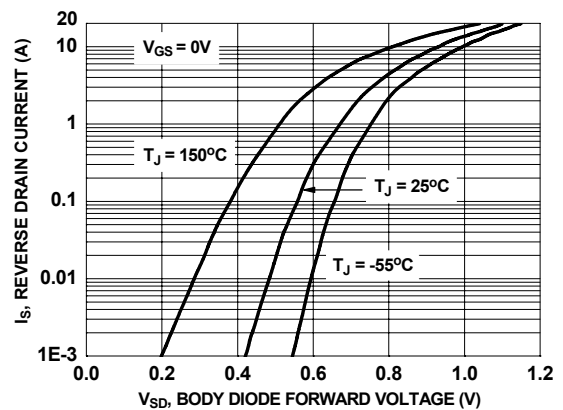
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

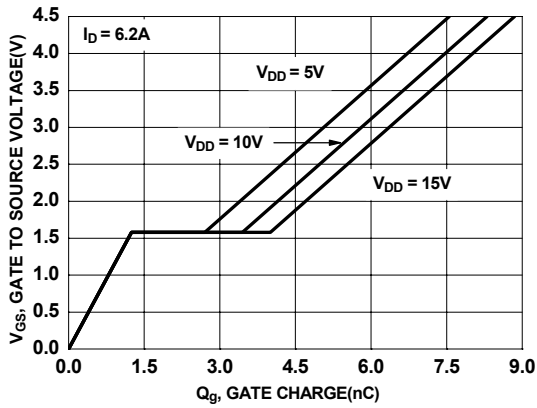


**Figure 5. Transfer Characteristics**

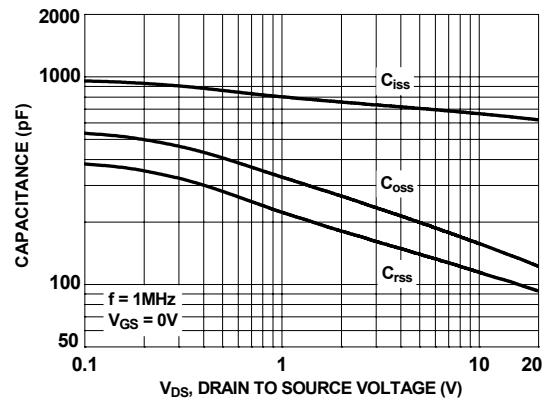


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

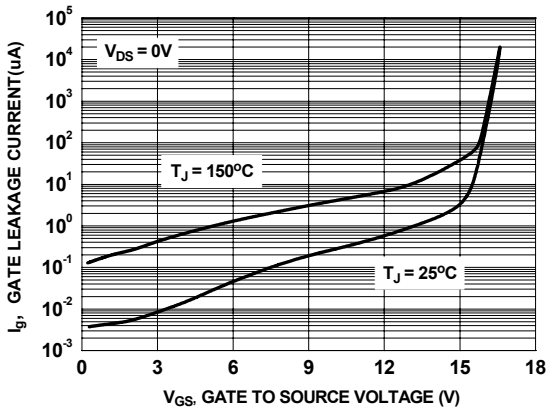
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



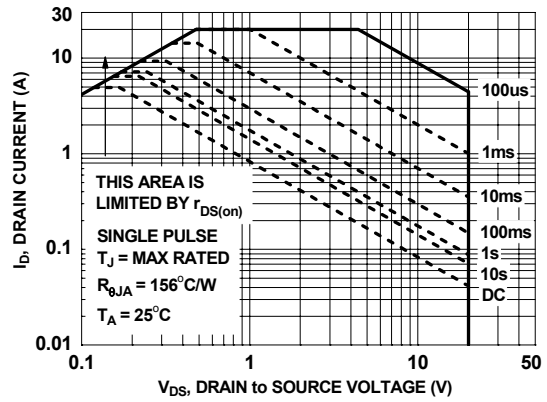
**Figure 7. Gate Charge Characteristics**



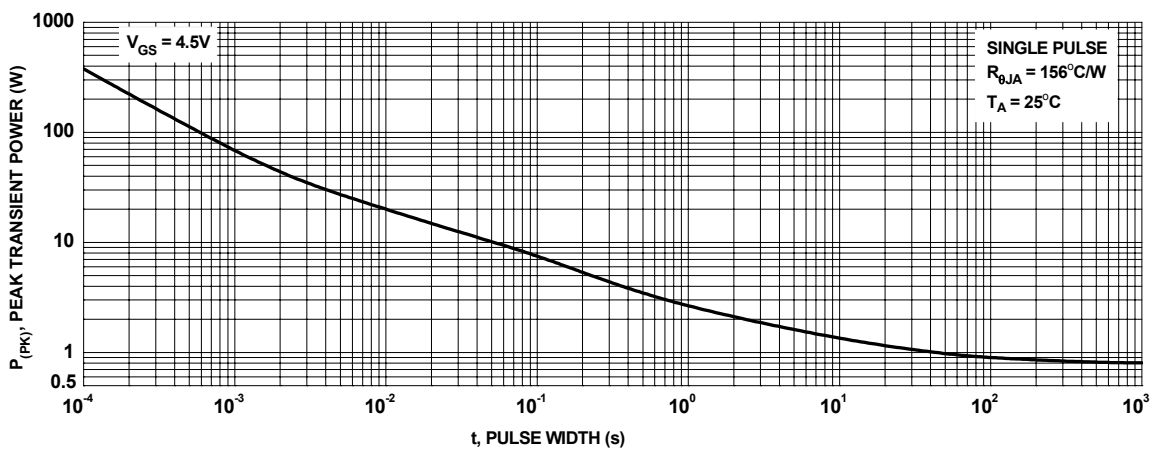
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Gate Leakage Current vs Gate to Source Voltage**

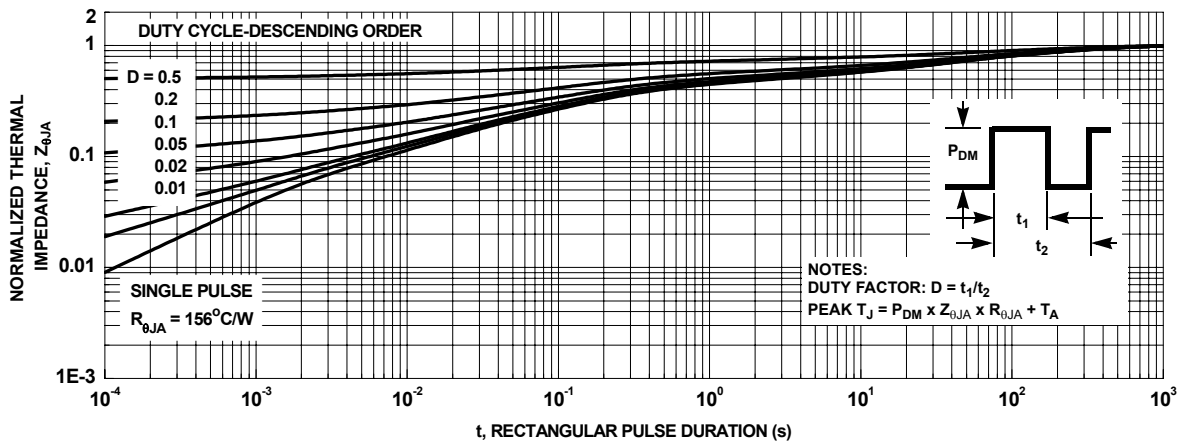


**Figure 10. Forward Bias Safe Operating Area**



**Figure 11. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted




**Figure 12. Transient Thermal Response Curve**



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