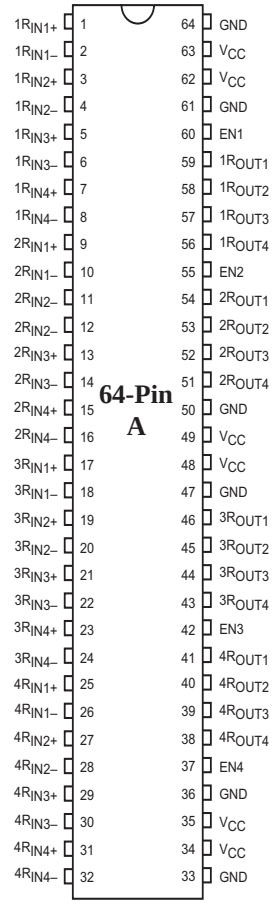
High-Speed Differential Line Receivers

Features

- Sixteen line receivers meet or exceed the requirements of the ANSI TIA/EIA-644-1995 Standard
- Designed for signaling rates up to 660 Mbps
- 0V to 3V common-mode input voltage range
- Operates from a single 3.3V supply
- Typical propagation delay time: 2.6ns
- Output skew 100ps (typical)
- Part-to-part skew is less than 1ns
- Integrated 110-Ohm termination on PI90LVT386
- Low Voltage TTL (LVTTL) levels are 5V tolerant
- Open-circuit fail safe
- Flow-through pin out
- Packaging (Pb-free & Green available):
  - 64-Pin Thin Shrink Small Output TSSOP (A)

Pin Configuration



16 Receivers

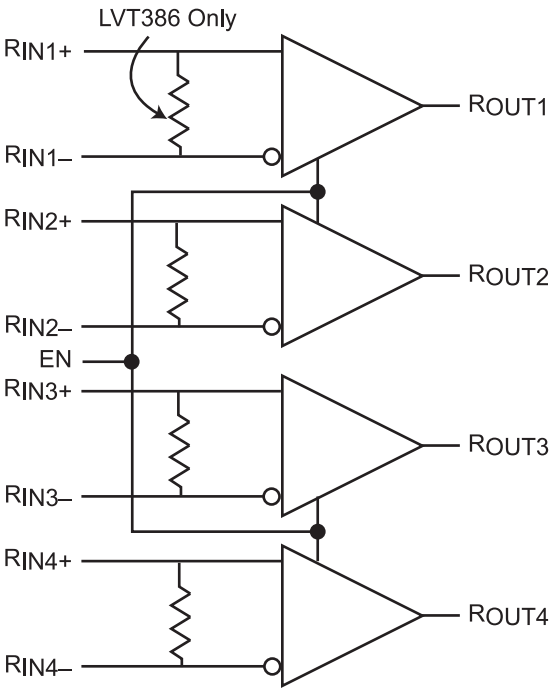
Description

The PI90LVx386 family consists of sixteen differential line receivers with 3-state outputs that implement Low-Voltage Differential Signaling (LVDS). Any of the differential receivers will provide a valid logical output state with a ±100mV differential input voltage within the input common-mode voltage range that allows 0 to 3V of ground potential difference between two LVDS nodes. The independent EN pins can be used to place the outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In high-impedance state, outputs neither load nor drive the bus lines.

The intended application of these devices, and their signaling techniques, is for point-to-point baseband data transmission over controlled impedance media of approximately 100-ohms with a 100-Ohm termination resistor. The PI90LVT386 integrates the terminating resistors while the PI90LV386 requires external resistors. The transmission media may be printed circuit board traces, backplanes, or cables. The PI90LV386's 16 receivers integrated into the same substrate allow precise timing alignment.

These parts are characterized for operation from –40°C to 85°C.

Block Diagram



1 of 4 LV386/LVT386

Absolute Maximum Ratings Over Operating Free-Air Temperature

(unless otherwise noted)†

Supply Voltage Range, V_{DD}(1) ..... –0.5V to 4V
Voltage Range: ..... Enables or R_{OUT}
–0.5V to V_{DD} +2V
R_{IN+} or $R_{IN–}$ ..... –0.5V to 4V
Electrostatic Discharge(2):
R_{IN+}, $R_{IN–}$, and GND ..... Class 3, A: 10kV, B:700V
All Pins ..... Class 3, A: 8kV, B:600V
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature 1,6mm (1/16 inch)
from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability.

Notes:
1. All voltage values, except differential I/O bus voltages, are with respect to ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7

Function Table

Differential Input	Enables	Output
R_{IN}±	EN	R_{OUT}
$V_{ID} \geq 100mV$	H	H
$-100mV < V_{ID} \leq 100mV$	H	?
$V_{ID} \leq -100mV$	H	L
X	L	Z
Open	H	H
X	H	R_{OUT_0}

Notes:
H = high level, L = low level, X = irrelevent
Z = high impedance (off), ? = indeterminate

Recommended Operating Conditions

	Min.	Nom.	Max.	Units
Supply Voltage, V_{CC}	3.0	3.3	3.6	V
High-Level Input Voltage, V_{IH}	2.0			
Low-Level Input Voltage, V_{IL}			0.8	
Magnitude of Differential Input Voltage $\lvert V_{ID} \rvert$	0.1		0.6	
Common-Mode input Voltage, V_{IC}	$\frac{\lvert V_{ID} \rvert}{2}$		$2.4 - \frac{\lvert V_{ID} \rvert}{2}$	
			V_{CC} –0.8	
Operating free-air temperature, T_A	–40		85	°C

Electrical Characteristics Over Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter		Test Conditions	Min.	Typ.(1)	Max.	Units
V_{ITH+}	Positive-going differential input voltage threshold					100	mV
V_{ITH-}	Negative-going differential input voltage threshold			–100			
V_{OH}	High-level output voltage		I_{OH} = –8mA	2.4	3.1		V
V_{OL}	Low-level output voltage		I_{OL} = 8mA		0.3	0.45	
I_{CC}	Supply Current		Enabled, No load		40	56	mA
			Disabled			3	
I_I	Input Current (R_{IN+} or R_{IN-} inputs)	LV	V_I = 0V			–20	µA
			V_I = 2.4V	–1.2			
		LVT	V_I = 0V, other input open			–40	
			V_I = 2.4V, other input open	–2.4			
$I_{I(OFF)}$	Power-off input current (R_{IN+} or R_{IN-} inputs)		V_{CC} = 0V, V_I = 2.4V		12	±20	
I_{IH}	High-level input current (enables)		V_{IH} =2V			10	
I_{IL}	Low-level input current (enables)		V_{IL} =0.8V				
I_{OZ}	High-impedance output current		V_O = 0V			±1	
			V_O = 3.6V			10	
C_{IN}	Input capacitance (R_{IN+} or R_{IN-} inputs to GND)		V_{ID} = 0.4 sin 2.5E09 t V		6		pF
$Z_{(t)}$	Termination Impedance (LVT)			88	110	143	Ohms

Note:
1. All typical values are at 25°C and with a 3.3V supply.

Switching Characteristics Over Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 2	1	2.2	3.1	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1	2.1	3.1	
t_r	Differential output signal rise time		500	900	1500	ps
t_f	Differential output signal fall time		500	820	1200	
$t_{sk(p)}$	Pulse skew ($t_{PHL} - t_{PLH}$)			120	244	
$t_{sk(o)}$	Output skew(2)			180	320	
$t_{sk(pp)}$	Part-to-part skew(3)				1	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 3(4)		2.5	3.7	
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			4.8	6.7	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			3.7	5.3	
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			6.4	8.7	
f_{MAX}	Maximum Clock frequency		300			MHz

Notes:
1. All typical values are at 25°C and with a 3.3V supply
2. $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.
3. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
4. R_{OUT0} disable time is 1 nanosecond greater.

Parameter Measurement Information

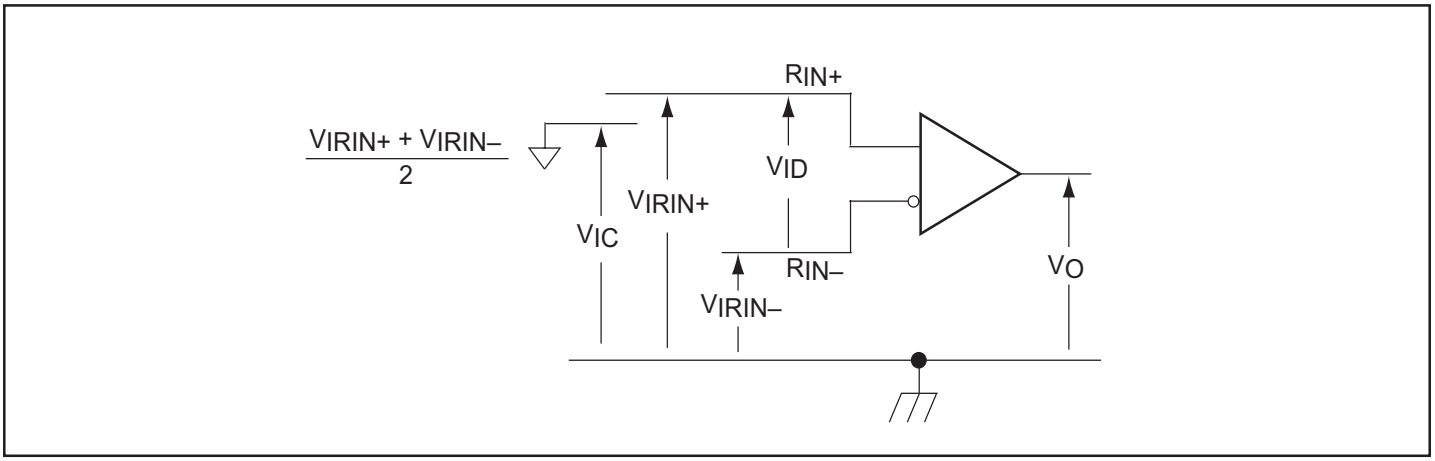
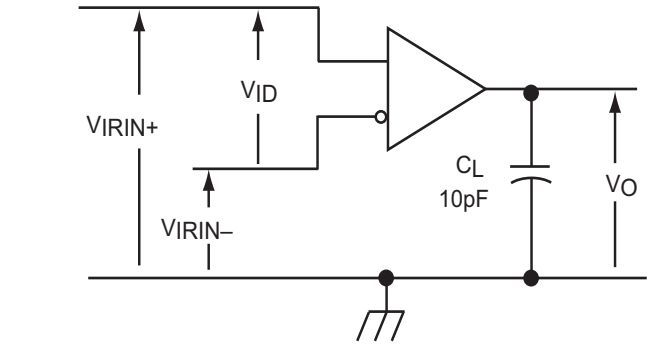


Figure 1. Voltage Definitions

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

Applied Voltages		Resulting Differential Input Voltage	Resulting Common-Mode Input Voltage
V_{IRIN+}	V_{IRIN-}	V_{ID}	V_{IC}
1.25V	1.15V	100mV	1.2V
1.15V	1.25V	–100mV	1.2V
2.4V	2.3V	100mV	2.35V
2.3V	2.4V	–100mV	2.35V
0.1V	0V	100mV	0.05V
0V	0.1V	–100mV	0.05V
1.5V	0.9V	600mV	1.2V
0.9V	1.5V	–600mV	1.2V
2.4V	1.8V	600mV	2.1V
1.8V	2.4V	–600mV	2.1V
0.6V	0V	600mV	0.3V
0V	0.6V	–600mV	0.3V

Parameter Measurement Information



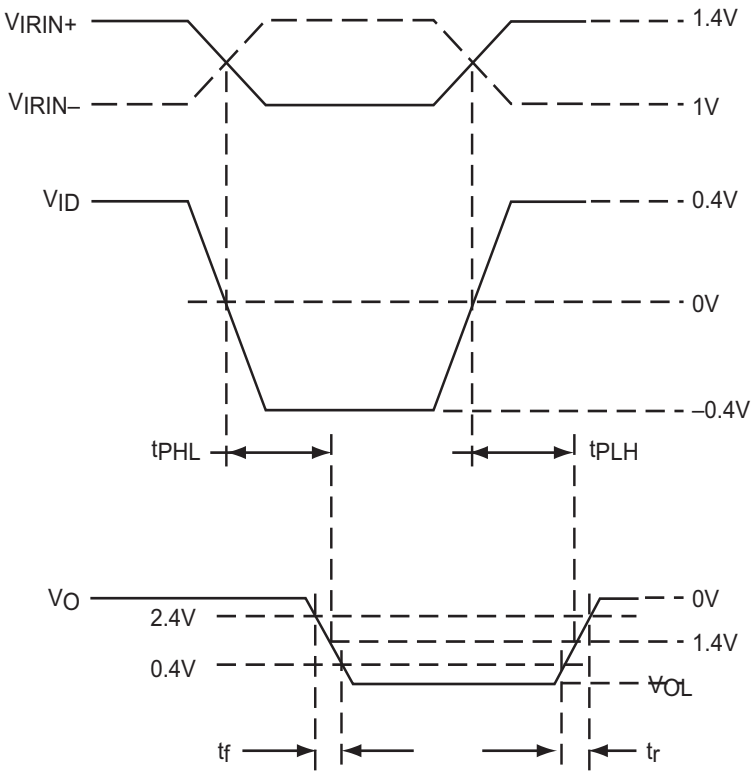
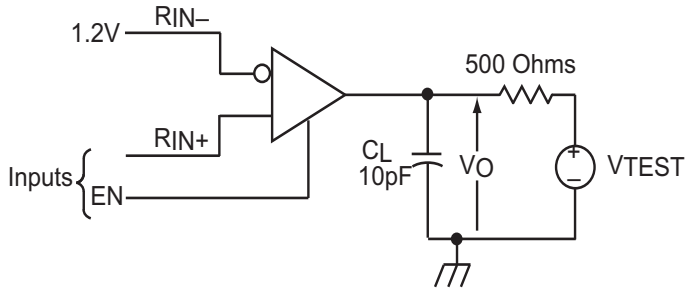


Figure 2. Timing Test Circuit and Waveforms

Note:

1. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1ns, Pulse Repetition Rate (PRR) = 50 Mpps, Pulse width = 10 ±0.2ns. C_L includes instrumentation and fixture capacitance within 0.06m of the D.U.T.

Parameter Measurement Information



Note:

1. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ns, Pulse Repetition Rate (PRR) = 0.5 Mpps, pulse width = 500 ±10ns. C_L includes instrumentation and fixture capacitance within 0.06m of the D.U.T.

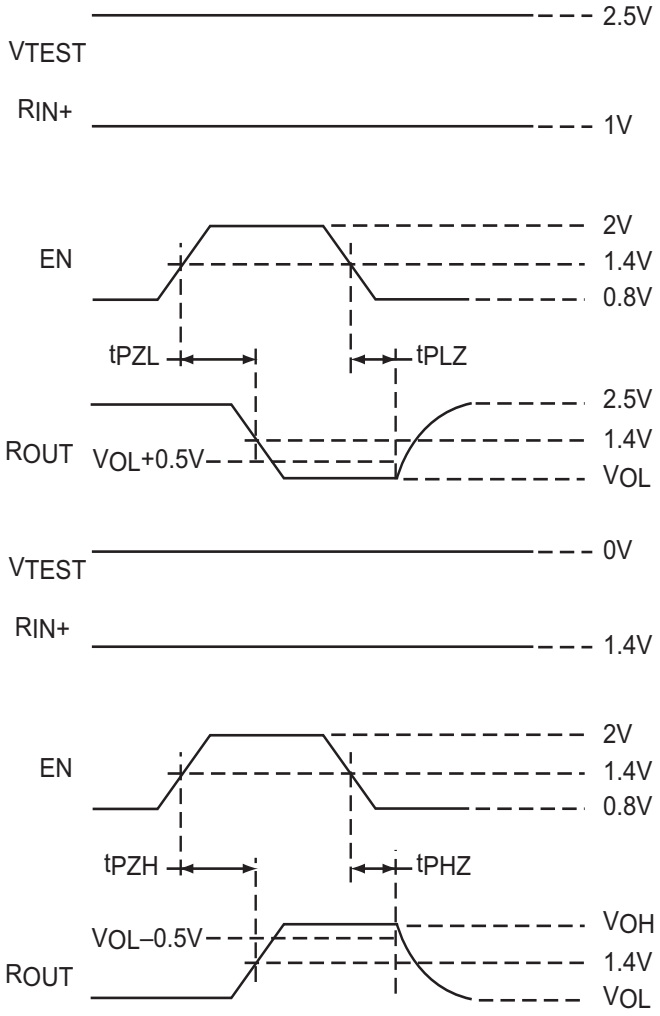
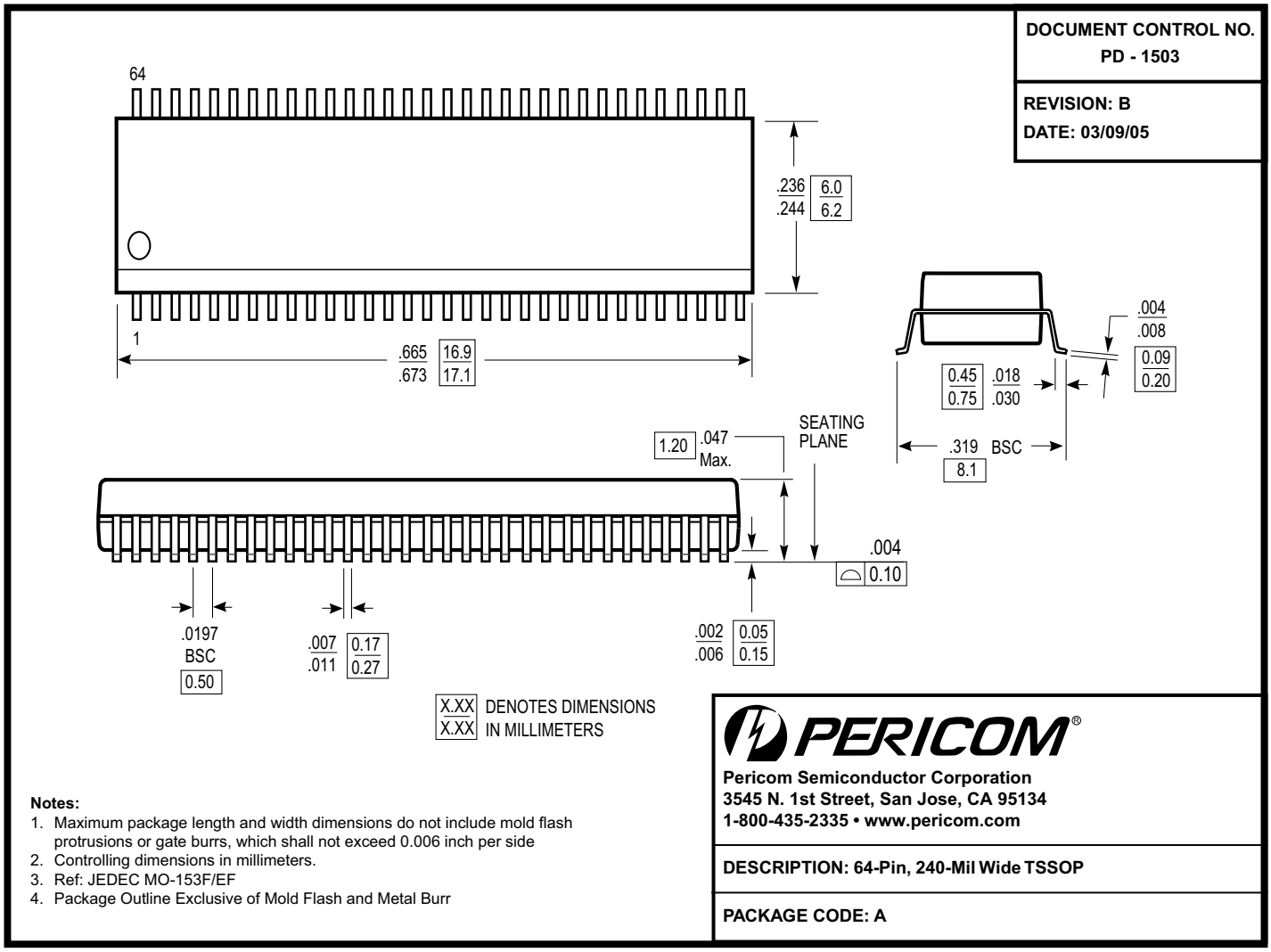


Figure 3. Enable/Disable Test Circuit and Waveforms

Packaging Mechanical: 64-Pin TSSOP (A)



Notes:
1. Maximum package length and width dimensions do not include mold flash protrusions or gate burrs, which shall not exceed 0.006 inch per side
2. Controlling dimensions in millimeters.
3. Ref: JEDEC MO-153F/EF
4. Package Outline Exclusive of Mold Flash and Metal Burr

Ordering Information

Ordering Code	Package Code	Package Type
PI90LV386AE	A	Pb-free & Green, 64-pin TSSOP
PI90LVT386AE	A	Pb-free & Green, 64-pin TSSOP

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. X = Tape and reel