KLI-2104

Linear CCD Image Sensor

Description

The KLI−2104 Image Sensor is a high dynamic range, multi-spectral, linear solid-state image sensor designed for demanding color scanning applications.

The KLI−2104 contains three parallel linear photodiode arrays, each with 2098 active photosites for the detection of red, green, and blue (R, G, B) signals. A fourth channel, comprised of 4,196 pixels, provides high resolution luminance information. This combination allows the KLI−2104 to provide high resolution scans with accurate color reproduction.

The device offers high sensitivity, low noise, and negligible lag.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Quadri-Linear CCD
Total Number of Pixels Chroma Luma	 3 × 2222 1 × 4244
Number of Active Pixels Chroma Luma	 3 × 2098 1 × 4196
Pixel Size Chroma Luma	 14 μm 7 μm
Inter-Array Spacing G to R, R to B B to L	 84 μm 87.5 μm
Active Image Size	29.4 mm (Diagonal)
Chip Size	35.64 mm (H) × 1.06 mm (V)
Saturation Signal Chroma Luma	 208,000 e^- 140,000 e^-
Output Sensitivity	12 μV/e^-
Peak Quantum Efficiency R; G; B; L	 73%; 55%; 62%; 88%
Responsivity R; G; B; L	 33; 36; 56; 16 V/μJ/cm^2
Total Read Noise	30 e^-
Dark Current Chroma Luma	 0.22 pA/Pixel 0.07 pA/Pixel
Dynamic Range Chroma Luma	 80 dB 75 dB
Charge Transfer Efficiency	0.99999
Photoresponse Non-Uniformity	15% Peak-Peak
Operating Frequency	20 MHz per Output
Package	CERDIP
Cover Glass Options	MAR Coated, 2 Sides

NOTE: Parameters above are specified at T = 25°C unless otherwise noted.

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Figure 1. KLI−2104 Linear CCD Image Sensor

Features

- Quadri-Linear Color Array Design (G, R, B, L) for High Resolution with Accurate Color Reproduction
- High Sensitivity Photosites
- Low Noise Design with Negligible Image Lag
- Pixel-Summing Support for Extended Sensitivity and Dynamic Range
- 5.0 V Clock Inputs with Two-Phase Register Clocking
- Choice of Multi-Layer Anti-Reflective Coated (MAR) or Clear Coverglass

Applications

- Digitization
- Photography

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION − KLI−2104 IMAGE SENSOR

Part Number	Description	Marking Code
KLI−2104−DAA−EB−AA	Color (RGB), No Microlens, CERDIP Package (Leadframe), Clear Cover Glass (No Coatings), Standard Grade	KLI−2104 Lot Number Serial Number
KLI−2104−DAA−EB−AE	Color (RGB), No Microlens, CERDIP Package (Leadframe), Clear Cover Glass (No Coatings), Engineering Grade	
KLI−2104−DAA−ED−AA	Color (RGB), No Microlens, CERDIP Package (Leadframe), Clear Cover Glass with AR Coating (Both Sides), Standard Grade	
KLI−2104−DAA−ED−AE	Color (RGB), No Microlens, CERDIP Package (Leadframe), Clear Cover Glass with AR Coating (Both Sides), Engineering Grade	

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

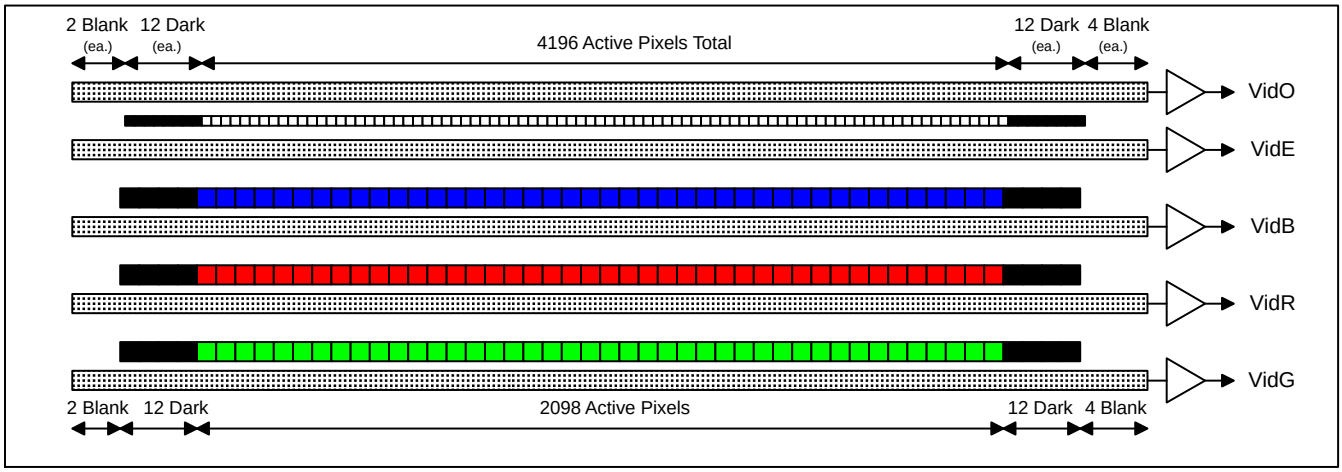
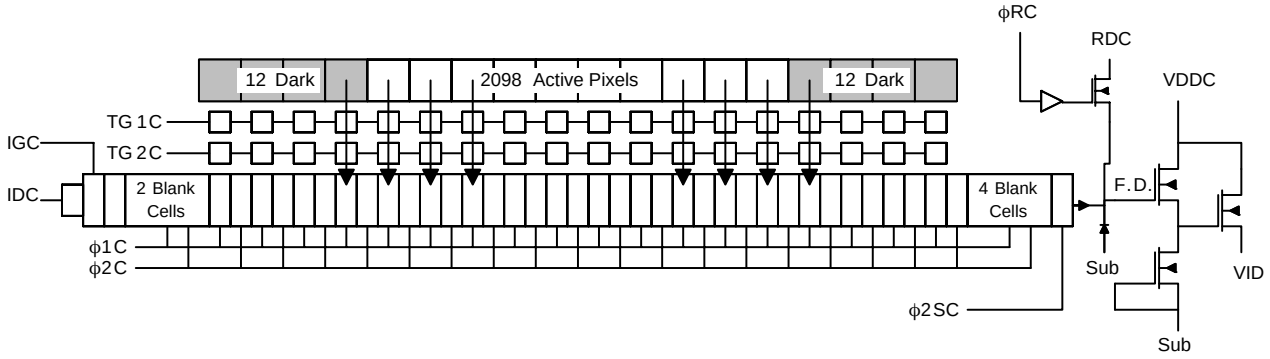


Figure 2. Block Diagram

Chroma Channel Schematic (Not Drawn to Scale)



Luma Channel Schematic (Not Drawn to Scale)

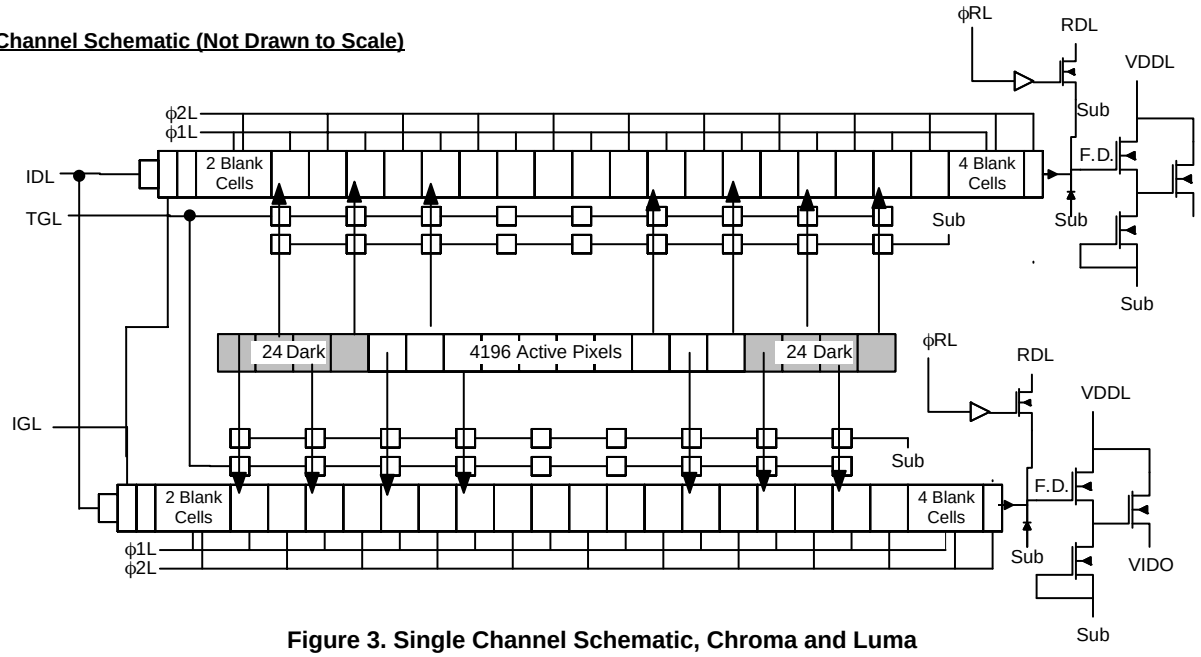


Figure 3. Single Channel Schematic, Chroma and Luma

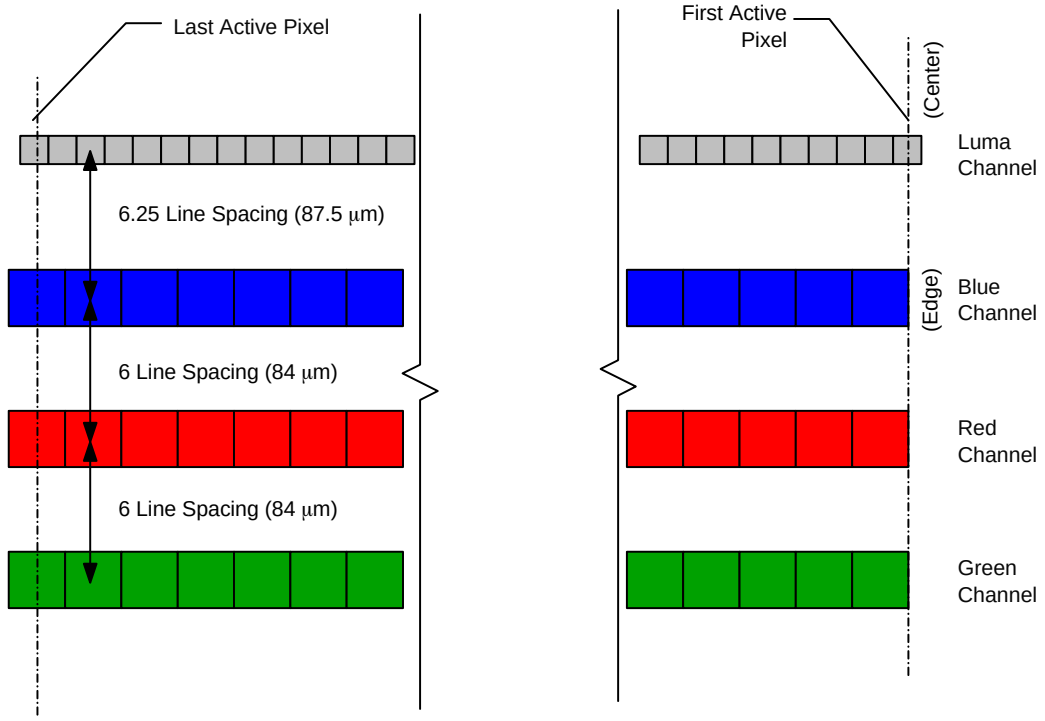


Figure 4. Active Pixel and Channel Alignment − KLI−2104

Imaging

During the integration period, an image is obtained by gathering electrons generated by photons incident upon the photodiodes. The charge collected in the photodiode array is a linear function of the local exposure. The charge is stored in the photodiode itself and is isolated from the CCD shift registers during the integration period by the transfer gates TG1 and TG2 for the chroma channels, which are held at a barrier potential. (The luminance channel has only one transfer gate, TG). At the end of the integration period, the CCD register clocking is stopped with the ϕ1 and ϕ2 gates being held in a ‘high’ and ‘low’ state respectively. Next, the TG gates are turned ‘on’ causing the charge to drain from the photodiode into the TG1 storage region. As TG1 is turned back ‘off’ charge is transferred through TG2 and into the ϕ1 storage region. The TG2 gate is then turned ‘off’, isolating the shift registers from the accumulation region once again. For the luminance channel, only one TG transfer is required. Complementary clocking of the ϕ1 and ϕ2 phases now resumes for readout of the current line of data while the next line of data is integrated.

Charge Transport and Sensing

Readout of the signal charge is accomplished by two-phase, complementary clocking of the ϕ1 and ϕ2 gates. The register architecture has been designed for high speed clocking with minimal transport and output signal degradation, while still maintaining low (5 Vp-p min) clock swings for reduced power dissipation, lower clock noise and simpler driver design. The data in all registers is clocked simultaneously toward the output structures. The signal is then transferred to the output structures in a parallel format at the falling edge of the ϕ2 clock. Re-settable floating diffusions are used for the charge-to-voltage conversion while source followers provide buffering to external connections. The potential change on the floating diffusion is dependent on the amount of signal charge and is given by $\Delta V_{FD} = \Delta Q/C_{FD}$, where ΔV_{FD} is the change in potential on the floating diffusion, ΔQ is the amount of charge, and C_{FD} is the capacitance of the floating diffusion node. Prior to each pixel output, the floating diffusion is returned to the RD level by the reset clock, ϕR.

Pixel Summing (Chroma Channels Only)

Enabling the pixel − summing feature can vary the effective resolution of the color channels of this sensor. A separate pin is provided for the last shift register gate labeled ϕ2SC. This gate, when clocked appropriately, stores the summation of signal from adjacent pixels. This combined charge packet is then transferred onto the sense node. As an example, the sensor can be operated in 2-pixel summing mode (1,049 pixels), by supplying a clock to ϕ2SC which is a 75% duty cycle signal at 1/2 the frequency of the ϕ2C signal, and modifying the ϕRC clock as depicted in Figure 25. Applications that require full resolution mode (2,098 pixels), must tie the ϕ2SC pin to the ϕ2C pin. Refer to Figure 24 for additional details.

The luma channel outputs are in an odd and even configuration. The odd pixel value and the even pixel value are available simultaneously during the ϕ2 clock low phase. In this manner, pixel summing is an option off-chip.

Physical Description

Pin Description and Device Orientation

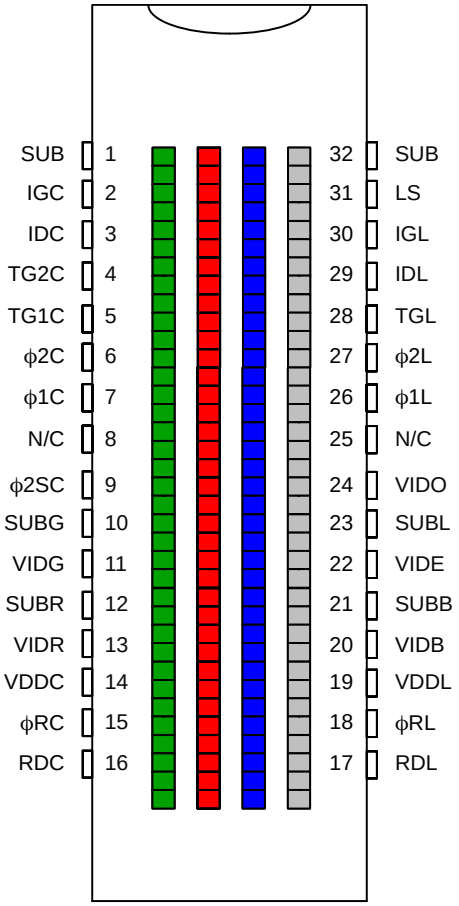


Figure 5. Pinout Diagram

Table 3. PACKAGE PIN DESCRIPTION

Pin	Name	Description
1	SUB	Substrate/Ground
2	IGC	Test Input − Input Diode, Chroma
3	IDC	Test Input − Input Diode, Chroma
4	TG2C	Transfer Gate 2 Clock, Chroma
5	TG1C	Transfer Gate 1 Clock, Chroma
6	ϕ2C	Phase 2 CCD Clock, Chroma
7	ϕ1C	Phase 1 CCD Clock, Chroma
8	N/C	No Connection (Ground)
9	H2SC	Phase 2 Summing Gate, Chroma
10	SUBx	Ground Reference (R, G, B)
11	VIDx	Output Video (R, G, B)
12	SUBx	Ground Reference (R, G, B)
13	VIDx	Output Video (R, G, B)
14	VDDC	Amplifier Supply (Chroma)
15	ϕRC	Reset Clock, Chroma
16	RDC	Reset Drain, Chroma

Pin	Name	Description
17	RDL	Reset Drain, Luma
18	ϕRL	Reset Clock, Luma
19	VDDL	Amplifier Supply (Luma)
20	VIDx	Output Video (R, G, B)
21	SUBx	Ground Reference (R, G, B)
22	VIDE	Output Video (Luma Even Channel)
23	SUBL	Ground Reference (Luma)
24	VIDO	Output Video (Luma Odd Channel)
25	N/C	No Connection (Ground)
26	ϕ1L	Phase 1 CCD Clock, Luma
27	ϕ2L	Phase 2 CCD Clock, Luma
28	TGL	Transfer Gate Clock, Luma
29	IDL	Test Input − Input Diode, Luma
30	IGL	Test Input − Input Gate, Luma
31	LS	Light Shield/Exposure Drain
32	SUB	Substrate/Ground

IMAGING PERFORMANCE

Specifications given under nominally specified operating conditions for the given mode of operation at 25°C, f_{CLK} = 1 MHz, 2.1 ms integration time, MAR cover glass, color filters, and an active load as in the schematic shown in Figure 23 of a typical output bias/buffer circuit, unless otherwise specified. See notes on next page for further descriptions.

Each limit identified as a maximum and/or a minimum is tested and guaranteed for every device. Nominal values are to be considered typical performance values that are design and manufacturing targets. These values are not guaranteed.

Table 4. SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Verification Plan[15]
Saturation Output Voltage, Chroma	V_{SAT}, Chroma	2.0	2.5	−	Vp-p	1, 9	Die
Saturation Output Voltage, Luminance	V_{SAT}, Luma	1.2	1.75	−	Vp-p	1, 9	Die
Output Sensitivity	$\Delta V_{OUT}/\Delta N_e$	−	12	−	$\mu V/e^-$		Design
Saturation Signal Charge, Chroma	Ne,sat chroma	−	208,000	−	e^-		Design
Saturation Signal Charge, Luminance	$N_{e,SAT}$ Luma	−	146,000	−	e^-		Design
Responsivity	R, Chroma					2, 9, 10	
Quantum Efficiency Blue Channel @ 460 nm Green Channel @ 540 nm Red Channel @ 650 nm Luma Channel @ 550 nm	QE, Chroma QE, Luma	 − − − −	 73 55 62 88	 − − − −	%	2, 9, 10 ±10% ±10% ±10% ±10%	Design
Dynamic Range Chroma Luma	 DR, Chroma DR, Luma	 − −	 80 75	 − −	dB	3	Design
Dark Noise, Chroma and Luma	Noise, Dark	−	30	−	e^-		Design
Dark Signal Non-Uniformity, Chroma Luma	 DSNU, Chroma DSNU, Luma	 − −	 2 2	 16 16	mV p-p	14	Die
Dark Current Chroma Luma	 I_{DARK}, Chroma I_{DARK}, Luma	 − −	 0.22 0.07	 0.5 0.2	pA/Pixel	4	Die
Charge Transfer Efficiency Chroma Luma	 CTE, Chroma CTE, Luma	 0.999995 0.999995	 0.999998 0.999998	 1 1	−	5	Die
Lag Chroma Luma	 L, Chroma L, Luma	 − −	 0.05 0.1	 1 1	%	1st Field	Die
DC Output Offset	V_{ODC}	5	6.6	8	V	9	Die
Photoresponse Non-Uniformity, Low Frequency, Chroma	PRNUC, Low	−	6	20	% p-p	6	Die
Photoresponse Non-Uniformity, Medium Frequency, Chroma	PRNUC, Med	−	6	20	% p-p	7	Die
Photoresponse Non-Uniformity, High Frequency, Chroma	PRNUC, High	−	3	15	%	8	Die
Photoresponse Non-Uniformity, Low Frequency, Luma	PRNUL, Low	−	6	20	% p-p	6	Die
Photoresponse Non-Uniformity, Medium Frequency, Luma	PRNUL, Med	−	6	20	% p-p	7	Die
Photoresponse Non-Uniformity, High Frequency, Luma	PRNUL, High	−	3	15	%	8	Die
Darkfield Defect, Brightpoint	Dark Def	−	−	0	Allowed	12	Die

Table 4. SPECIFICATIONS (continued)

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Verification Plan[15]
Brightfield Defect, Dark or Bright	Bfld Def	−	−	0	Allowed	13	Die
Smear, Photodiode to CCD Crosstalk Blue Channel @ 450 nm Green Channel @ 550 nm Red Channel @ 650 nm	Smear, Chroma	 − − −	 0.2 0.05 0.4	 − − −	%		Design
Smear Luma channel @ 550 nm	Smear, Luma	 −	 1.2	 −	%		Design
Linearity, Maximum from Best Fit Straight Line Blue Channel Green Channel Red Channel Luma Channel	Linearity, Chroma Linearity, Luma	 − − − −	 0.6 1.2 1 1	 − − − −	%		Design
DC Amplifier Gain	Gain, DC	−	0.75	−			Design
Amplifier Output Resistance	R_{OUT}	−	220	−	Ω		Design
Output Buffer Bandwidth	f_{-3dB}	−	72	−	MHz		Design

1. Calculated under a flat field illumination. Defined as the maximum output level achievable before linearity or PRNU performance is degraded beyond specification.
2. With color filter. Values specified at filter peaks. 50% bandwidth = ±30 nm. Color filter arrays become transparent after 710 nm. It is recommended that a suitable IR cut filter be used to maintain spectral balance and optimal MTF. See quantum efficiency plots in Figure 7.
3. This device utilizes 2-phase clocking for cancellation of driver displacement currents. Symmetry between $\phi 1$ and $\phi 2$ phases must be maintained to minimize clock noise.
4. Dark current doubles approximately every +7°C.
5. Measured per transfer, 2 phases per pixel. For the typical total line (Chroma): $(0.99999)^{4256} = 0.9583$. For the typical total line (Luma): $(0.99999)^{4256} = 0.9583$. It should be noted that this parameter degrades with increasing horizontal clock frequency.
6. Low frequency response is measured across the entire array with a 1,000 pixel-moving window and a 5 pixel median filter evaluated under a flat field illumination.
7. Medium frequency response is measured across the entire array with a 50 pixel-moving window and a 5 pixel median filter evaluated under a flat field illumination.
8. High frequency response non-uniformity represents individual pixel defects evaluated under a flat field illumination. An individual pixel value may deviate above or below the average response for the entire array by a certain threshold.
9. Increasing the current load (nominally 6 mA) to improve signal bandwidth will decrease these parameters.
10. If resistive loads are used to set current, the amplifier gain will be reduced, thereby reducing the output sensitivity and net responsivity.
11. Where defective pixels are allowed, they will be separated by at least one non-defective pixel within and across channels.
12. Pixels whose response is greater than the average response by the specified threshold, (16 mV). See Figure 6.
13. Pixels, whose response is greater or less than the average response by the specified threshold, contained in the high frequency PRNU specification for that channel. See Figure 6.
14. Absolute difference between the maximum and minimum average signal level for an entire video channel.
15. A “die” parameter is measured on every sensor during production testing. A “design” parameter is quantified during design verification and not guaranteed by specification.

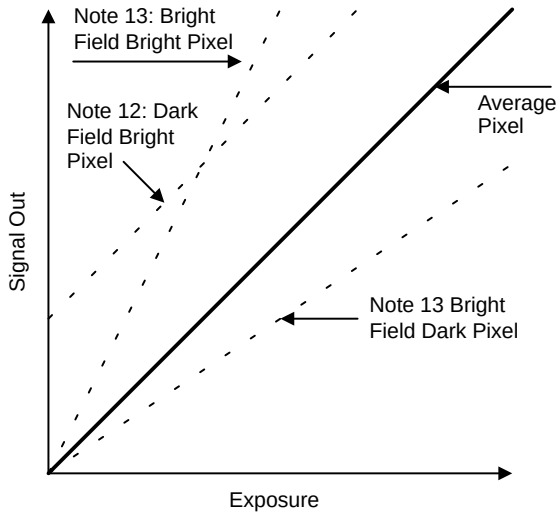


Figure 6. Defective Pixel Classification

TYPICAL PERFORMANCE MEASURES

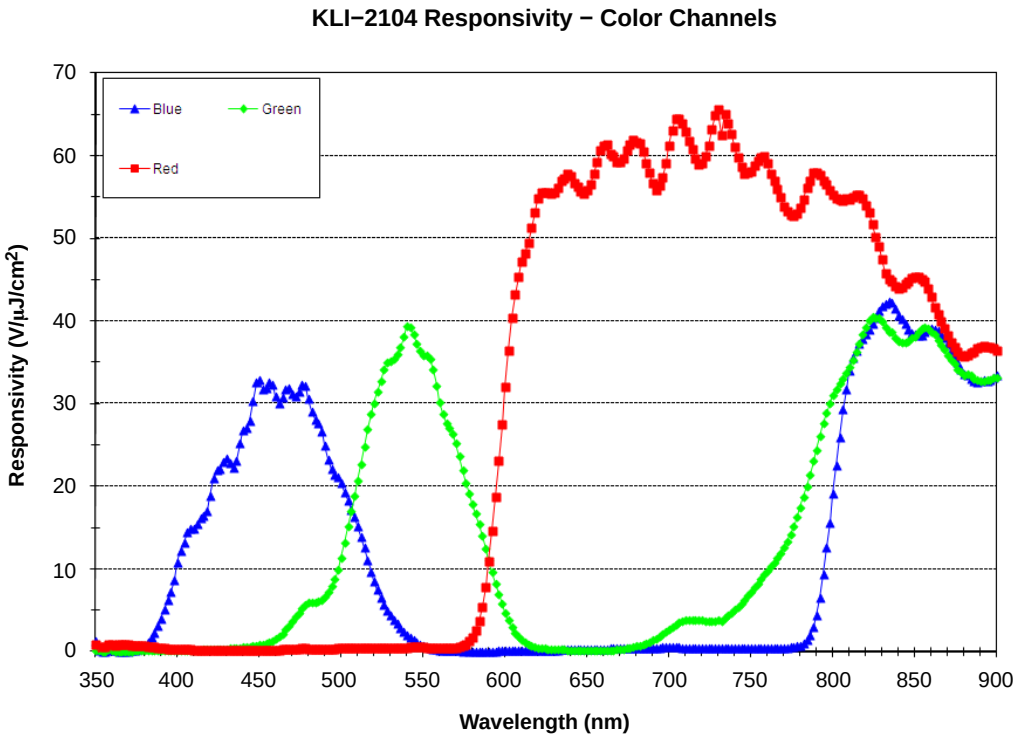


Figure 7. KLI−2104 Responsivity − Color Channels

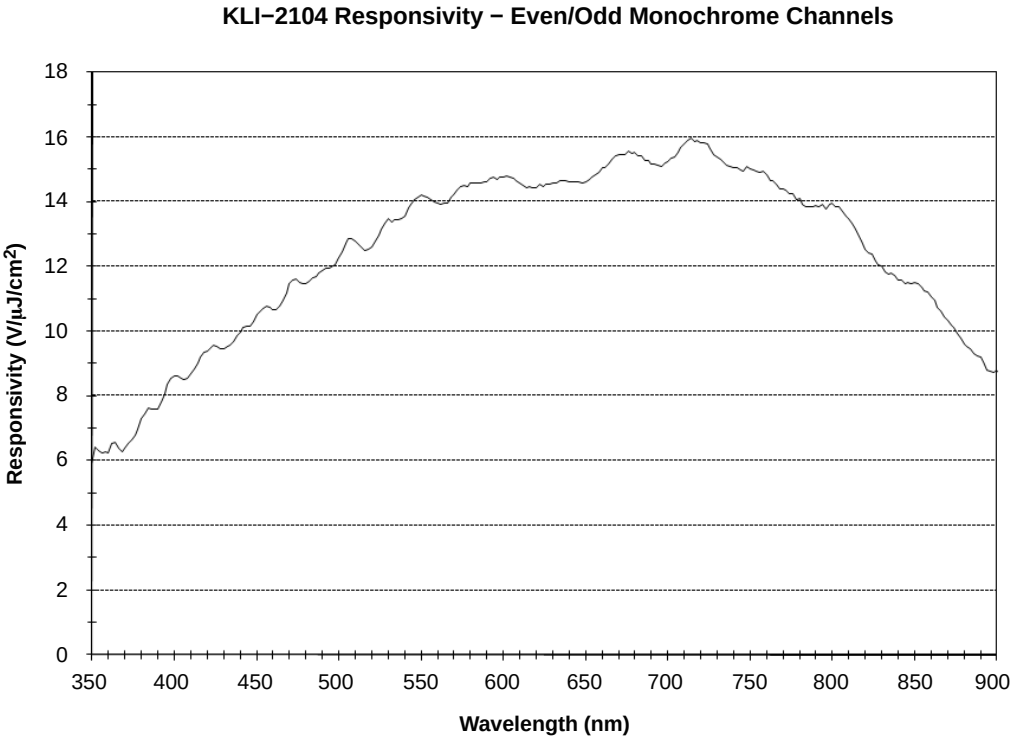


Figure 8. Luminance Channel Responsivity

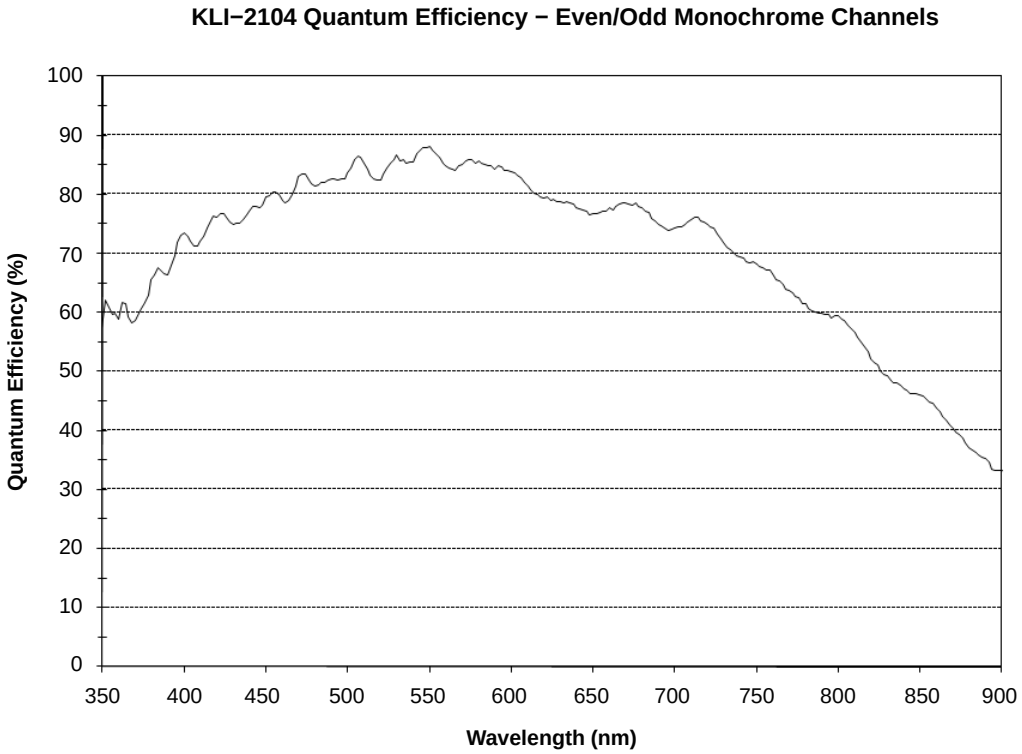


Figure 9. KLI−2104 Quantum Efficiency − Even/Odd Monochrome Channels

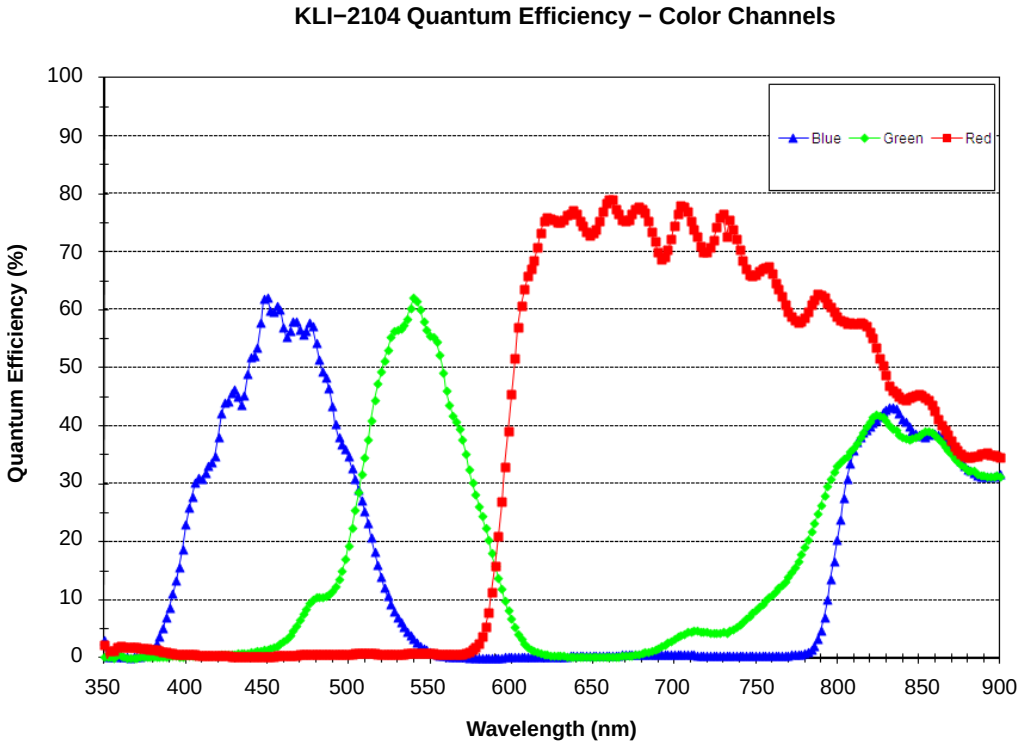


Figure 10. KLI−2104 Quantum Efficiency − Color Channels

RED Channel Linearity, Typical Response − Red LED Illumination

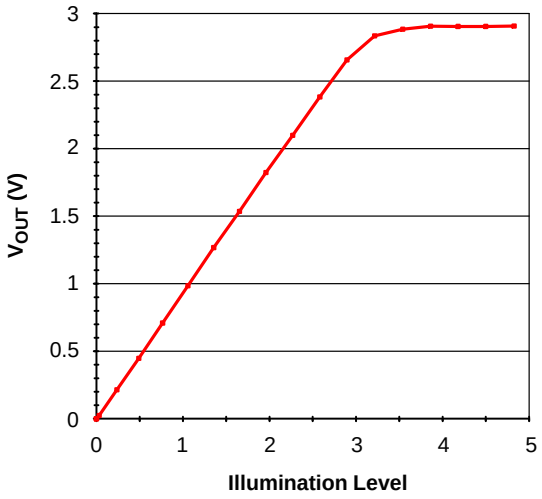


Figure 11. Red Channel Linearity

GREEN Channel Linearity, Typical Response − Green LED Illumination

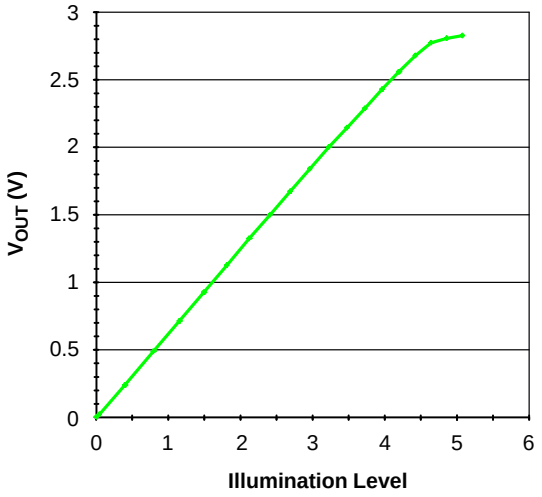


Figure 12. Green Channel Linearity

BLUE Channel Linearity, Typical Response − Blue LED Illumination

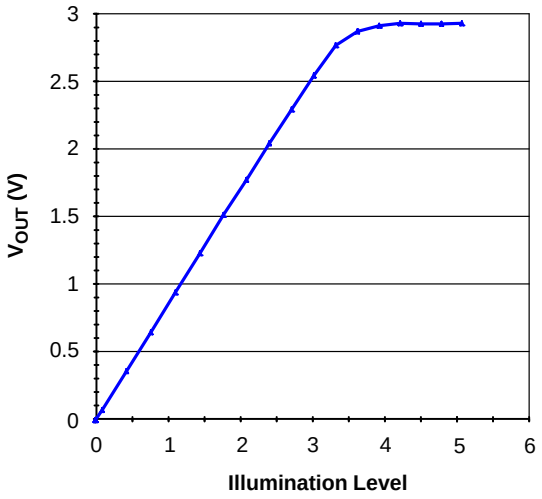


Figure 13. Blue Channel Linearity

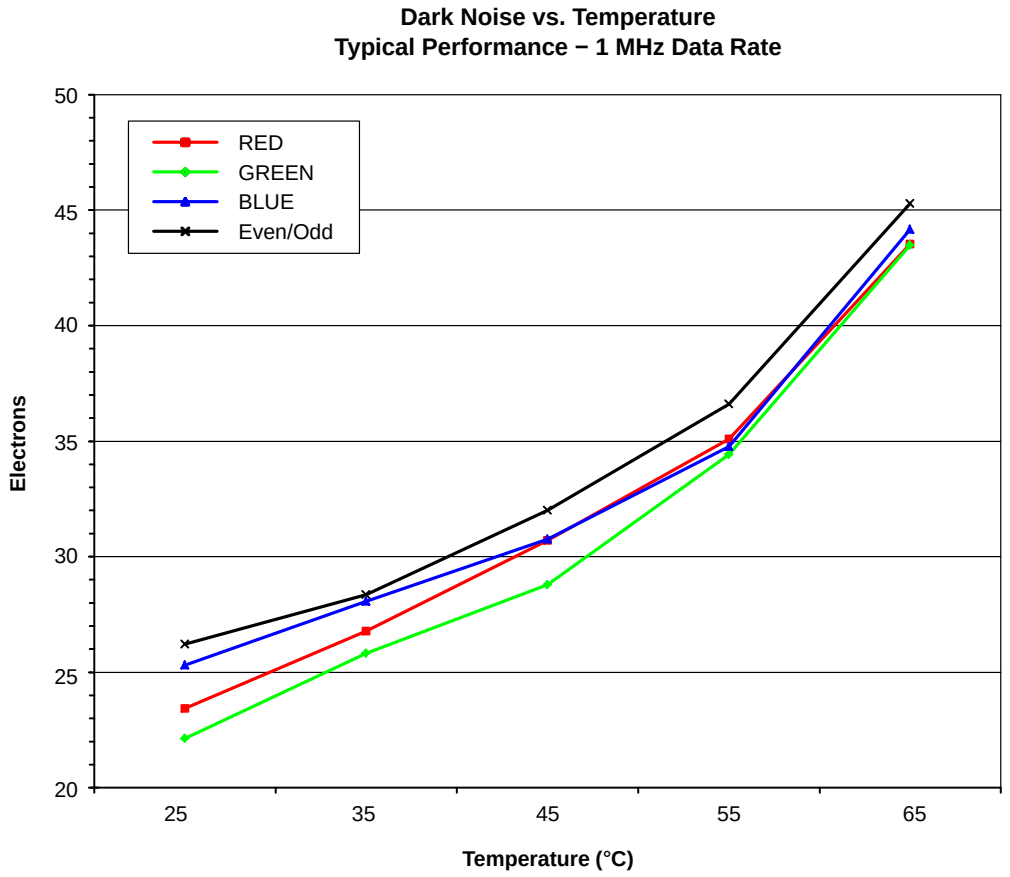


Figure 14. Dark Noise vs. Temperature

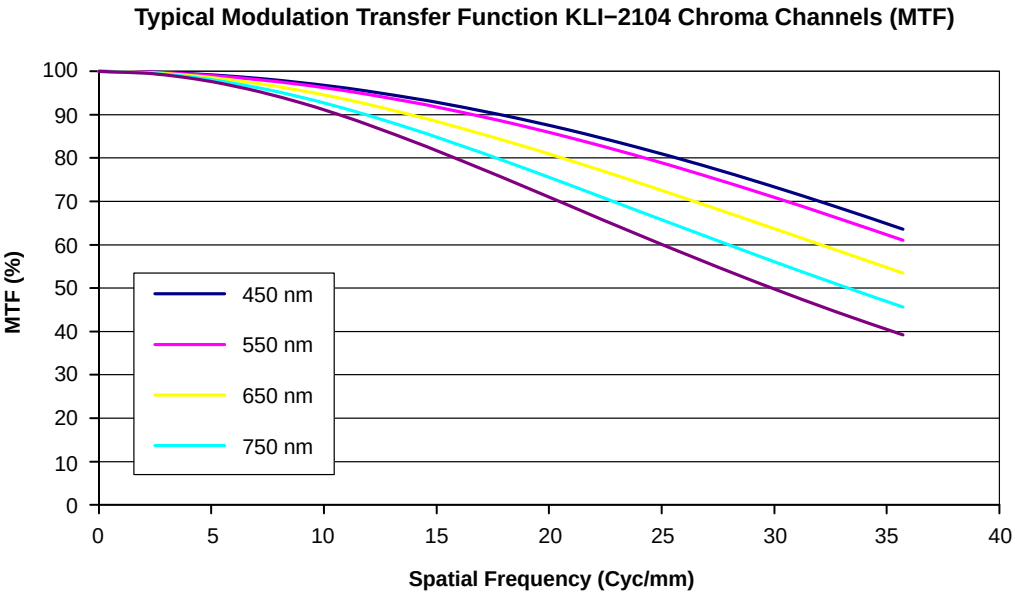


Figure 15. Typical Modulation Transfer

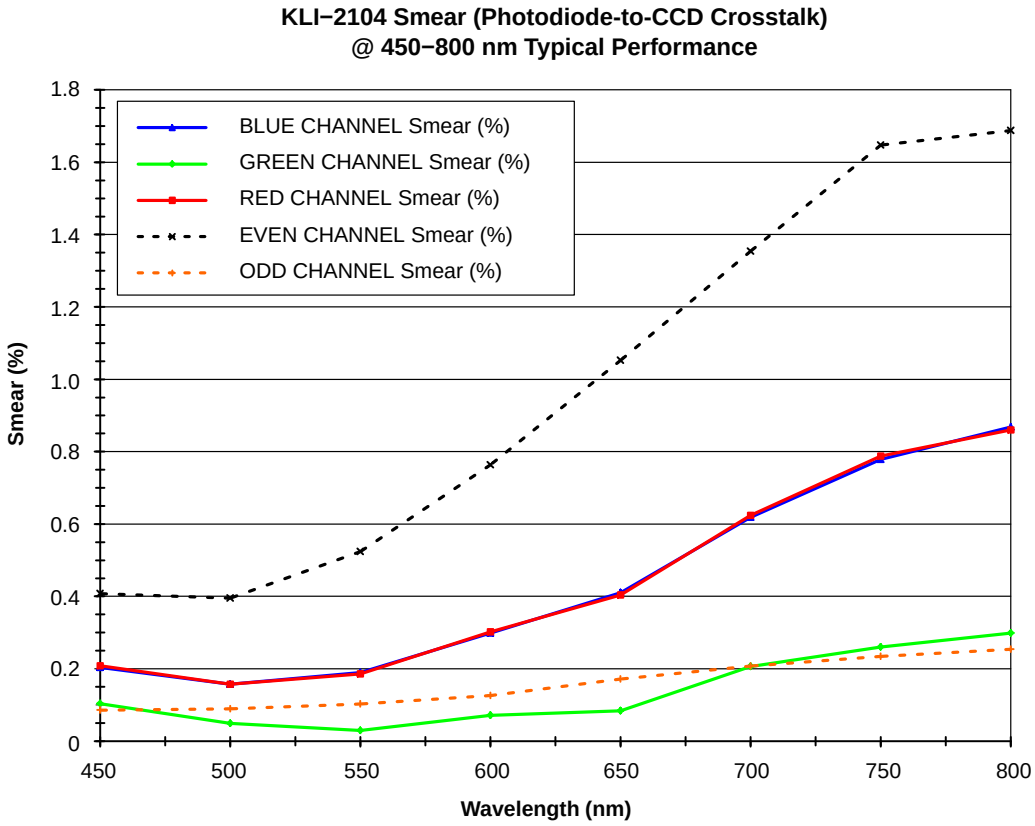


Figure 16. KLI−2104 Smear

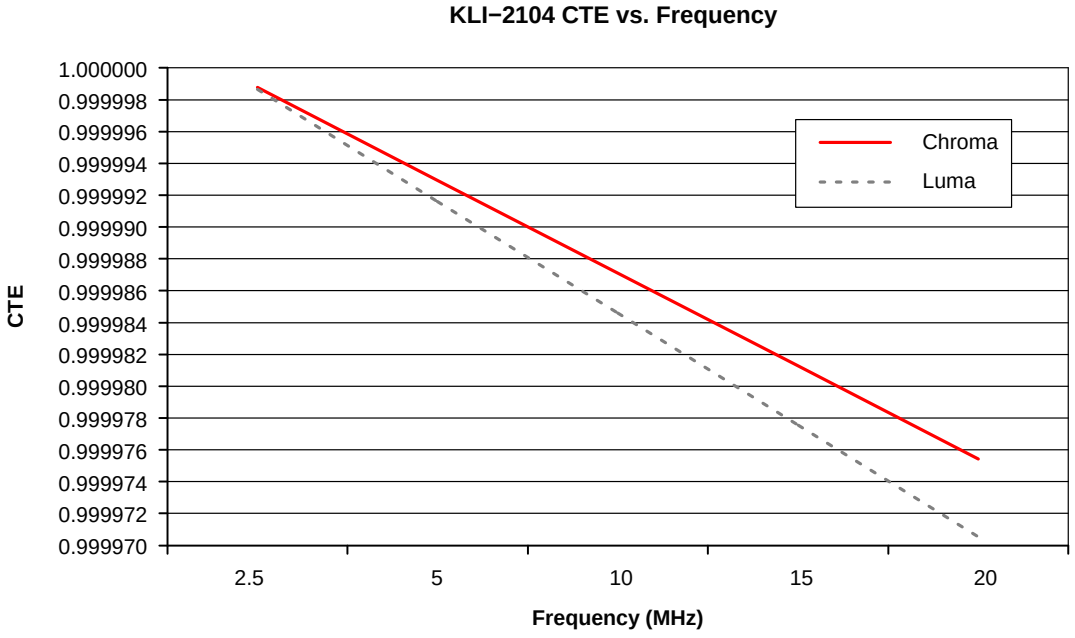


Figure 17. CTE vs. Frequency

Typical KLI−2104 Dark Noise vs. CCD Clock Frequency

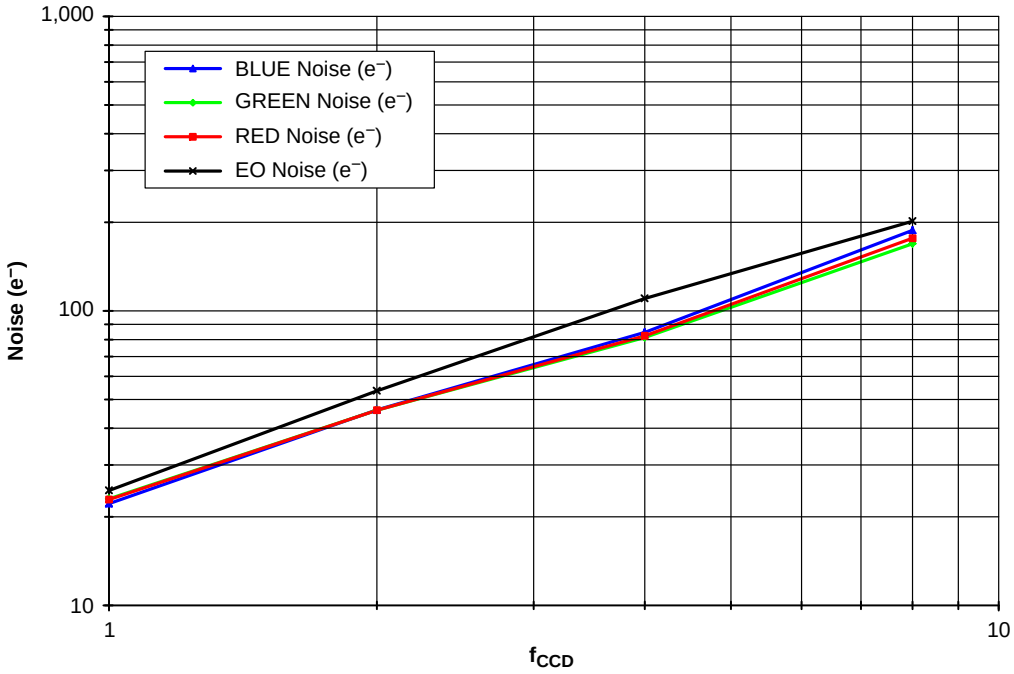


Figure 18. Typical KLI−2104 Dark Noise vs. CCD Clock Frequency

Typical KLI−2104 Dark Noise vs. CCD Clock Frequency

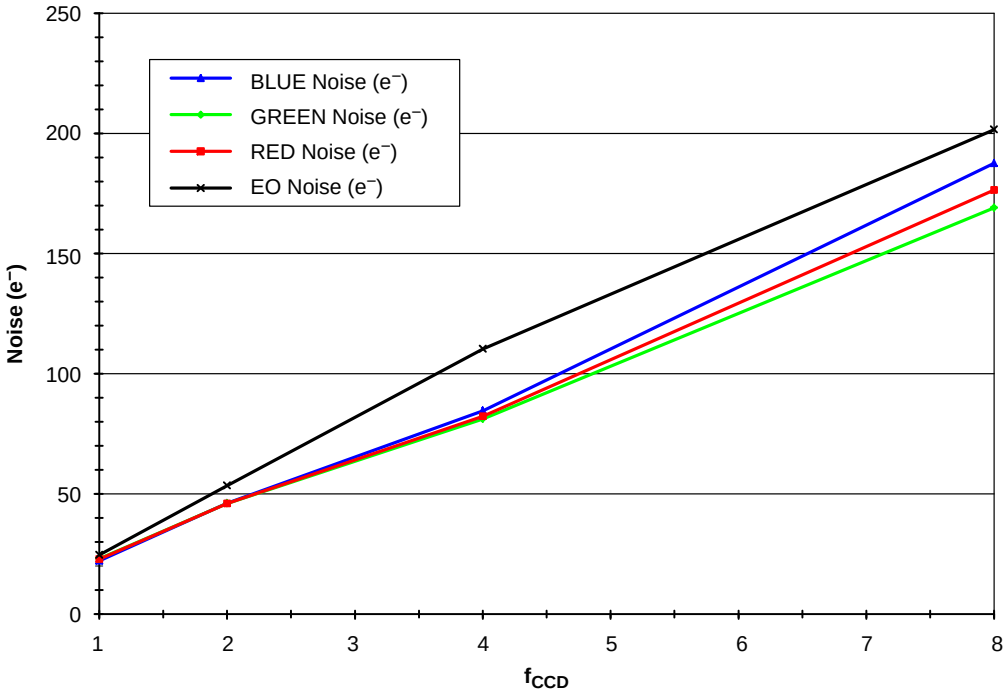


Figure 19. Typical KLI−2104 Dark Noise vs. CCD Clock Frequency

Typical KLI−2104 Noise vs. Temperature
(1 MHz)

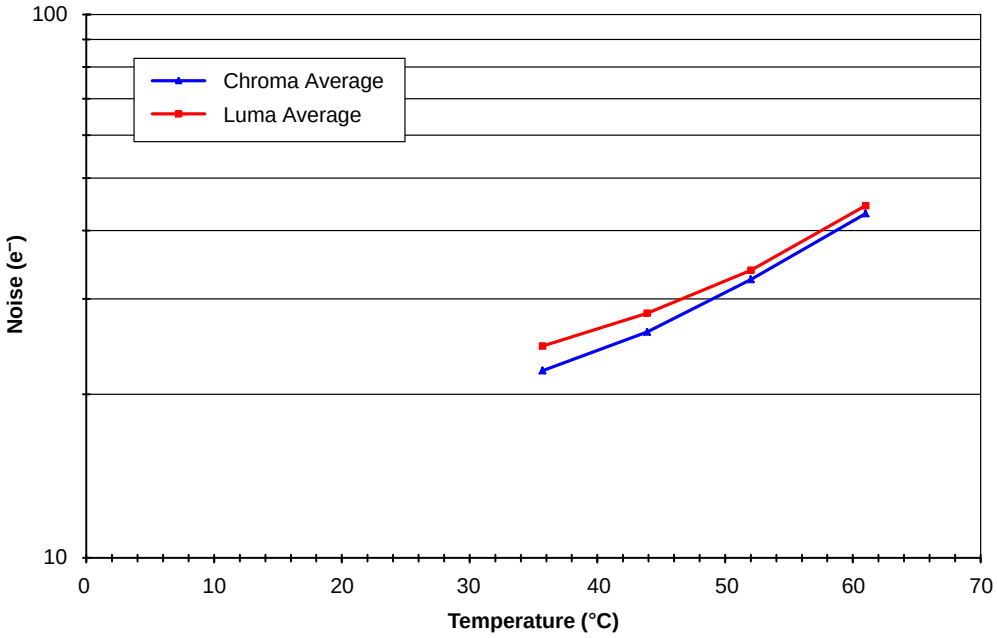


Figure 20. Noise vs. Temperature

Typical KLI−2104 Dark Voltage vs. Temperature
(1 MHz/t_{INT} = 2.2 ms)

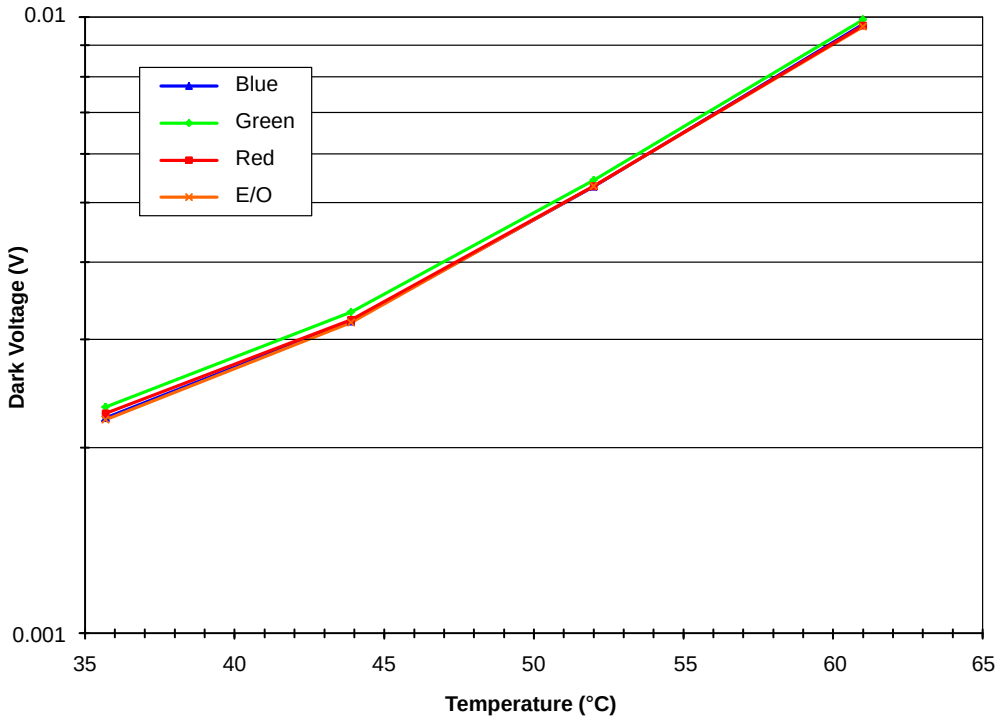


Figure 21. Dark Voltage vs. Temperature

OPERATION

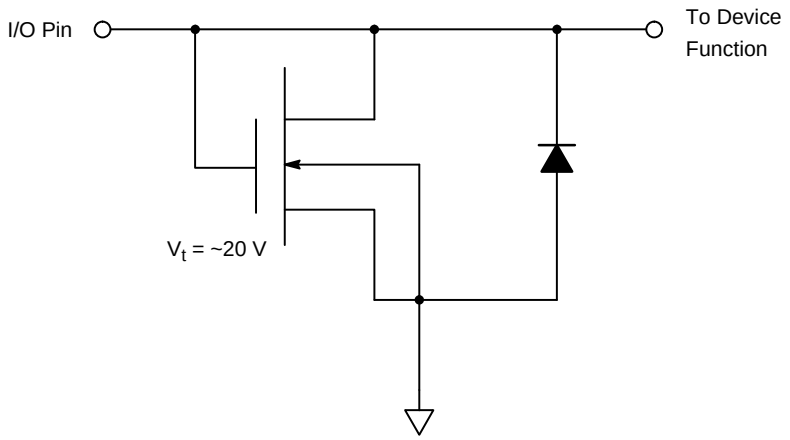
Table 5. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Gate Pin Voltage	V_{GATE}	0	16	V	1, 2
Pin-to-Pin Voltage	$V_{PIN-PIN}$	−	16	V	1, 3
Diode Pin Voltages	V_{DIODE}	−0.5	16	V	1, 4
Output Bias Current	I_{DD}	−10	−1	mA	5
Output Load Capacitance	$C_{VID,LOAD}$	−	10	pF	9
CCD Clocking Frequency	f_{CLK}	−	20	MHz	6
Operating Temperature	T_{OP}	0	70	°C	7
Storage Temperature	T_{ST}	−25	80	°C	8

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Referenced to substrate voltage.
2. Includes pins: H1n, H2n, TGx, ϕRx, OGx, IGx.
3. Voltage difference (either polarity) between any two pins.
4. Includes pins: VIDn, VSSn, RDx, VDDx, LS and IDx.
5. Care must be taken not to short output pins to ground during operation as this may cause permanent damage to the output structures.
6. Charge transfer efficiency will degrade at frequencies higher than the maximum clocking frequency. VIDn load resistor values may need to be decreased as well.
7. Noise performance will degrade with increasing temperatures.
8. Long term storage at the maximum temperature will accelerate color filter degradation.
9. Exceeding the upper limit on output load capacitance will greatly reduce the output frequency response. Thus, direct probing of the output pins with conventional oscilloscope probes is not recommended.
10. The absolute maximum ratings for the entire table indicate the limits of this device beyond which damage may occur. The Operating ratings indicate the conditions that the device is functional. Operating at or near these ratings do not guarantee specific performance limits. Guaranteed specifications and test conditions are contained in the Imaging Performance section.

Device Input ESD Protection Circuit (Schematic)



CAUTION: To allow for maximum performance, this device was designed with limited input protection; thus, it is sensitive to electrostatic induced damage. These devices should be installed in accordance with strict ESD handling procedures!

Figure 22. ESD Protection Circuit

DC Bias Operating Conditions

Table 6. DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Substrate	$V_{SUB\ C,L}$	−	0	−	V	
Reset Drain Bias (Color)	$V_{RD\ C,L}$	11.5	12.0	12.5	V	
Output Buffer Supply	$V_{DD\ C,L}$	11.5	12.0	12.5	V	
Output Bias Current/Channel	I_{VIDPIN}	−4.0	−6.0	−8.0	mA	1
Light Shield/Drain Bias	V_{LS}	11.5	12.0	12.5	V	
Test Pin − Input Gate	$V_{IG\ C,L}$	−	0	−	V	
Test Pin − Input Diode	$V_{ID\ C,L}$	−	12.0	−	V	

1. A current sink must be supplied for each output. Load capacitance should be minimized so as not to limit bandwidth. The values of R_X and R_L should be chosen to optimize for a given operating frequency, but. Rx should not be less than 75 Ω. The values shown in Figure 23 below represent one possible solution.

Typical Output Bias/Buffer Circuit

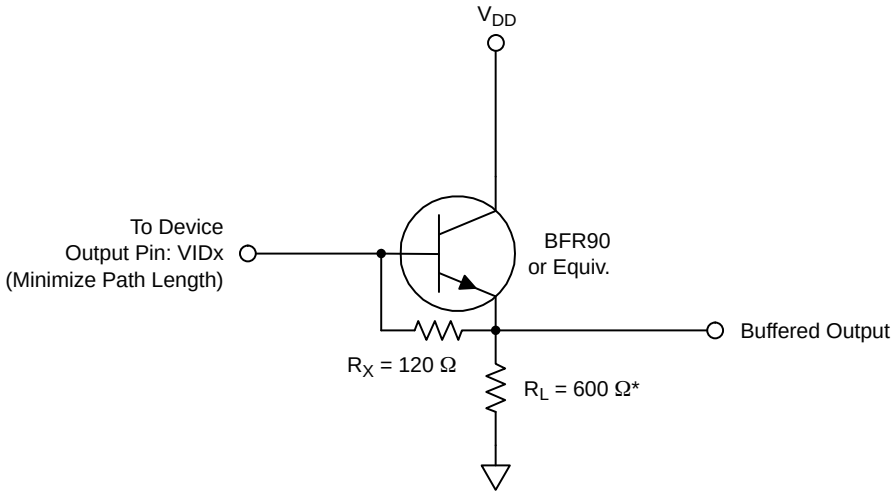


Figure 23. Typical Output Bias/Buffer Circuit

AC Operating Conditions

Table 7. AC ELECTRICAL CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
CCD Element Duration	$1e = 1/f_{CLK}$	50	50	−	ns	1 e Count
ϕ1L, ϕ1C, ϕ2L, ϕC2, Rise Time	t_R	−	30	−	ns	Typical
Line/Integration Period	$1L = t_{INT}$	0.1064	2.128	−	ms	2128 e Counts
PD−CCD Transfer Period	t_{PD}	1,000	−	−	ns	8 e Counts
Transfer Gate 1 Clear	t_{TG1}	500	1,000	−	ns	1 e Count
Transfer Gate 2 Clear	t_{TG2}	500	1,000	−	ns	1 e Count
Reset Pulse Duration	t_{RST}	9	−	−	ns	1
Clamp to ϕ2 Delay	t_{CD}	5	−	−	ns	2
Sample to Reset Edge Delay	t_{SD}	5	−	−	ns	2
LOG Gate Duration	t_{LOG1}	1,000	−	−	ns	
LOG Gate Clear	t_{LOG2}	1,000	−	−	ns	

1. Minimum values given are for 20 MHz CCD operation.
2. Recommended delays for Correlated Double Sampling (CDS) of output.

Table 8. CLOCK LEVELS

Description	Symbol	Minimum	Nominal	Maximum	Units
CCD Readout Clocks High	$V_{\phi 1CH}$, $V_{\phi 2CH}$, $V_{\phi 1LH}$, $V_{\phi 2LH}$	4.6	5.0	−	V
CCD Readout Clocks Low	$V_{\phi 1CL}$, $V_{\phi 2CL}$, $V_{\phi 1LL}$, $V_{\phi 2LL}$	−0.1	0.0	0.1	V
Transfer Clocks High	V_{TGLH}, V_{TG1H}, V_{TG2H}	4.6	5.0	−	V
Transfer Clocks Low	V_{TGLL}, V_{TG1L}, V_{TG2L}	−0.1	0.0	0.1	V
Reset Clock High	$V_{\phi RCH}$, $V_{\phi RLH}$	4.6	5.0	−	V
Reset Clock Low	$V_{\phi RCL}$, $V_{\phi RLL}$	−0.1	0.0	0.1	V

1. Care should be taken to insure that low rail overshoot does not exceed −0.5 VDC. Exceeding this value may result in non-photogenerated charged being injected into the video signal.
2. Connect pin to ground potential for applications where exposure control is not required.

TIMING

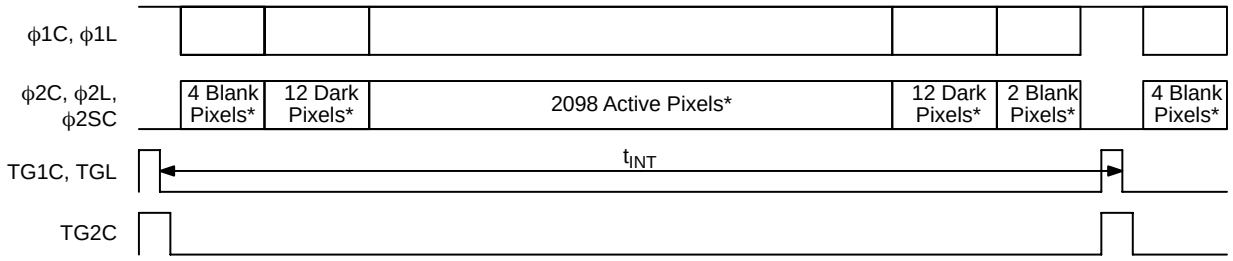
Requirements and Characteristics

Table 9. CLOCK LINE CAPACITANCE

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
CHROMA						
Phase 1 Clock Capacitance	$C_{\phi 1C}$	−	758	−	pF	1
Phase 2 Clock Capacitance	$C_{\phi 2C}$	−	558	−	pF	1
Transfer Gate 1 Capacitance	C_{TG1C}	−	440	−	pF	
Transfer Gate 2 Capacitance	C_{TG2C}	−	222	−	pF	
Reset Gate Capacitance	$C_{\phi RC}$	−	6	−	pF	
LUMA						
Phase 1 Clock Capacitance	$C_{\phi 1L}$	−	397	−	pF	1
Phase 2 Clock Capacitance	$C_{\phi 2L}$	−	302	−	pF	1
Transfer Gate Capacitance	C_{TGL}	−	92	−	pF	
Reset Gate Capacitance	$C_{\phi RL}$	−	6	−	pF	

1. This is the total load capacitance per CCD phase. Since the CCDs are driven from both ends of the sensor, the effective load capacitance per drive pin is approximately half the value listed.

Line Timing − Full Resolution Mode



* Pixel counts are per output.

Transfer Timing − Full Resolution Mode

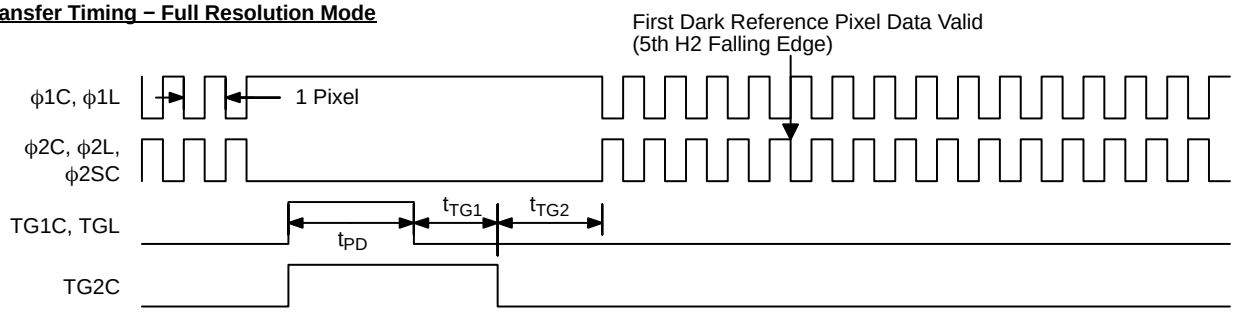
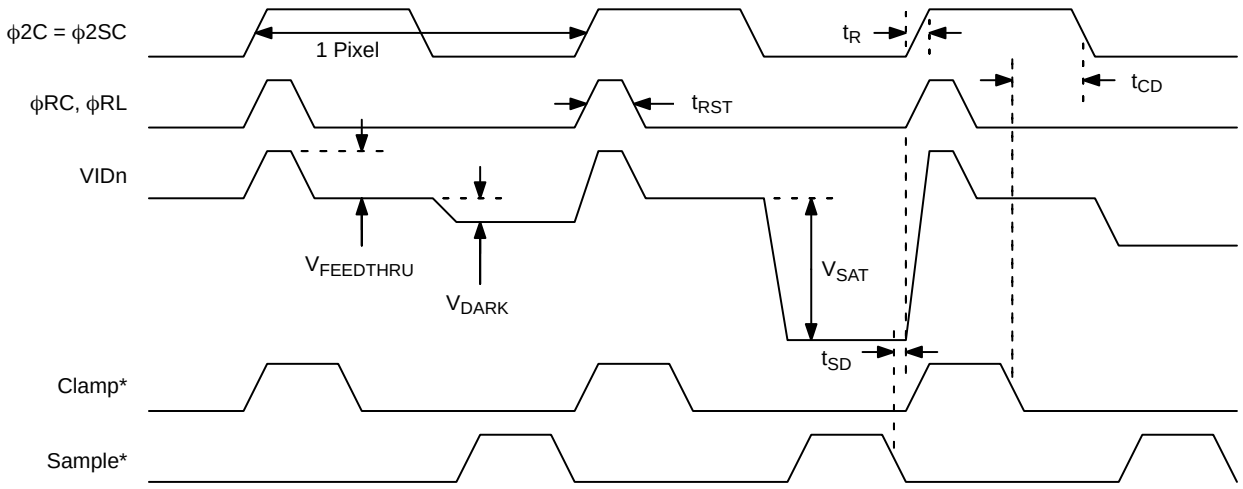
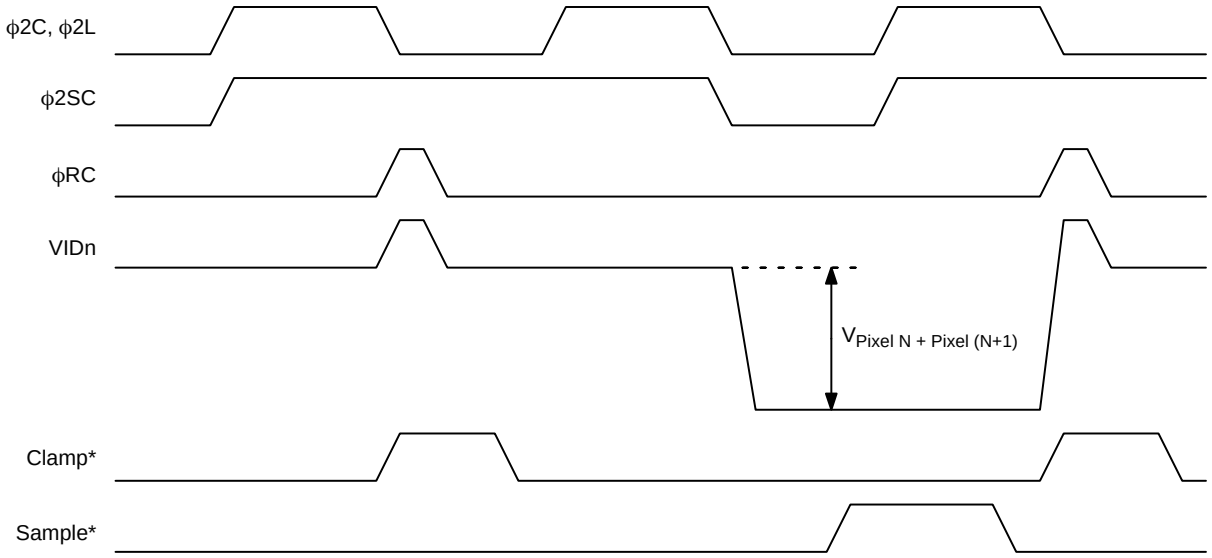


Figure 24. Timing Diagram

Output Timing − Full Resolution Mode



Output Timing − 2-Pixel Summing Mode



* Required for Optional Off-Chip, Analog, Correlated Double Sampling (CDS) Signal Processing.

Figure 25. Output Timing

MECHANICAL DRAWINGS

Completed Assembly

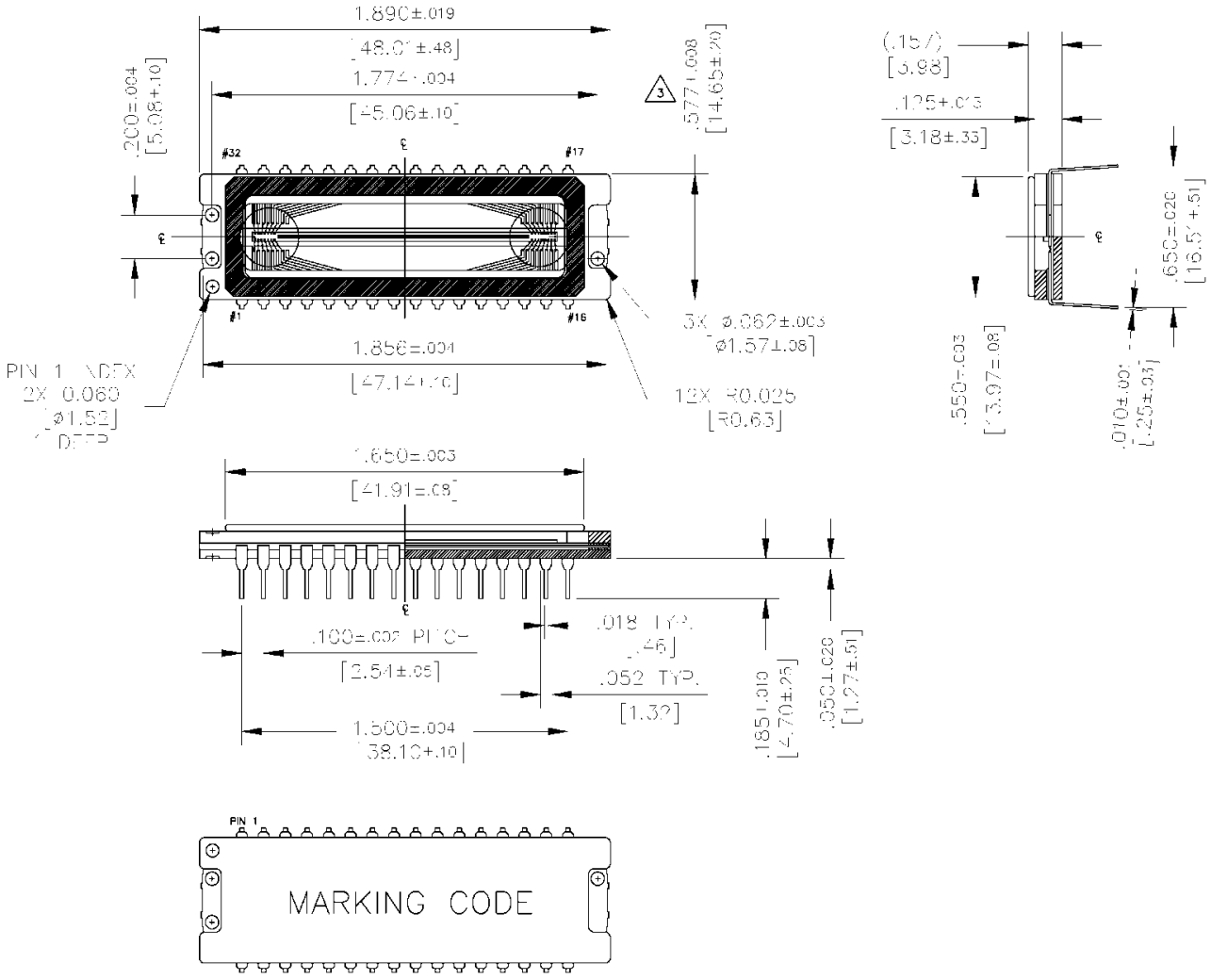


Figure 26. Completed Assembly

COVER GLASS SPECIFICATION

Two-Sided Multi-Layer Anti-Reflective Cover Glass Specification (MAR)

This device is configured with a coverglass designed to reduce reflections and maximize transmission of the visible light. The typical spectral characteristics of this glass is found below:

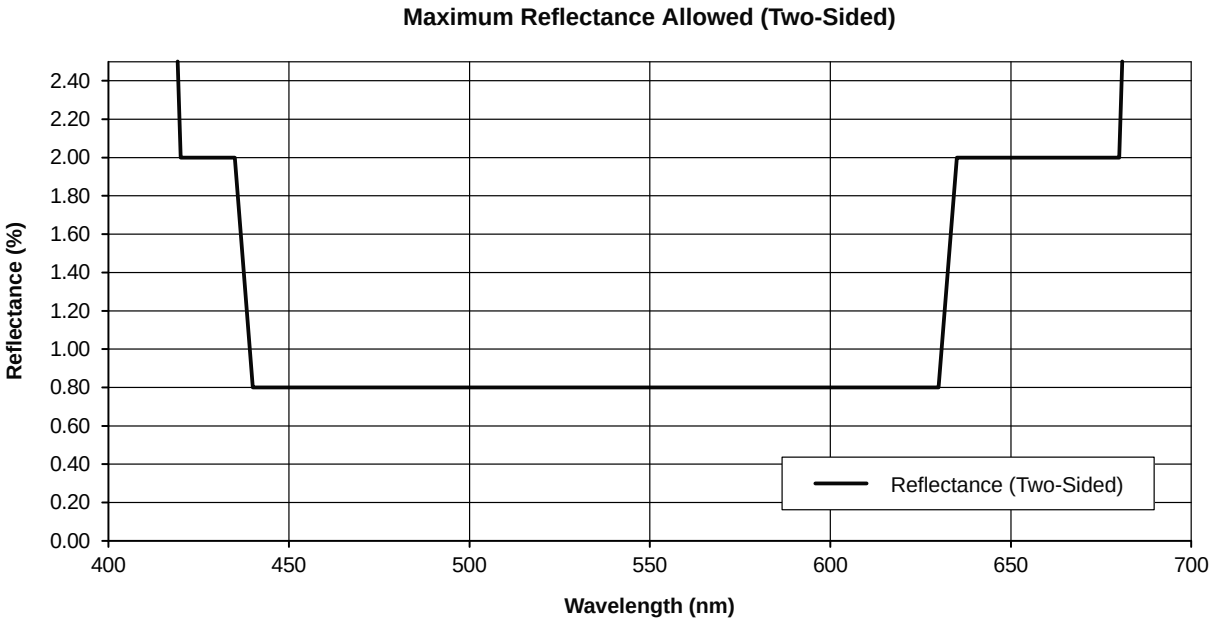


Figure 27. Maximum Reflectance Allowed

REFERENCES

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

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