FURUNO GPS/ GNSS Receiver
Model: GN-86/87, GV-86/87 and GT-86/87 Series

User's Design Guide

(Document No. SE13-900-001-06)

FURUNO ELECTRIC CO., LTD.

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Revision History

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0	Initial release	2013.06.07
1	2nd preliminary release	2013.06.14
2	3rd preliminary release	2013.07.18
3	Formal revision release	2013.12.11
4	Corrected Figure 3-1, 3-2 and 3-6 Updated Chapter 1, Chapter 6 and Contact Information	2014.10.09
5	Corrected the cover	2015.05.26
6	Corrected section 3.5.1	2015.10.30

Table of contents

FURUNO

1   General Description

This document presents the useful design guidance to improve the performance and the quality of our customers' products that contain FURUNO 86/87 series GPS/GNSS receiver modules (86/87 series module) listed as below.

- GN-86F	- GV-86	- GT-86
- GN-87F	- GV-87	- GT-87
- GN-8615	- GV-8615	
- GN-8715	- GV-8715	

Please insure the quality of your own design with the final design guide.

2   RF Section PCB Layout Design

Figure 2-1 shows an overview of the RF section PCB design for using the active antenna.

39nH inductor is placed to bias the active antenna, 33pF capacitor is placed to block the DC voltage, and λ/4 short stub works to bypass ESD noise to the ground.

The line from the antenna connector to RF_IN pin through 33pF capacitor should be designed to have 50Ω characteristic impedance with using the PCB design technique known as microstrip line. Since the input impedance of 86/87 series module is design to be 50Ω, so it is not needed to place 50Ω matching network between the antenna connector through the receiver RF_IN pin.

▬ :Active Antenna Power Supply Line

▬ : 1.5GHz / 1.6GHz 50Ω Microstrip Line

☐ : Ground

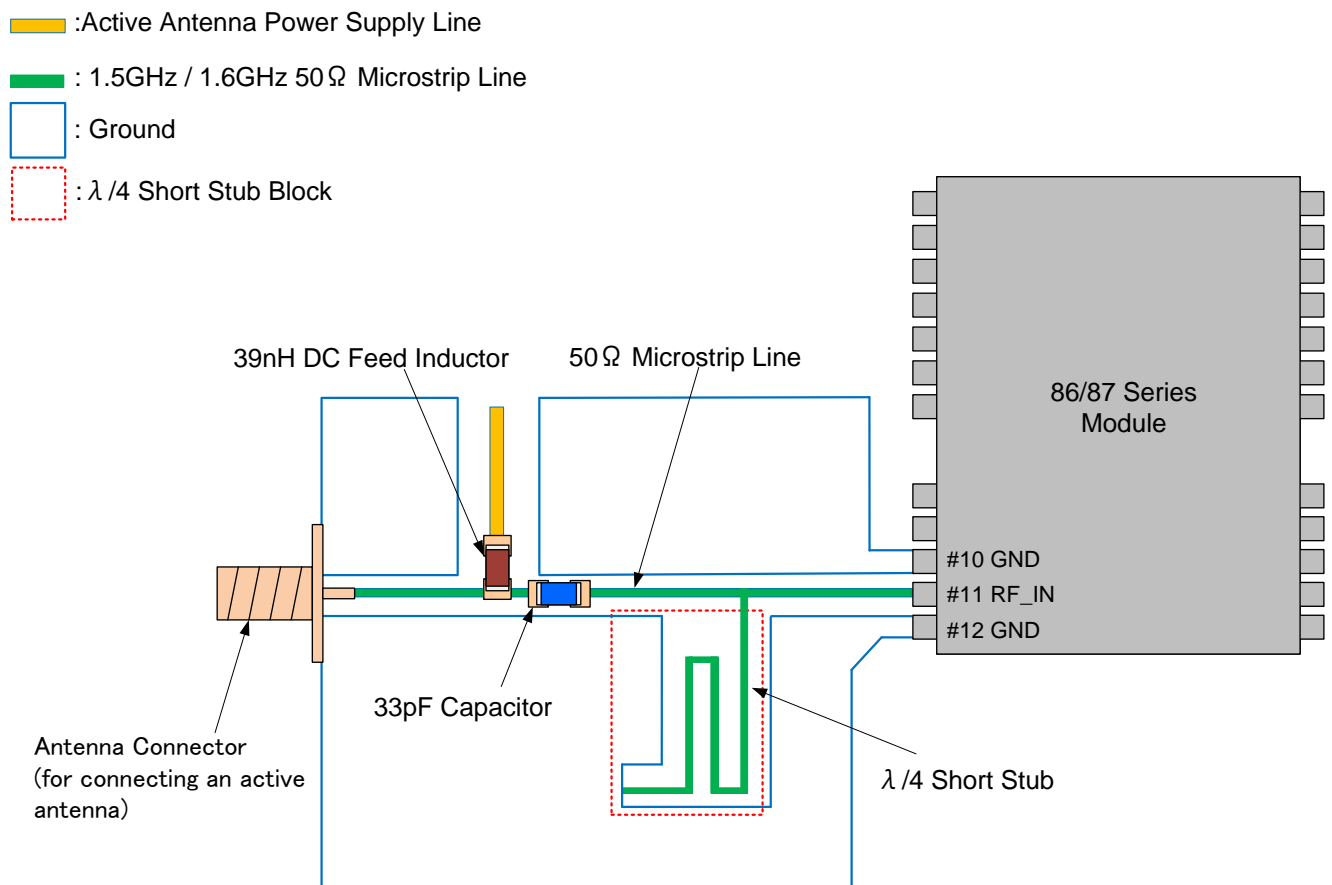⬚ : λ/4 Short Stub Block

Figure 2-1 RF Section PCB Layout Design Overview for Active Antenna

Figure 2-2 shows an overview of the RF section PCB design for using the passive antenna.

There is no need to bias the antenna, so 39nH inductor and 33pF capacitor are removed from Figure 2-1. But λ/4 short stub is placed to keep the higher robustness against ESD noise.

The routing between the passive antenna and RF_IN should be designed as 50Ω microstrip line, and there is no need to place any matching network externally as same as the active antenna case.
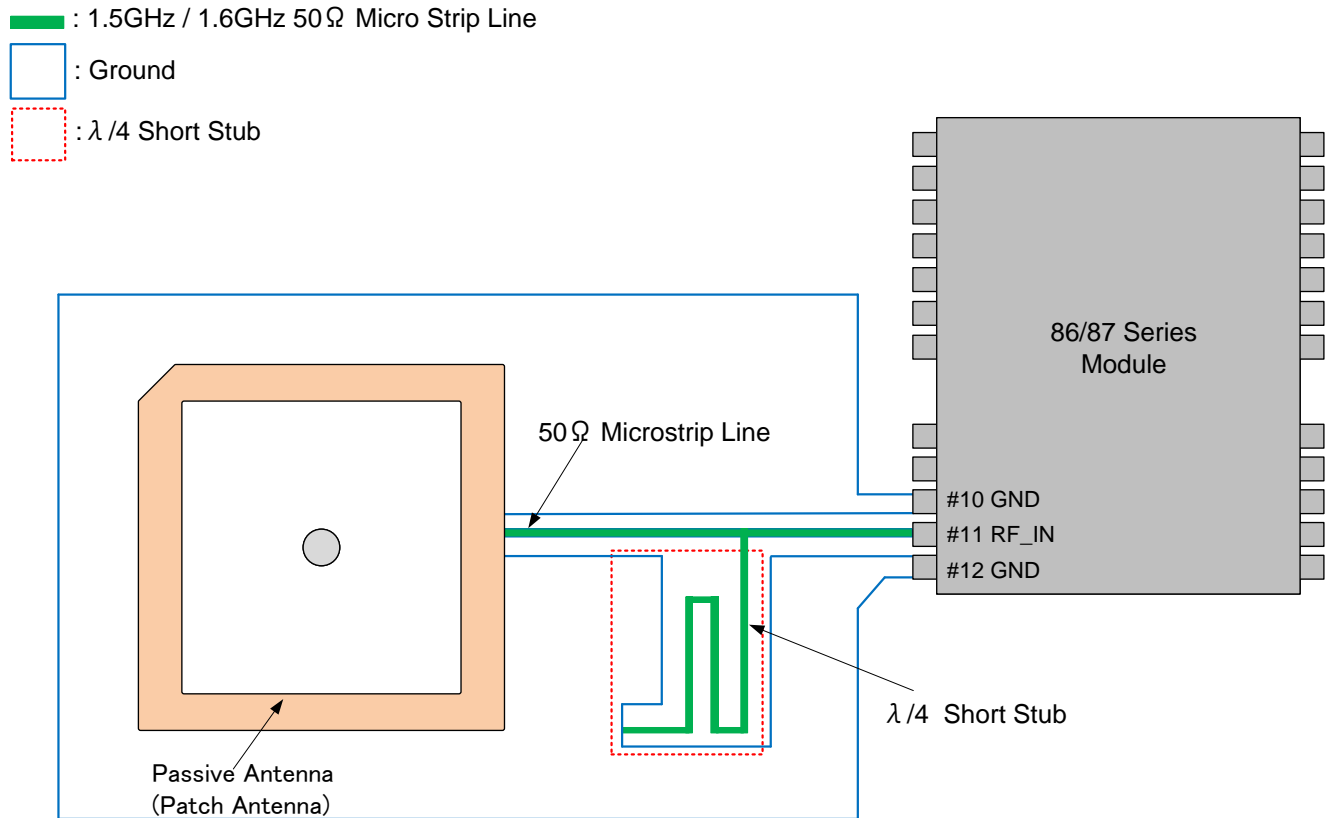
Figure 2-2 RF Section PCB Layout Design Overview for Passive Antenna

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2.1 PCB Ground Layout Design

At the bottom of the module, there are some signal lines and via holes. For avoiding any signal shortage, please do not put any signal line nor via hole at the part of the user's board where is facing to the bottom of the module. This also contributes to reduce noise influence.

If a double-sided board is used, the back side of the RF line should be a ground plane. If a multi-layer board is used, the 2nd layer below the RF line should be a ground plane.

For better noise suppression, the guarding ground plane around the RF signal line is also recommended. Details are described in Section 2.2.
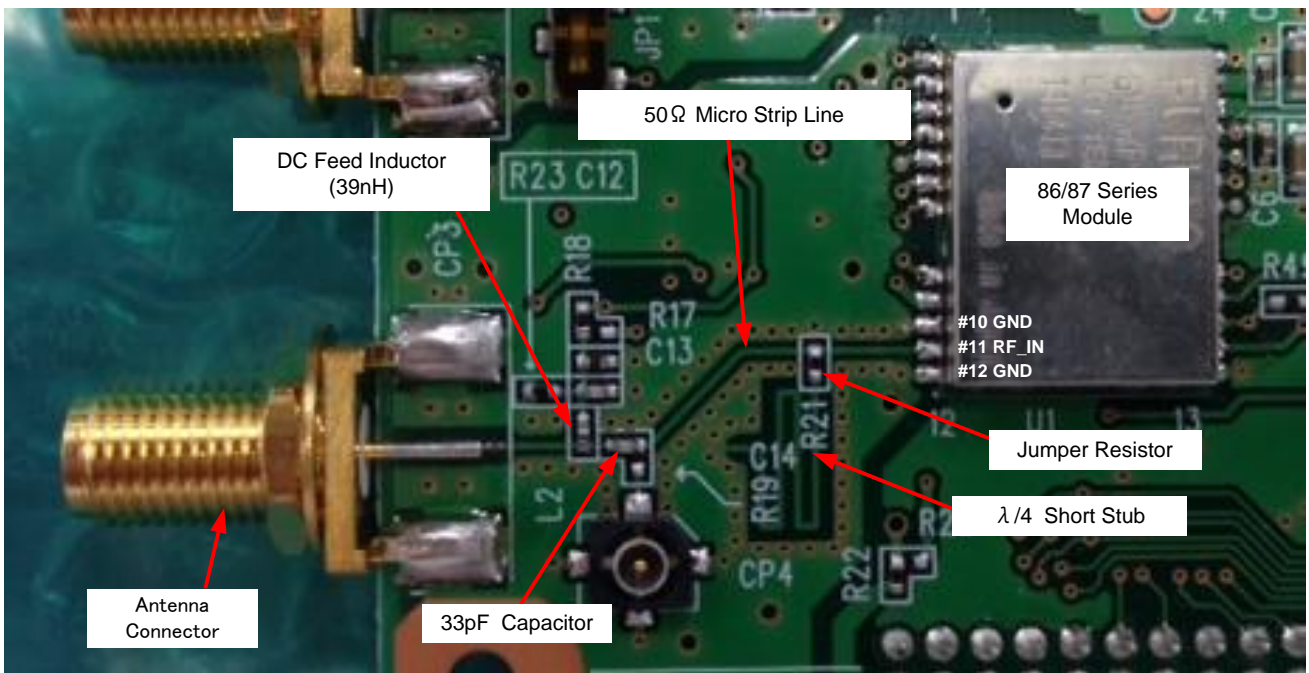

Figure 2-3 An Example of PCB Design around RF Section in Evaluation Kit

2.2 Microstrip Line Design

The PCB design of RF line from the antenna connector to RF_IN pin is very important for keeping the reception sensitivity performance of the receiver module. For achieving the best performance, please follow the design guidelines below.
- Use the microstrip line for RF line to keep 50Ω characteristic impedance.
- Make the length of RF line as short as possible.
- Do not place any digital signal source nor signal line around RF line.
- Use guarding ground plane for decoupling the noise source such as Figure 2-6.

The microstrip line is the most popular technique to obtain 50Ω characteristic impedance line on usual PCB. The basic structure is shown at the bottom-right in Figure 2-4. The conductor part at the upper side is the signal transmission path, and the conductor part at the lower side is ground. The characteristic impedance (Z_c) of microstrip line is determined by the following parameters relevant to the specifications of PCB materials.
- Dielectric constant of PCB: Er
- Distance between signal line and ground: H
- Signal line thickness: Tmet
- Signal line width: W

For the calculation of the characteristic impedance, Microstrip Analysis/Synthesis Calculator[*1] (MASC) is recommended, which is a free software, useful to design the microstrip line onto customer's board. Figure 2-4 shows an example of the calculation result by MASC. For details, please see the web site below.

The transmission loss per length of the microstrip line is determined by the following parameters relevant to the specifications of PCB materials.
- Metal resistivity relative to copper: Rho
- Loss tangent of the dielectric: Tanσ
- Metal surface roughness: Rough

Figure 2-4 also contains the calculation result of the transmission loss by MASC.

Note: (*1) Microstrip Analysis/Synthesis Calculator (Copyright (c) 1994-2003, 2010 Dan McMahill All rights reserved). See URL below.
http://mcalc.sourceforge.net/,

Analysis/Synthesis Values

Width	0.31	--->	Z0 (Ohms)	50.18
Length	23.5	<---	Elec. Len. (degrees)	78.77
Frequency	1589		MHz	

Output Values

Keff	3.0862		Loss (dB)	0.181
Physical Units	mm		Loss per length (dB/{Phys. Unit})	7.7E-3
Calculation Status	DONE		Skin depth {Phys. Units}	0.002
DeltaL {Phys. Units}	0.071		Delay (ns)	0.138
Len.-DeltaL {Phys. Units}	23.429			

Substrate Parameters

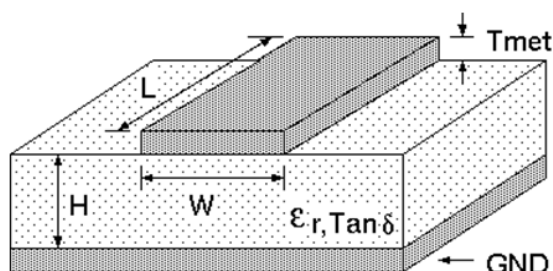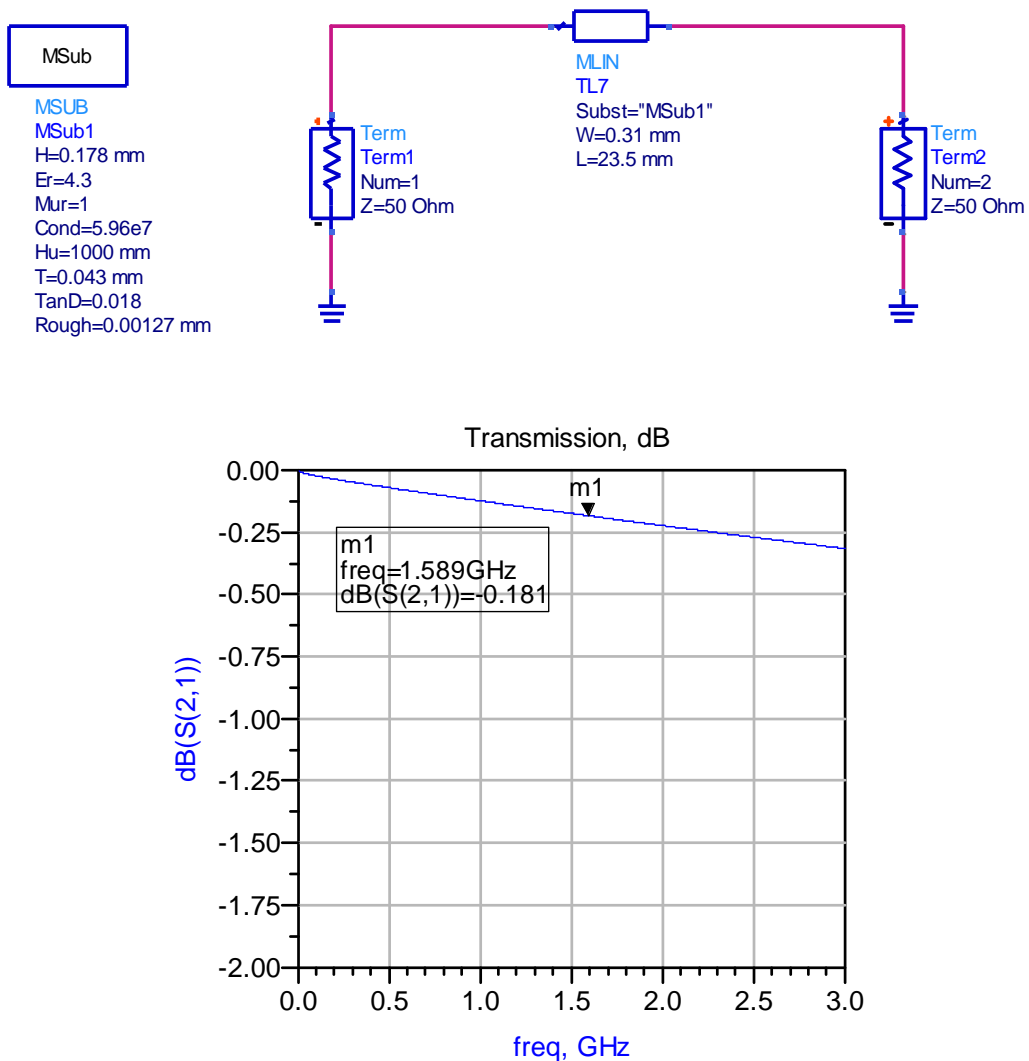| Er	4.3	Rho	1
H	0.178	Rough	0.00127
Tmet	0.043	Tanδ	0.018

Figure 2-4 An Example of Microstrip Line Design by MASC

Figure 2-5 shows Transmission Loss-Frequency characteristics of the microstrip line shown in Figure 2-4. It is simulated by Agilent ADS[TM].

MSub

MSUB
MSub1
H=0.178 mm
Er=4.3
Mur=1
Cond=5.96e7
Hu=1000 mm
T=0.043 mm
TanD=0.018
Rough=0.00127 mm

MLIN
TL7
Subst="MSub1"
W=0.31 mm
L=23.5 mm

Term
Term1
Num=1
Z=50 Ohm

Term
Term2
Num=2
Z=50 Ohm

Transmission, dB

m1
freq=1.589GHz
dB(S(2,1))=-0.181

Figure 2-5 Simulation Result on Transmission Loss-Frequency Characteristics of the Microstrip line by Agilent ADS[TM]

Usually the microstrip line is routed at the surface layer of the PCB, and it is not protected from the radio interference. So sometimes the interference causes the degradation of the receiver performance. In such case, the guarding ground plane can improve the performance with decoupling the interference noise source. The guarding ground plane is the ground placed around the microstrip line as shown in Figure 2-6. The important thing for designing and layouting the guarding ground plane is to keep the gap between the microstrip line and guarding ground plane wider than the microstrip line width. Otherwise this line is not able to work as microstrip line but coplanar line.
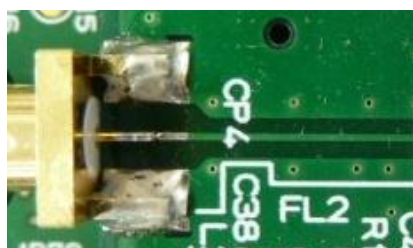
Figure 2-6 Example of Layout of Microstrip Line

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2.3 ESD Protection by λ/4 Short Stub

The implementation of λ/4 short stub is the best way to improve the product's robustness against ESD coming through RF line. λ/4 short stub is structured with the microstrip line, and the input impedance depends on the electrical length of it. So it is very important to design the electrical length of λ/4 short stub correctly.

Well-designed λ/4 short stub has features as below.
- High impedance in GPS/GNSS signal frequency band to minimize the insertion loss.
- Low impedance in other frequency band to bypass the ESD energy to ground.
- No additional component required.

MASC is also very useful to design λ/4 short stub correctly and efficiently. Figure 2-7 shows an example of calculation result.

In case of using 87 series module, which can receive GPS/Galileo and GLONASS, the frequency should be set to 1,589 MHz as the center frequency of both constellations. In case of using 86 series receiver module, it should be set to 1575.42 MHz as the center frequency of GPS/Galileo signal.

Analysis/Synthesis Values

Width	0.31	--->	Z0 (Ohms)	50.18
Length	26.85	<---	Elec. Len. (degrees)	90
Frequency	1589		MHz ▾	

Figure 2-7 An Example of λ/4 Short Stub Line Length Design by MASC

Figure 2-8 shows an example of the simulation result on Insertion Loss-Frequency characteristics of λ/4 short stub shown in Figure 2-7 by using Agilent ADS^{TM} software. This result shows the insertion loss will be only 0.281 dB at 1.589 GHz, and the variation of insertion loss between 1.234 GHz to 1.830 GHz is less than 0.1 dB. It means that the λ/4 short stub design is not critical against the in insertion loss.
In case of using active antenna, this loss is compensated by the LNA in the active antenna, and the total system NF (Noise Figure) won't be changed. Therefore there is no negative impact from inserting λ/4 short stub in this case.

In case of using passive antenna, it can cause the degradation of receiver sensitivity. However, the loss itself is very small, and the benefit to implement the λ/4 short stub is significant for protecting the module from ESD stress. Therefore it is highly recommended to install λ/4 short stub even in the passive antenna case.
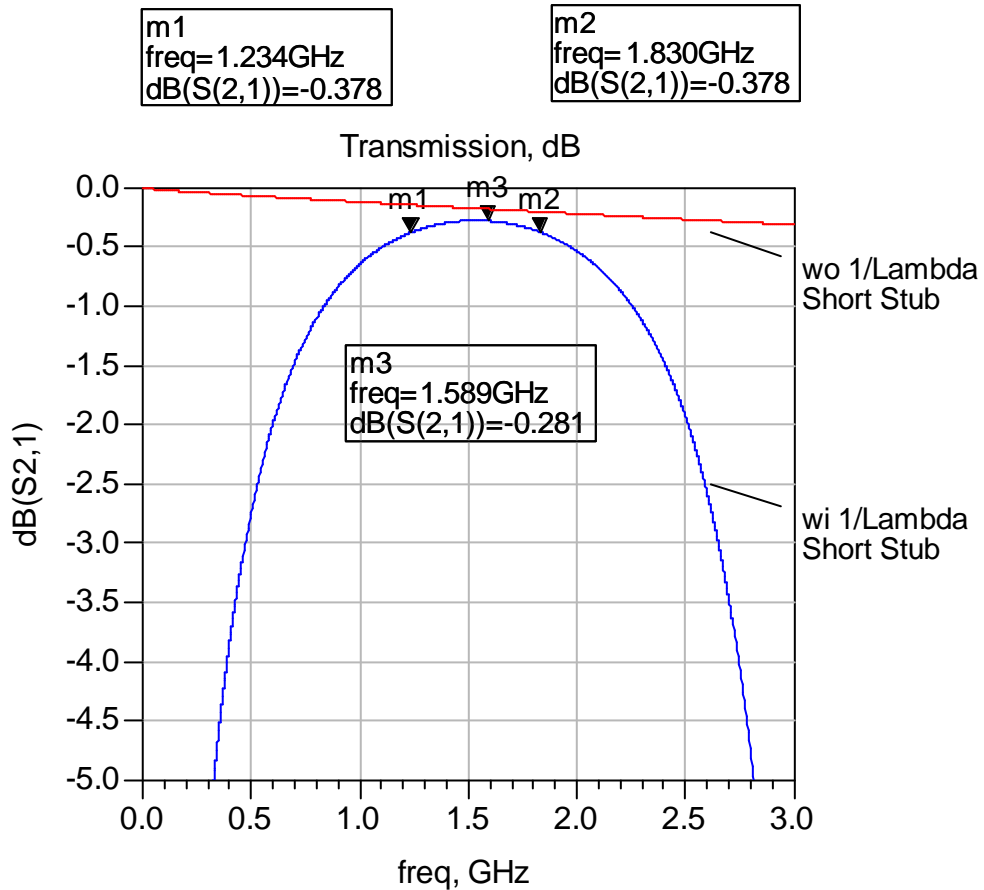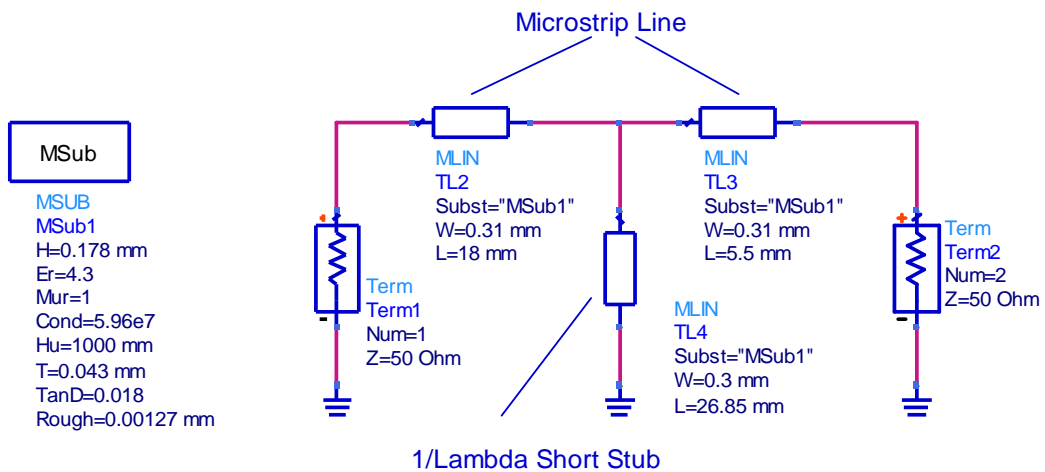
Microstrip Line

MSub

MSUB
MSub1
H=0.178 mm
Er=4.3
Mur=1
Cond=5.96e7
Hu=1000 mm
T=0.043 mm
TanD=0.018
Rough=0.00127 mm

MLIN
TL2
Subst="MSub1"
W=0.31 mm
L=18 mm

MLIN
TL3
Subst="MSub1"
W=0.31 mm
L=5.5 mm

Term
Term1
Num=1
Z=50 Ohm

MLIN
TL4
Subst="MSub1"
W=0.3 mm
L=26.85 mm

Term
Term2
Num=2
Z=50 Ohm

1/Lambda Short Stub

m1
freq=1.234GHz
dB(S(2,1))=-0.378

m2
freq= 1.830GHz
dB(S(2,1))=-0.378

Transmission, dB

m3
freq=1.589GHz
dB(S(2,1))=-0.281

wo 1/Lambda
Short Stub

wi 1/Lambda
Short Stub

Figure 2-8 Insertion Loss-Frequency Characteristics with λ/4 Short Stub by Agilent ADS[TM]

2.4 DC Feed Inductor

For biasing an active antenna, an inductor is used to superpose DC voltage to RF line as a general method. In this case, the inductor must be selected to minimize the effect to the RF line characteristics, especially the characteristic impedance. Also the inductor needs to have enough current supply capability against the active antenna combined.

The guidelines to choice the inductor are shown below.
1. Need to have higher self-resonance frequency (SRF) than GPS/GNSS signal frequency.
2. Need to have high impedance in GPS/GNSS signal frequency band.
3. Need to have lower insertion loss in GPS/GNSS signal frequency band.
4. Need to have enough absolute maximum current ratings against current consumption of the active antenna.

Table 2-1 shows an example of inductor specifications, which is from HK1005 series data sheet made by TAIYO YUDEN. And also Figure 2-9 shows Impedance-Frequency characteristics of HK1005 series.

Table 2-1 Specifications of HK1005 Series

Part Number	Inductance	Q (min)	Rated Current (max)	DC Resistance (max)
HK100515NJ-T	15nH	8	300mA	0.46Ω
HK100518NJ-T	18nH	8	300mA	0.55Ω
HK100522NJ-T	22nH	8	300mA	0.6Ω
HK100527NJ-T	27nH	8	300mA	0.7Ω
HK100533NJ-T	33nH	8	200mA	0.8Ω
HK100539NJ-T	39nH	8	200mA	0.9Ω
HK100547NJ-T	47nH	8	200mA	1Ω
HK100556NJ-T	56nH	8	200mA	1Ω
HK100568NJ-T	68nH	8	180mA	1.2Ω
HK100582NJ-T	82nH	8	150mA	1.3Ω
HK1005R10J-T	100nH	8	150mA	1.5Ω

According to the guideline #1:
The peak of each impedance curve in Figure 2-9 shows the self-resonance phenomenon, and the frequency at the peak means the SRF of each inductor. It is shown that SRF of HK100582NJ-T (82nH) is lower than GPS/GNSS band. Also SNR of HK100568NJ-T (68nH) and HK100556NJ-T (56nH) are too close to GPS/GNSS band. So these three inductors are not eligible.

According to the guideline #2:
From Figure 2-9, it is also readable that the inductor that has a bigger inductance has a higher impedance in GPS/GNSS band. So HK100547NJ-T or HK100539NJ-T will be the best candidates.

According to the guideline #3:
Figure 2-10 shows the simulation result of the insertion loss. In this figure, HK100547NJ-T and HK100539NJ-T show similar insertion losses, so both can be used for the DC feed inductor.

According to the guideline #4:
The judgment according to the guideline #4 depends on the specifications of the active antenna that is combined and used together with 86/87 series module. In general, commercial active antennas require 30mA or less for LNA bias current, and HK1005 series inductor can supply 150mA or more, so this series can be used for almost applications.

From above verifications, HK100539NJ-T is recommended. This device is also selected for FURUNO 86/87 series module Evaluation Kit.

This type of SMD component has many second sources and similar series. If the other manufacturer's component or the other series component is used, it is recommended to gather all the necessary information from the provider, and to study through the guidelines as above.
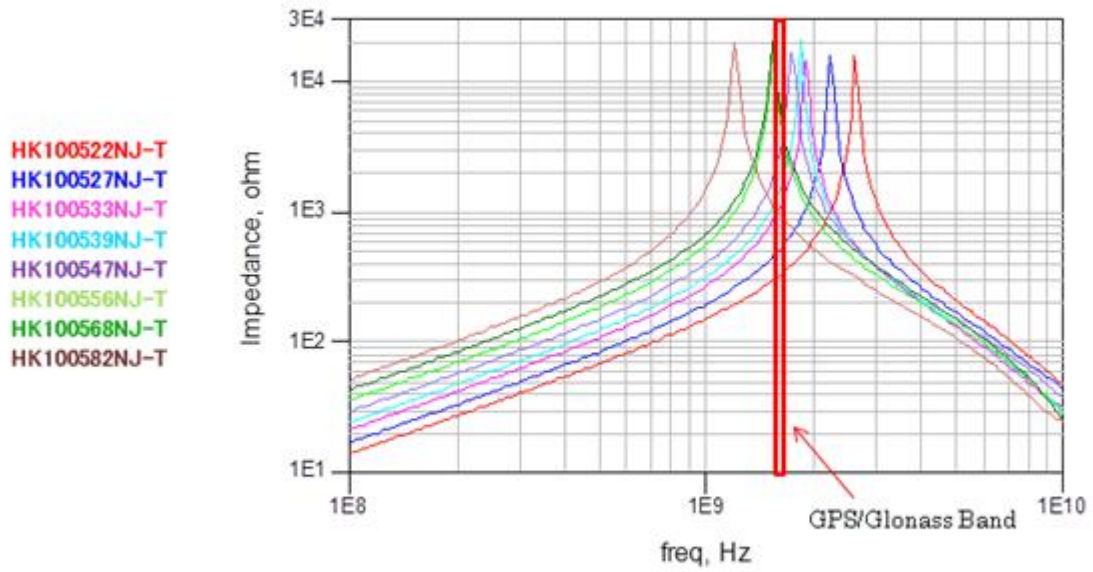
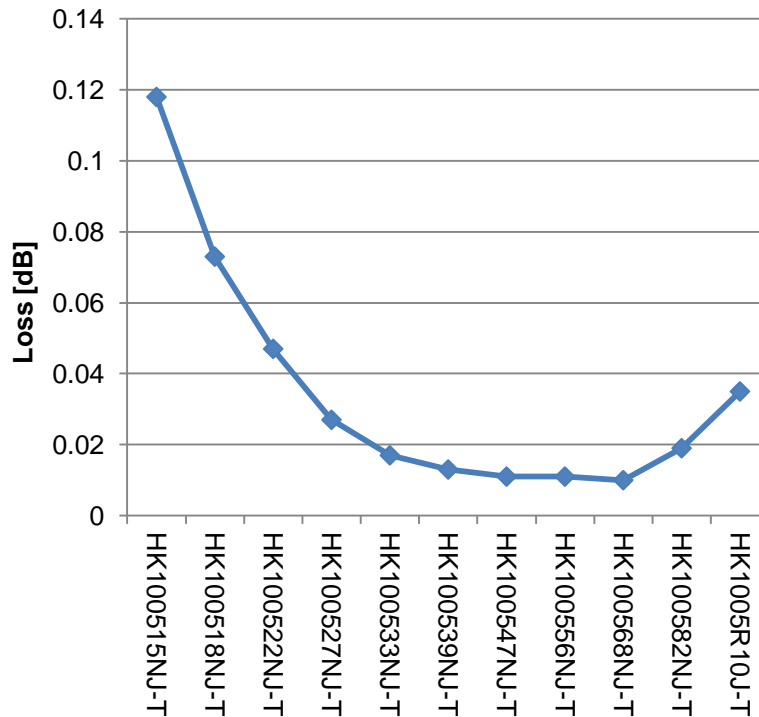**Figure 2-9 Impedance-Frequency Characteristics of HK1005 Series**

Figure 2-10 Insertion Loss by Implementing HK1005 Series @1589MHz

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It is recommended that DC Feed Inductor is placed close to the microstrip line as much as possible. If the soldering pad of the inductor is smaller than the width of the microstrip line, it should be placed on the microstrip line without any routing as shown in Figure 2-11.

Microstrip line

No Good   **Good**
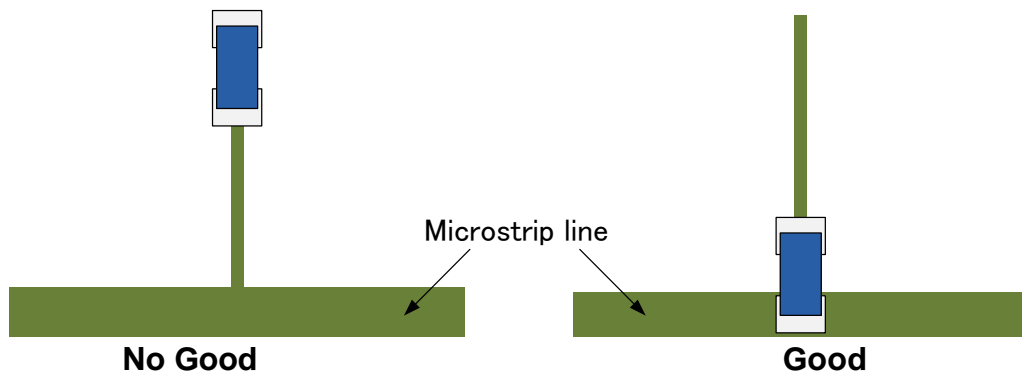
Figure 2-11 Recommended Layout of DC Feed Inductor at Microstrip Line

3 Antenna Interface

3.1 LNA Gain Selection

86/87 series modules have selectable gain LNA inside, which is able to be set to high gain mode or low gain mode for adapting various antennas. The high gain mode is applicable for using the passive antenna or the low gain active antenna, and the low gain mode for using the high gain active antenna, as shown in Table 3-1.

Table 3-1 Internal LNA Select Configuration

Antenna	LNA Config	Notes
Passive Antenna or Low Gain Active Antenna (Total Gain: 0 - 35 dB)	High Gain Mode	"High Gain Mode Antenna configuration the input of LNA in the active antenna to RF_IN of the module. It should include all the transmission losses such by coaxial cable, SAW filter (if inserted), the microstrip line, λ/4 short stub and so on.
High Gain Active Antenna (Total Gain: 15 - 50 dB)	Low Gain Mode	

For obtaining the better jamming immunity, the total gain of the active antenna must be lower as possible in the total gain window shown in Table 3-1. For example, in case of using the low gain mode, 15dB total gain antenna will show the best jamming immunity.

If the total gain is between 15dB to 35dB, it is recommended to use low gain mode. It also contributes to obtain lower power consumption.

There are two ways to configure the LNA gain as below:
- Connect FLNA pin to VCC or not (Hardware configuration)
- Feed ANTSEL command through serial communication channel (Software configuration)

Table 3-2 shows the configuration with using FLNA pin setting. And Table 3-3 shows the serial commands to configure the LNA gain via serial communication channel. The serial commands have higher priority than FLNA pin setting, and FLNA pin setting is ignored once the serial commands are fed. So DO NOT send ANTSEL commands when FLNA pin setting is used for configuration.

Table 3-2 Selection of LNA by FLNA Pin Setting

LNA	FLNA	Condition of ANTSEL
High Gain	Open	DO NOT send command.
Low Gain	High (connect to VCC)	

Table 3-3 Selection of LNA by ANTSEL Command

LNA	ANTSEL command	Condition of FLNA
High Gain	$PERDSYS,ANTSEL,FORCE1H*7F	These ANTSEL command is prioritized higher than FLNA pin setting. So once these commands are issued, FLNA pin setting is ignored.
Low Gain	$PERDSYS,ANTSEL,FORCE1L*7B	

3.2 Bias Circuit Design for Active Antenna

86/87 series module supports two ways to bias the active antenna. One is to use VCC_RF pin, which is designed to supply the antenna power from the module, as shown at the left side in Figure 3-1. The other is to provide from an independent antenna power (VANT) which is prepared by customer's system, as shown in the right side.

In case of using VCC_RF, the antenna bias voltage is same with VCC voltage provided to the module by customer's system. Therefore, if the active antenna requires different voltage like 5VDC, customer's system needs to prepare the required voltage as VANT and feed it to the antenna connector through the inductor as shown at the right side in Figure 3-1.
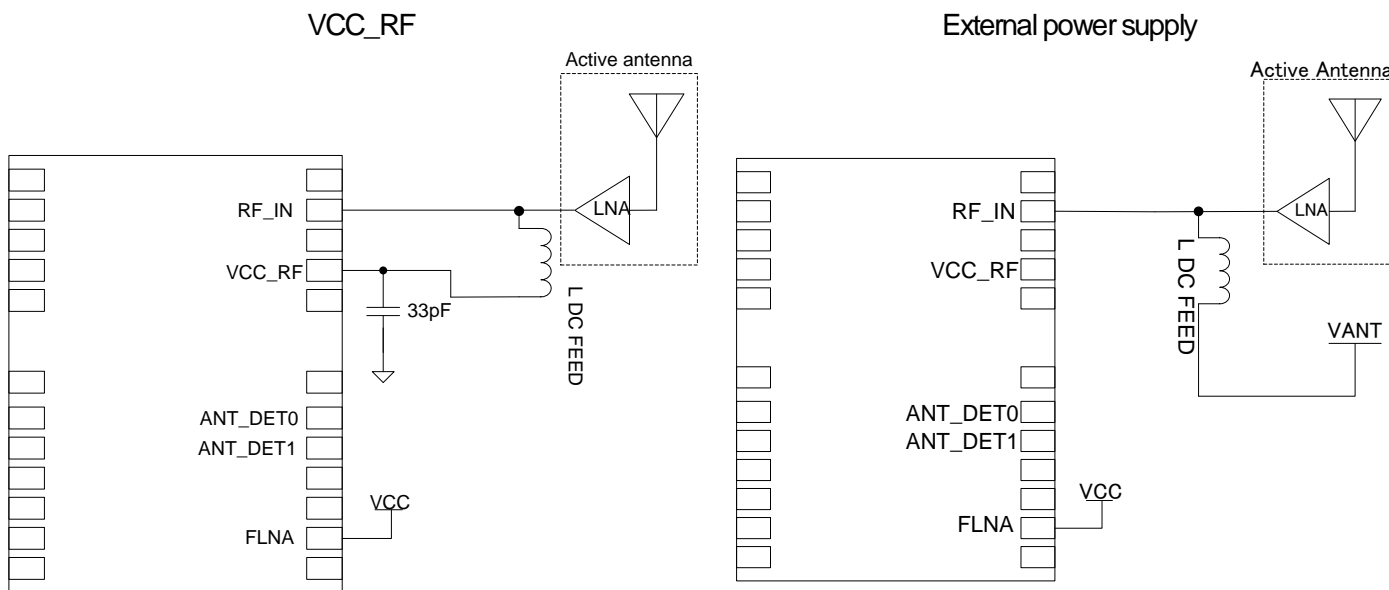
Figure 3-1 Active Antenna Power Supply Configuration

Figure 3-2 shows the insertion of the antenna detection circuit. Details are described in Section 3.5.
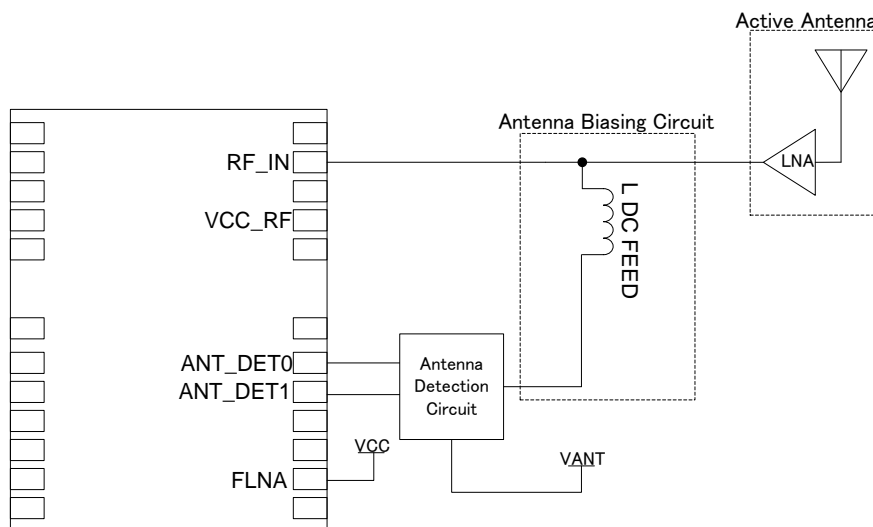
Figure 3-2 In Case of Using Antenna Detection Circuit
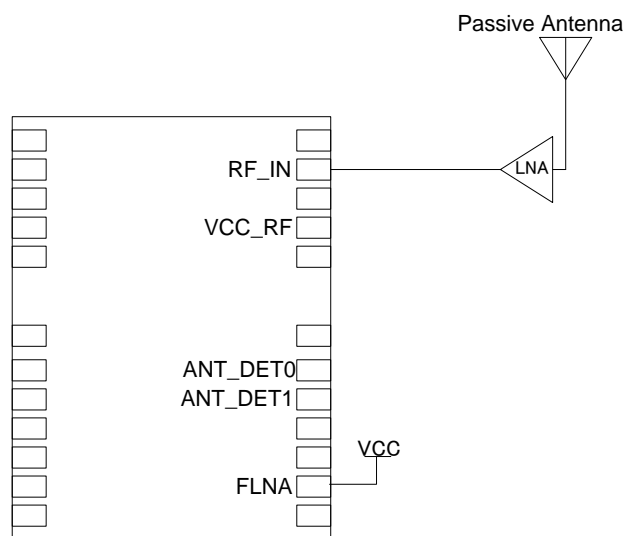
3.3 Passive Antenna Connection

Figure 3-3 shows the simplest circuit for passive antenna connection. Since the LNA in the module should be configured to high gain mode for passive antenna, so FLNA pin is left Open (no connection). The routing between the passive antenna and RF_IN pin should follow the microstrip line design rule as described in Section 2.2.

The sensitivity of 86/87 series module, that is described in the hardware specifications, is defined by the signal level at RF_IN pin. If the customer's product is required to achieve the system sensitivity same as the module sensitivity, the length of the cable and/or PCB routing between the passive antenna and RF_IN should be zero. In other words, the transmission loss from the passive antenna through RF_IN directly degrades the sensitivity of the system, for example, if the loss of this part is 3dB, then the system sensitivity will be 3dB worse than the module sensitivity.
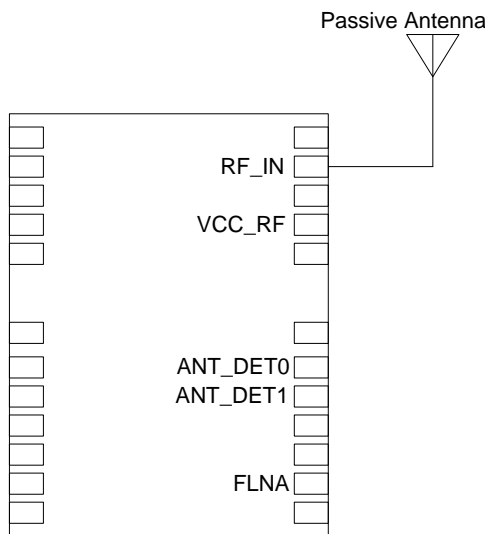
Figure 3-3 Most Simple Passive Antenna Configuration

In case the distance between passive antenna and the receiver module is long, and the transmission loss of this routing is not negligible, it is needed to add LNA near the passive antenna as shown in Figure 3-4. If the coaxial cable is used for the connection between the passive antenna and RF_IN, and the loss of the coaxial cable is not negligible, it is recommended to switch to the appropriate active antenna.

Figure 3-4 Passive Antenna Configuration with External LNA

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3.4 SAW Filter Insertion

86/87 series module contains SAW filter after the internal LNA, so normally it is not necessary to insert SAW filter on the user's board. But if the antenna receives very strong interference signal, it can cause the saturation of the internal LNA, then the reception performance can be degraded. In such case, inserting SAW filter between the antenna and RF_IN pin can improve the performance. If the system is required to work under the strong interference environment, it is recommended to insert SAW filter on the user's board as below.

When the active antenna is used, SAW filter should be placed between the capacitor and RF_IN pin as shown in Figure 3-5 (left). SAW filter has an insertion loss, generally 1dB to 2dB, but the insertion loss is negligible if the LNA in the active antenna has enough gain. If the total gain including SAW filter's insertion loss is in the adequate range shown in Table 3-1, no sensitivity degradation occurs.

When the passive antenna is used, SAW filter should be placed simply between the passive antenna and RF_IN pin as shown in Figure 3-5 (right). In this case, the reception sensitivity will be degraded 1dB to 2dB due to the insertion loss of SAW filter. But still enough sensitivity is kept for normal usage.
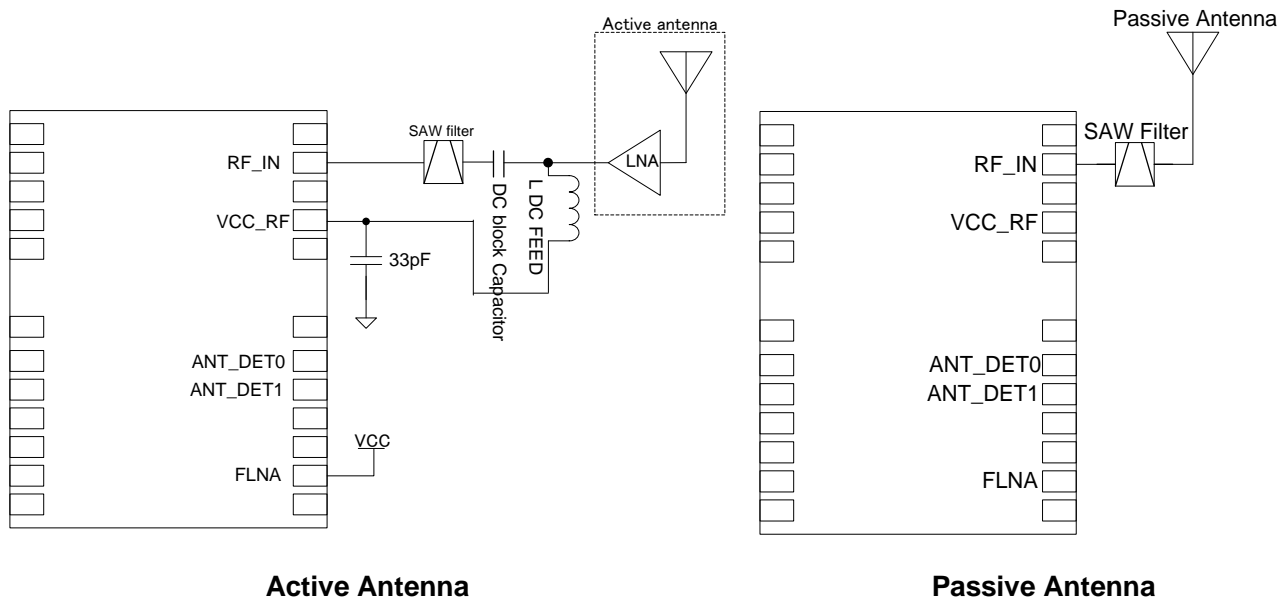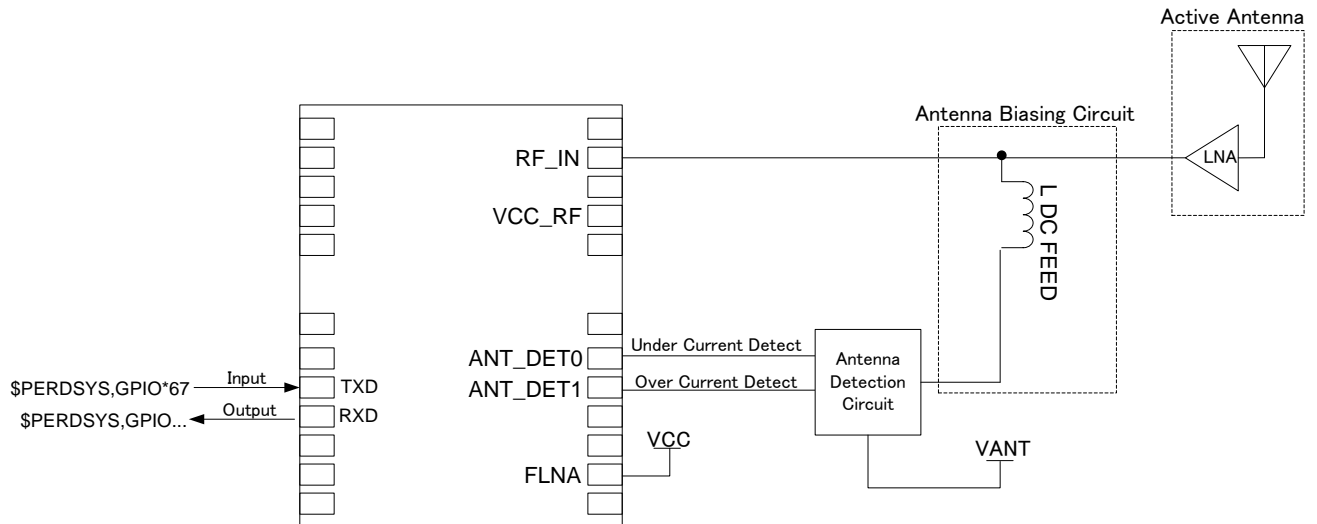
Active Antenna   **Passive Antenna**

Figure 3-5 Antenna Configuration with SAW Filter

3.5 Antenna Detection Circuit

3.5.1 Antenna Detection Circuit Overview

86/87 series module has two digital input pins (ANT_DET0 and ANT_DET1) to sense the status of the active antenna connection. These 2 input pins are designed to recognize 3 states of the antenna connection, that are "Antenna Open", "Normal" and "Antenna Short", and the status is reported to the host system via the serial communication channel.

For enabling this feature, Antenna Detection Circuit needs to be placed between the DC feed inductor and VANT, as shown in Figure 3-6. The details of the antenna detection circuit are described in Section 3.5.2.

Figure 3-6 Active Antenna Configuration with Antenna Detection Circuit

The NMEA sentence of "$PERDSYS,GPIO" is used to report the antenna status to the host system. When the module receives NMEA command "$PERDSYS,GPIO*67", the receiver responds once with transmitting the NMEA sentence shown below, which contains 2 bits to copy the status of ANT_DET0 and ANT_DET1 pins. The logic of these 2 bits is shown in Table 3-4.

$PERDSYS ,GPIO, X X H H L L L L L L*07
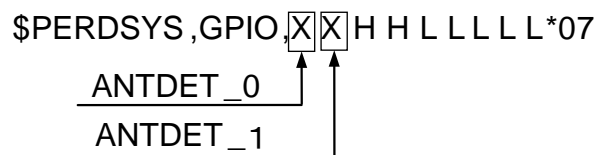
ANTDET_0

ANTDET_1

Table 3-4 Relation ANT_DET0 and ANT_DET1 to Status of Antenna Connection

Status of antenna connection	ANT_DET0	ANT_DET1
Antenna open	1	1
Normal	0	1
Antenna short	0	0
Undefined	1	0

3.5.2 Antenna Detection/Protection Circuit

The Antenna Detection Circuit, shown at the right side in Figure 3-8, contains one sensing resistor (R1) and two comparators. The sensing resistor is inserted between VANT and the antenna connector, and all the antenna bias current runs through this, so the voltage drop (VANT – VDET) is proportional to the antenna bias current. Two comparators compare VDET with two threshold voltages, VREF_O for detecting Antenna open state and VREF_S for Antenna short state, and create ANT_DET0 and ANT_DET1 signals. Note that VREF_O is always higher than VREF_S.

If VDET is higher than VREF_O, ANT_DET0 and ANT_DET1 are both set to "1". This shows "Antenna open" state. If VDET is lower than VREF_O but higher than VREF_S, ANT_DET0 is set to "0" and ANT_DET1 is set to "1". This shows "Normal" state. And if VDET is lower than VREF_S, ANT_DET0 and ANT_DET1 are both set to "0". This shows "Antenna short" state. Figure 3-7 shows the relation between the bias current and two detection bits, ANT_DET0 and ANT_DET1.

It is recommended to implement Over Current Protection Circuit for preventing any potential incident in the market field. The Over Current Protection Circuit, shown at the left-upper side in Figure 3-8, contains two transistors and resistors. Once the antenna bias current increases, the voltage drop at R2 also increases, Q1 turns on, the bias voltage of Q2 decreases, then the antenna bias current decrease. Note that the maximum current (shown as "IOC" in Table 3-5) keeps flowing even if the antenna connector is shorted to ground.

The threshold currents of the Antenna Detection Circuit and the maximum current of the Over Current Protection Circuit are determined by the combination of resistor values and VANT. Table 3-5 shows the specifications of these circuits with the resistor values shown in Figure 3-8 and Table 3-6.

It is possible to change these thresholds and limitation with changing resistor values. Details are described in Section 3.5.3 and 3.5.4.

Table 3-5 Specifications of Sample Circuit Shown in Figure 3-8

$@T_A=25°C$

Antenna power supply voltage(VANT)	5V [typ]
Threshold of antenna open(I_{ANT_O}):	6 mA [typ]
Threshold of antenna short (I_{ANT_S}):	64 mA [typ]
Over current limitation (I_{OC}):	117 mA [typ]
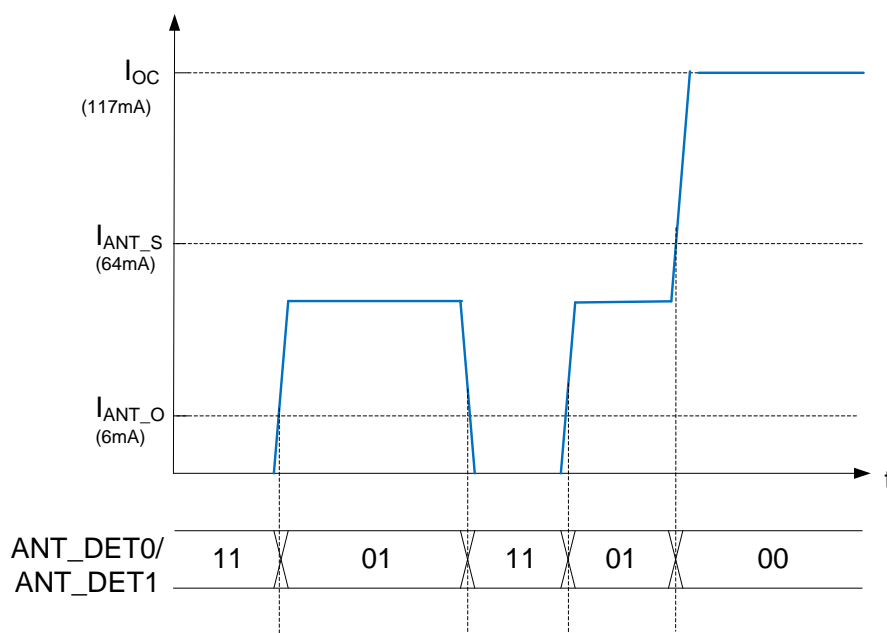
Figure 3-7 Relation between IANT and ANT_DET0/1 bits
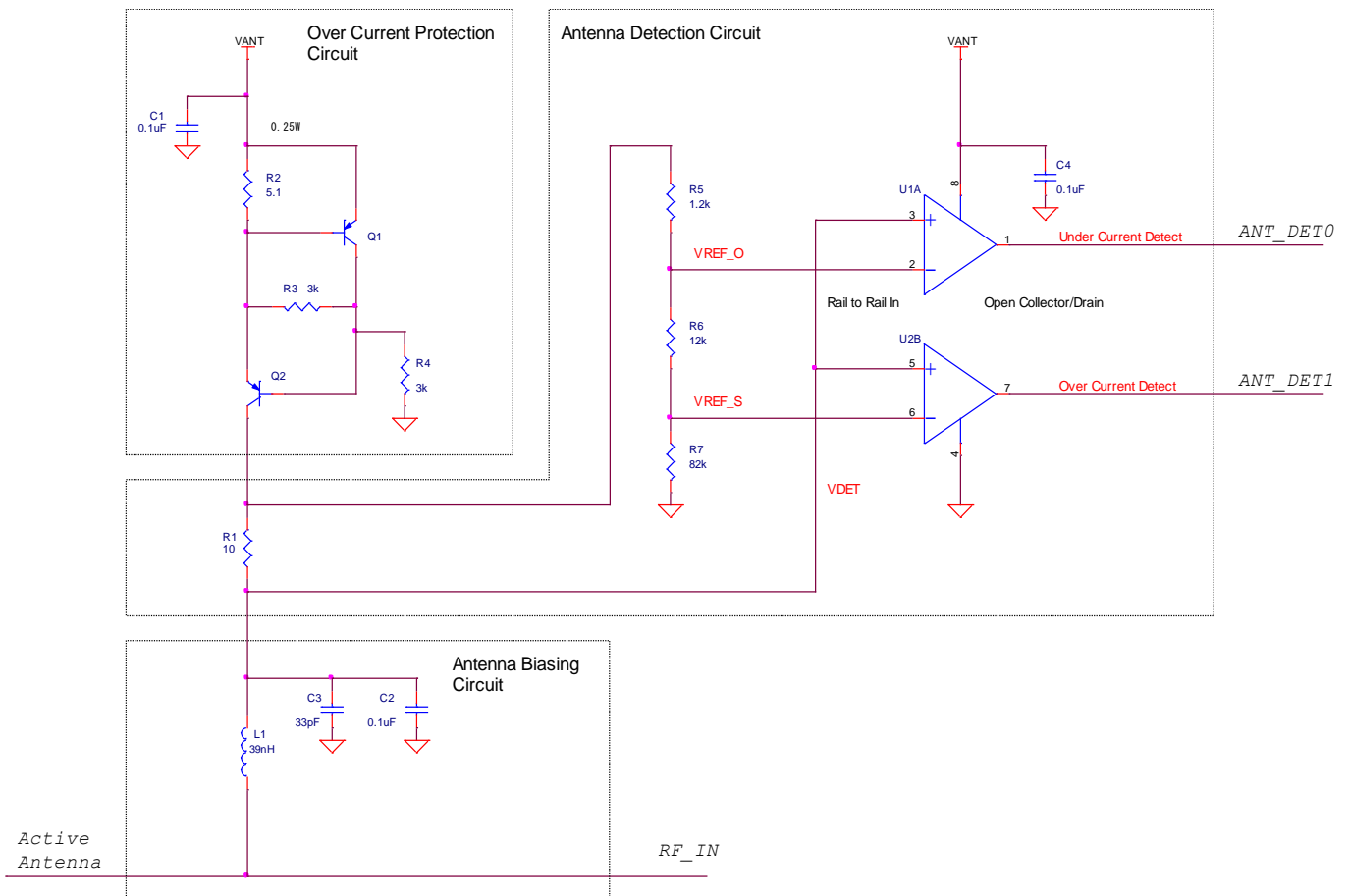
Figure 3-8 Recommended Antenna Detection and Over Current Protection Circuit

Table 3-6 Bill of Material

Component	Recommended Specification	Notes
C1,C2,C4	0.1uF	
C3	33pF	
L1	39nH	e.g. HK100539NJ-T (TAIYO YUDEN)
Q1	PNP Transistor	e.g. 2SA2029 (ROHM)
Q2	PNP Transistor	Corrector tolerance dispassion more than 1W e.g. MCH6101 (SANYO)
R1	10Ω±5%, 1/4W	
R2	5.1Ω±5%, 1/8W	
R3, R4	3kΩ±5%	
R5	1.2kΩ±5%	
R6	12kΩ±5%	
R7	82kΩ±5%	
U1	2ch comparator Rail to Rail Input Open Collector /Drain Output	e.g. TLV3402 (Texas Instruments)

3.5.3 Modification of Antenna Short/Open Threshold

The threshold currents for detecting "Antenna open" and "Antenna short" are able to be changed with adjusting the values of resistors in Antenna Detection Circuit.

The three parameters, that are VREF_O, VREF_S and VDET, are given by following three equations.

Reference voltage for antenna open (VREF_O) is given as
$$V_{RFF\_O} = (VANT - I_{ANT} \times R2 - V_{CE}) \times (R6 + R7)/(R5 + R6 + R7) \qquad (3.1)$$

Reference voltage for antenna short (VREF_S) is given as
$$V_{RFF\_S} = (VANT - I_{ANT} \times R2 - V_{CE}) \times R7/(R5 + R6 + R7) \qquad (3.2)$$

Detection voltage (VDET) is given as
$$V_{DET} = VANT - I_{ANT} \times (R1 + R2) - V_{CE} \qquad (3.3)$$

V_{CE}: Transistor Q2 Collector-Emitter voltage
I_{ANT}: Antenna current

As described in Section 3.5.2, detection conditions are as below:
Antenna open status: $V_{REF\_O} < V_{DET}$
Antenna short status: $V_{DET} < V_{REF\_S}$

Then Antenna open and short detection current are derived from above equations.

Antenna open detection current：
$$I_{ANT\_O} < \frac{R5}{R1 \times (R5+R6+R7) + R2 \times R5} \times VANT \qquad (3.4)$$

Antenna short detection current：
$$I_{ANT\_S} > \frac{R5+R6}{R1 \times (R5+R6+R7) + R2 \times (R5+R6)} \times VANT \qquad (3.5)$$

Notes: V_{CE} is omitted for VANT = 5V typ. >> V_{CE} = 0.11V typ.

So it is possible to shift the threshold current with adjusting the values of registers in above equations.

3.5.4 Modification of Over Current Protection Threshold

The setting of the Over Current Protection Threshold (I_{CC}) is simple. It is given with the equation (3.6).

$$I_{OC} = V_{BE}/R2 \qquad (3.6)$$

V_{BE}: Transistor Q1 Base-Emitter voltage

In Figure 3-8, R2 is set to 5.1Ω, and VBE is 0.6V typically, so I_{OC} is set to 117 mA (=0.6/5.1) as shown in Table 3-5.

Notes: In case of changing I_{OC}, please make sure the maximum current and/or the power rating of relevant resistors, inductors and capacitors.

3.6   Layout Design with Patch Antenna

### 3.6.1   Incurrence to Antenna Characteristics by Layout

As the following electrical characteristics of patch antenna are changed due to ground plane effect by placement of where the patch antenna is located and VSWR, user has to ask antenna vendor to do tuning of the electrical characteristics with actual location environment.

-Center frequency
-Gain at Zenith
-Axial Ratio
-Directivity pattern

As an example, we measured antenna characteristics (frequency characteristics and directivity pattern) with the following three kind of PCB size (PCB1, PCB2 and PCB3) and location of patch antenna.

Notes: We use antenna by tuning at PCB1
PCB size and implementation position of patch antenna

PCB1	PCB2	PCB3
75mm x 75mm	40mm x 140mm	40mm x 140mm
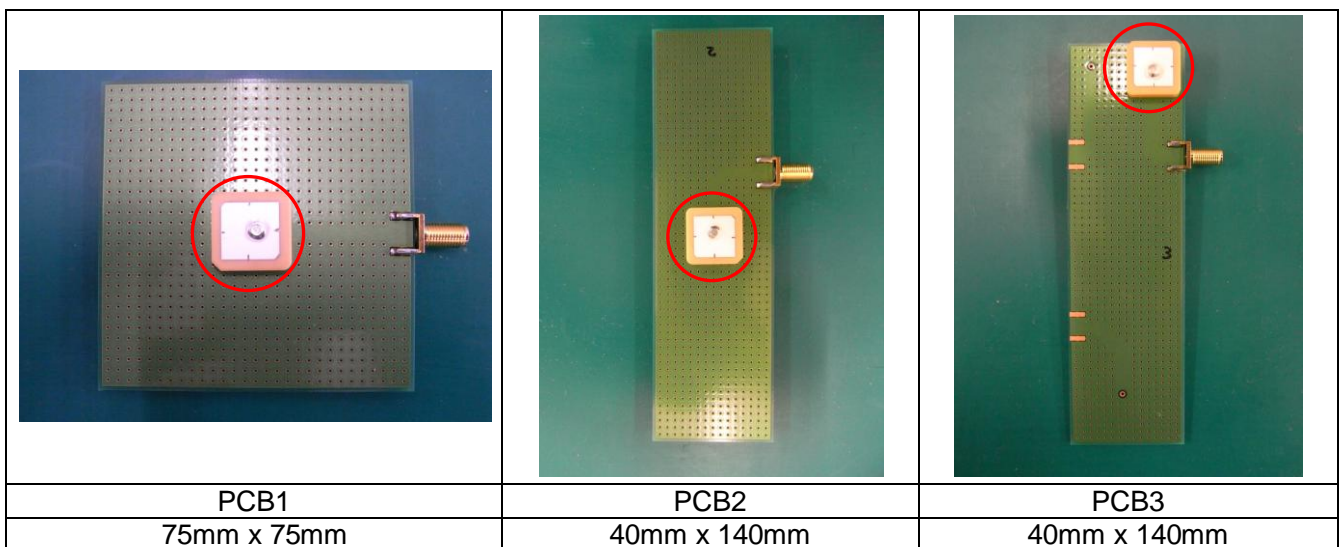
**Figure 3-9 Printed Circuit Board Size and Patch Antenna Position**
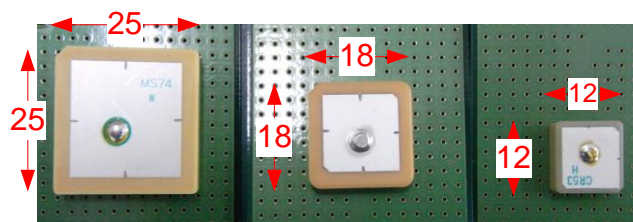
Figure 3-10 Patch Antenna Size (unit: mm)

We measured the following evaluation item after tuning return loss characteristic at 75mm x75mm PCB.

Table 3-7 Measurement Data

Measurement Item		Measurement Data								
		PCB1			PCB2			PCB3		
		25mm	18mm	12mm	25mm	18mm	12mm	25mm	18mm	12mm
Return Loss	1575MHz[dB]	-17.9	-23.6	-31.6	-16.1	-12.7	-20.2	-12.3	-4.3	-2.8
	B.W.@-10dB[MHz]	29.3	18.3	11.2	24.4	16.8	11.1	27.6	7.9	- [*1]
Gain [dBic]	1575MHz	3.6	2.5	2.4	0.6	0.0	-1.6	0.6	-5.4	-8.1
Axial Ratio [dB]	1575MHz	2.1	2.8	3.1	18.1	10.7	22.4	10.6	14.1	26.2

Notes **1)**: - Not possible to measure due to huge degradation

25mm x 25mm

18mm x 18mm

12mm x 12mm
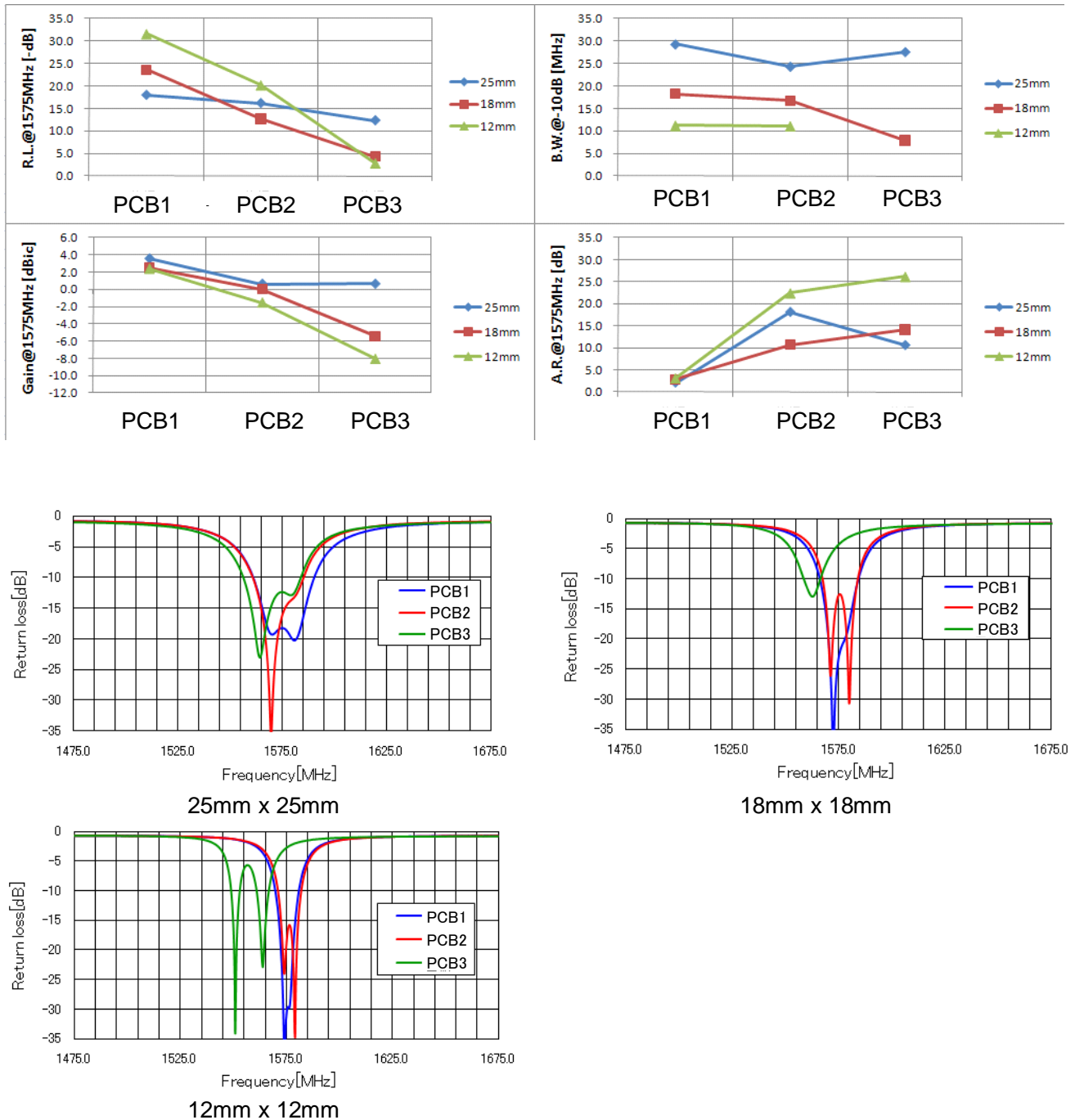
Figure 3-11 Measurement Data

This graph shows the directivity pattern. You can observe directivity has influence by implementation position on the PCB.
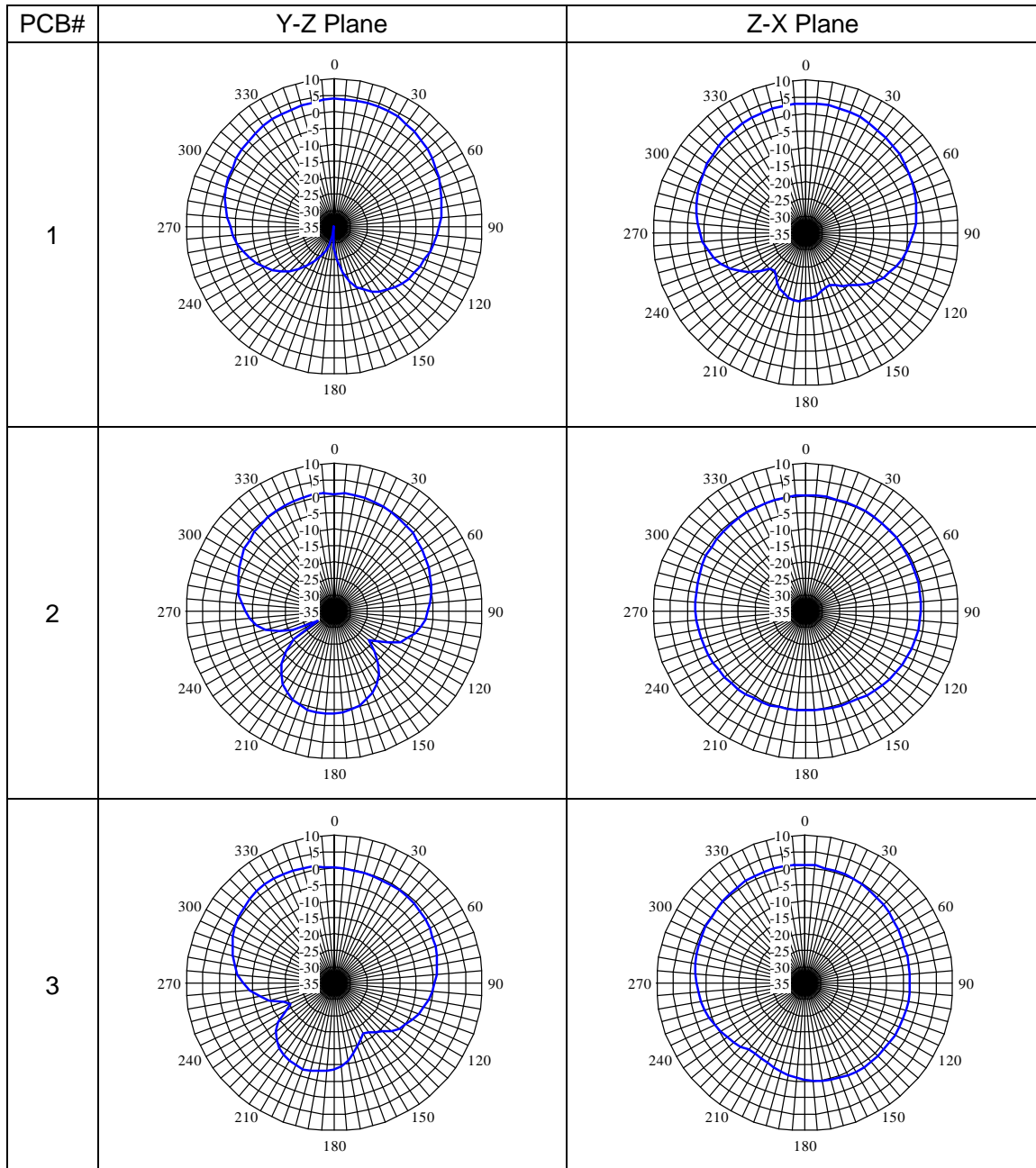
PCB#	Y-Z Plane	Z-X Plane
1		
2		
3		

Figure 3-12 Directivity Pattern (25 mm x 25 mm Size Patch Antenna)

PCB#	Y-Z Plane	Z-Plane
1		
2		
3		
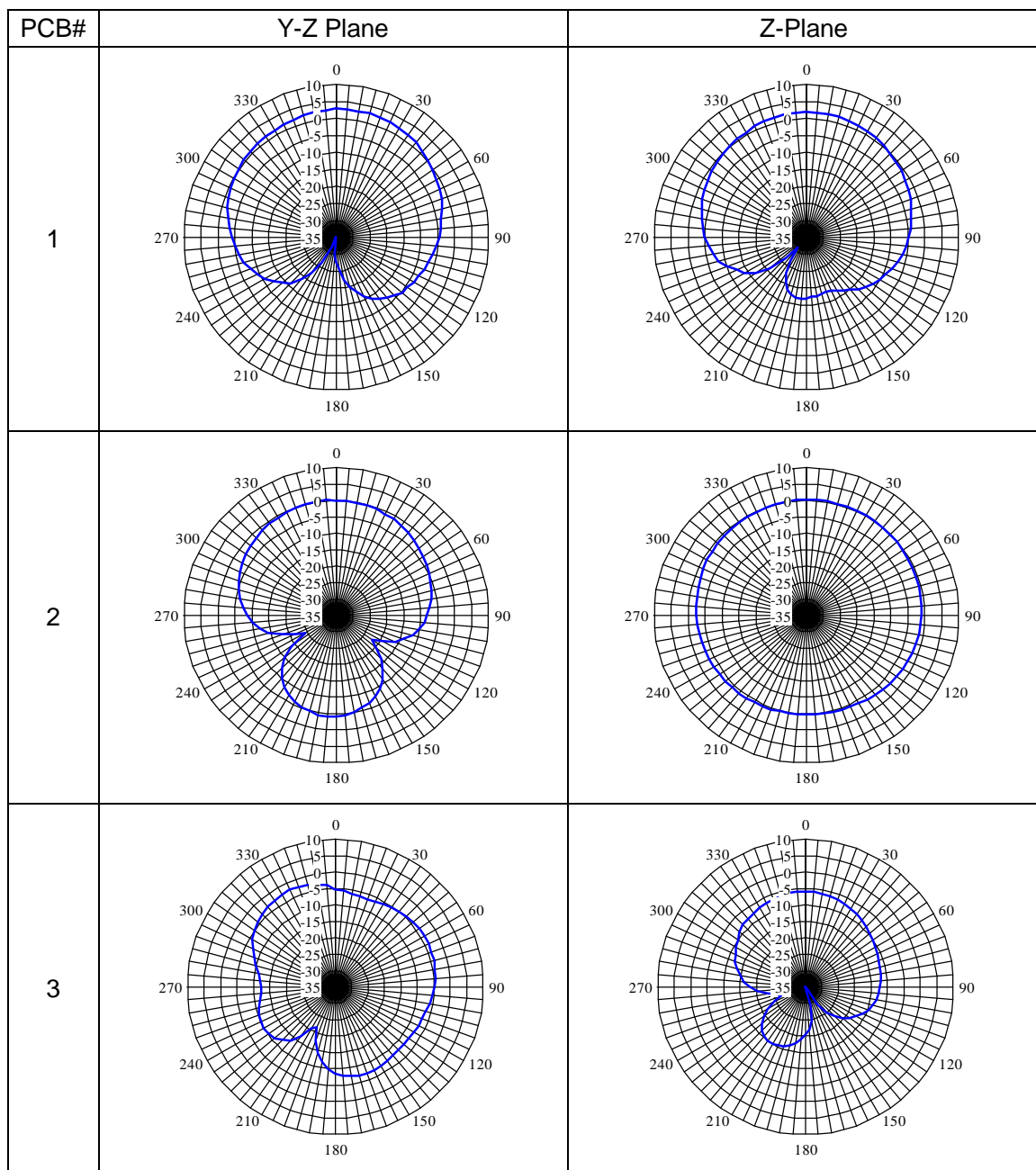
Figure 3-13 Directivity Pattern (18 mm x 18 mm Size Patch Antenna)

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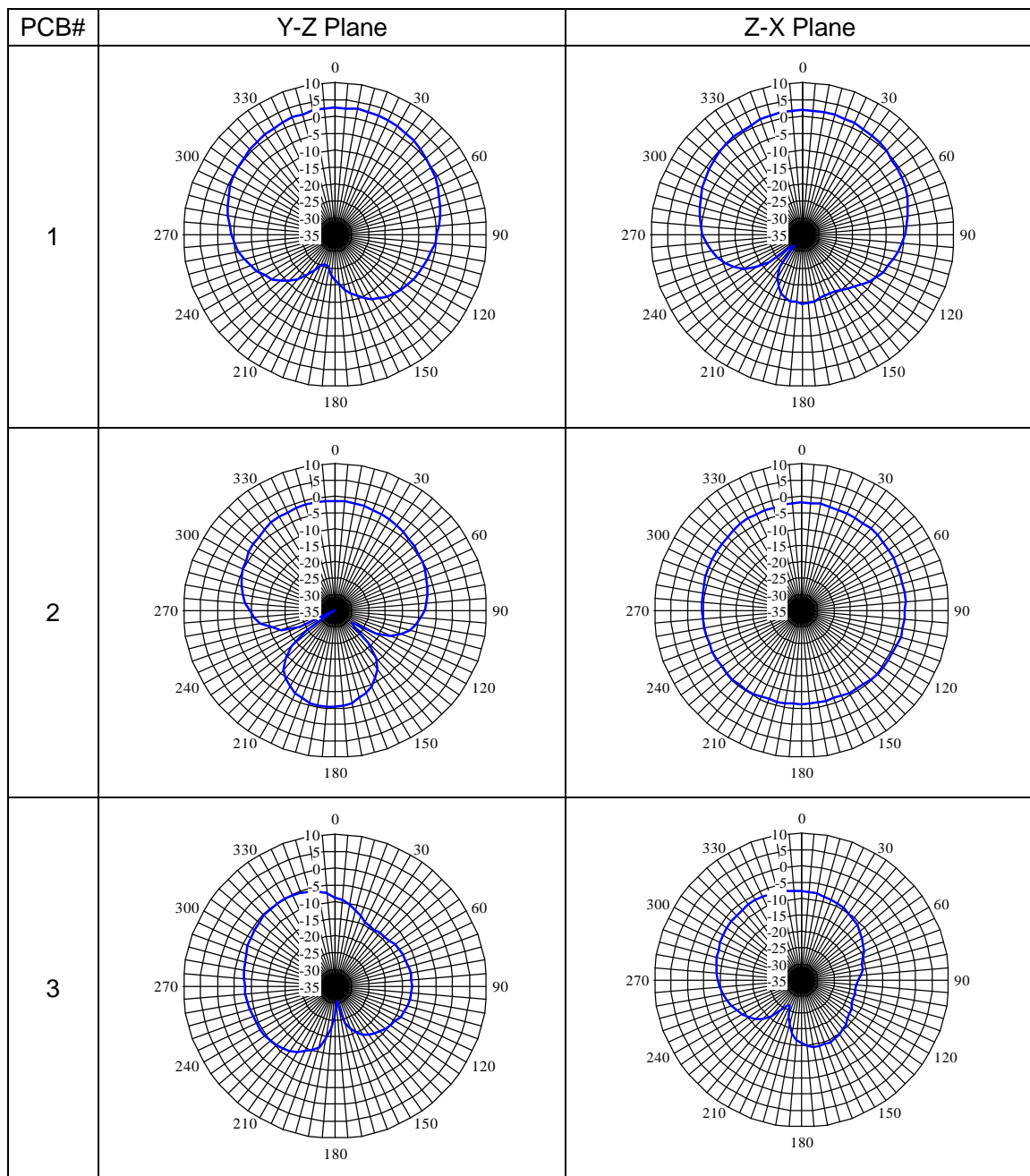| PCB#	Y-Z Plane	Z-X Plane
1		
2		
3		

Figure 3-14 Directivity Pattern (12 mm x 12 mm Size Patch Antenna)

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3.6.2 Noise Influence Issue by Layout

As patch antenna may have the influence radiation noise from via hole on the bottom side of antenna, layout of bottom side of antenna should be no via hole.

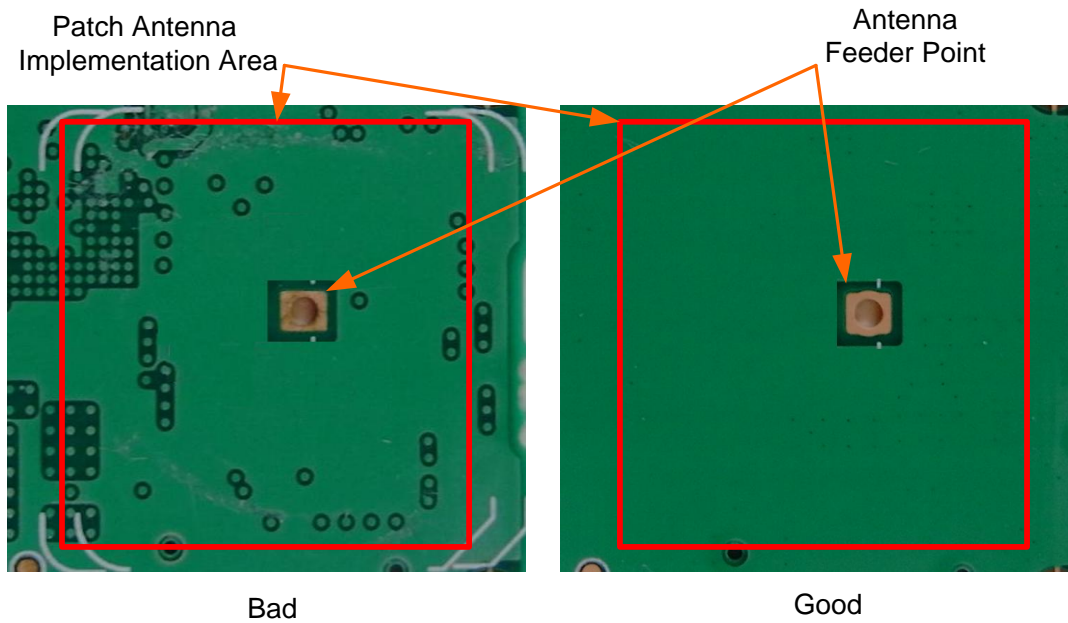The below pictures show bad and good layout of the bottom side of antenna.

Figure 3-15

4 Bypass Capacitor for VCC

Since 86/87 series module internally has bypass capacitors for VCC, so it is not required to implement any bypass capacitor on the customer's board. However, in case the ripple noise on VCC line is more than ±50 mV, the additional bypass capacitor is required to be placed close to VCC pin.

Please note that the ripple noise amplitude should be kept less than ±50 mV, otherwise the receiver may have the degradation of sensitivity performance due to noise influences.

5 Mechanical Stress Control

Depend on the location of 86/87 series module on user's PCB, the receiver may have the mechanical stress due to the wrap of the PCB that is given with screwing the PCB to the chassis with unbalanced torque. Therefore, It is recommended to layout the module to the place at the middle of the of screw holes.

If the module is placed close to the screw hole, it is needed to manage the screw torque uniform for every screw holes for minimizing the stress from the wrap of the PCB.
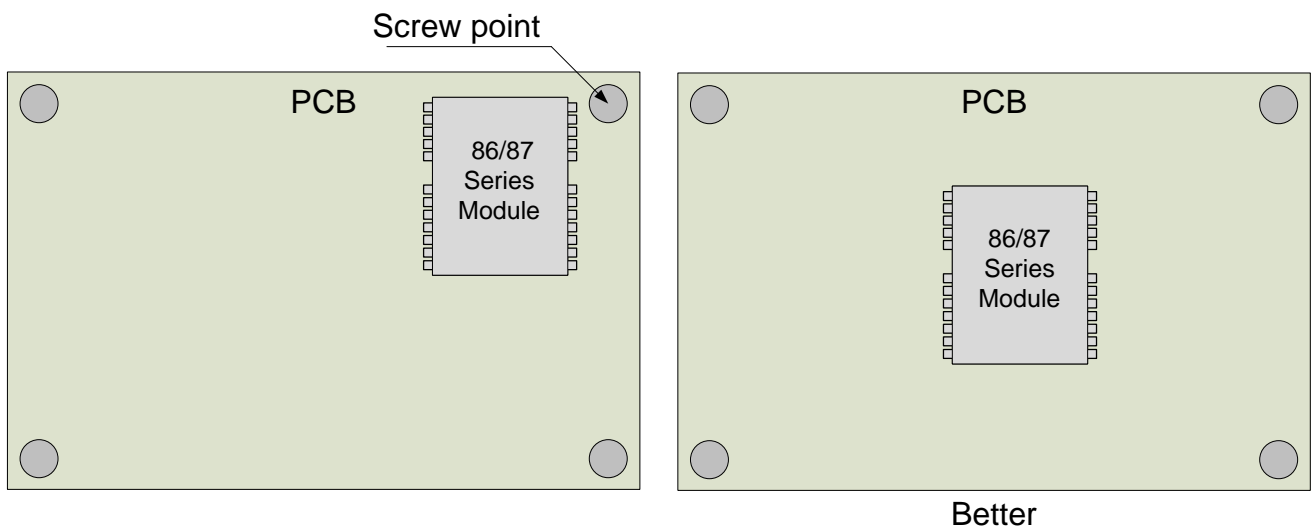

Figure 5-1 Recommended Receiver Implementation Position

6   Related Documents

-GN-86F Hardware Specifications   (Document No. G13-000-10-003)
-GN-87F Hardware Specifications   (Document No. G13-000-10-001)
-GN-8615 Hardware Specifications   (Document No. G14-000-10-007)
-GN-8715 Hardware Specifications   (Document No. G14-000-10-009)
-GV-86 Hardware Specifications   (Document No. G13-000-10-008)
-GV-87 Hardware Specifications   (Document No. G13-000-10-006)
-GV-8615 Hardware Specifications   (Document No. G14-000-10-011)
-GV-8715 Hardware Specifications   (Document No. G14-000-10-013)
-GT-86 Hardware Specifications   (Document No. G13-000-10-017)
-GT-87 Hardware Specifications   (Document No. G13-000-10-015)

7   Contact Information

FURUNO ELECTRIC CO., LTD
2-20 Nishinomiya-Hama
Nishinomiya, Japan
Tel: +81-798-33-9588

FURUNO U.S.A., Inc.
GPS/OEM Timing Division
70 Engerman Avenue
Denton, MD 21629
Tel: +1 (410) 479-4420
Fax: +1 (410) 479-4429
gpssales@furuno.com

FURUNO Deutschland GmbH
GPS-Core Business Support
Konrad Zuse Platz 8
Wappenhalle
81829 Munich, Germany
Tel: +49 (89) 207-042-340
infoEurope@furuno.com