AK6480C/81C

8Kbit Serial CMOS EEPROM

Features

☐ ADVANCED CMOS EEPROM TECHNOLOGY

☐ READ/WRITE NON-VOLATILE MEMORY
- Wide VCC (1.8V to 5.5V) operation
- 8192 bits: 512 × 16 organization

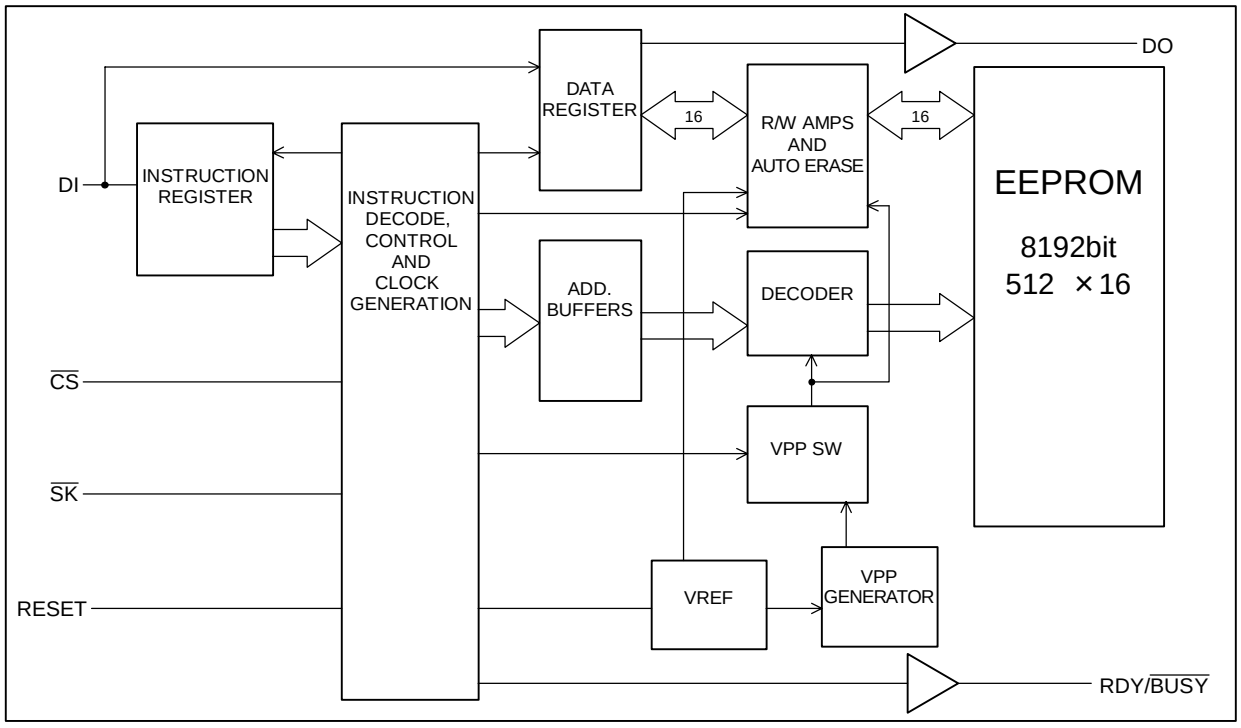
☐ ONE CHIP MICROCOMPUTER INTERFACE
- Interface with one chip microcomputer's serial communication port directly

☐ LOW POWER CONSUMPTION
- 0.8μA Max. (Standby mode)

☐ HIGH RELIABILITY
- Endurance : 1000K cycles/Address
- Data Retention : 10 years

☐ SPECIAL FEATURES
- 8 word Page Write Mode
- High speed operation (f_{MAX}=5MHz: VCC=4.5V to 5.5V)
- Automatic write cycle time-out with auto-ERASE (5ms Max.)
- Automatic address increment (READ)
- Ready/ $\overline{\text{Busy}}$ status signal
- Software and Hardware controlled write protection

☐ IDEAL FOR LOW DENSITY DATA STORAGE
- Low cost, space saving, 8-pin package (SOP, SSOP, MSOP, SON)



Block diagram

General Description

The AK6480C/81C is a 8192bit, serial, read/write, non-volatile memory device fabricated using an advanced CMOS EEPROM technology. The AK6480C/81C has 8192bits of memory organized into 512 registers of 16 bits each. The AK6480C/81C can operate full function under wide operating voltage range from 1.8V to 5.5V. The charge up circuit is integrated for high voltage generation that is used for write operation.
The AK6480C/81C can connect to the serial communication port of popular one chip microcomputer directly (3 line negative clock synchronous interface). At write operation, AK6480C/81C takes in the write data from data input pin (DI) to a register synchronously with rising edge of input pulse of serial clock pin ($\overline{SK}$). And at read operation, AK6480C/81C takes out the read data from a register to data output pin (DO) synchronously with falling edge of $\overline{SK}$.
The AK6480C/81C has 5 instructions such as READ, WRITE, PAGE WRITE, WREN (write enable) and WRDS (write disable). Each instruction is organized by op-code block (8bits), address block (8bits) and data (8bits x 2). When input level of $\overline{SK}$ pin is high level and input level of chip select ($\overline{CS}$) pin is changed from high level to low level, AK6480C/81C can receive the instructions.
Special features of the AK6480C/81C include : automatic write time-out with auto-ERASE, Ready/ $\overline{Busy}$ status signal output and ultra-low standby power mode when deselected ($\overline{CS}$ =high).

・Software and Hardware controlled write protection
The AK6480C/81C has 2 (hardware and software) write protection functions.
After power on or after execution of WRDS (write disable) instruction, execution of WRITE instruction will be disabled. This write protection condition continues until WREN instruction is executed or VCC is removed from the part.
Execution of READ instruction is independent of both WREN and WRDS instructions.
Reset pin should be low level when WRITE instruction is executed. When the Reset pin is high level, the WRITE instruction is not executed.

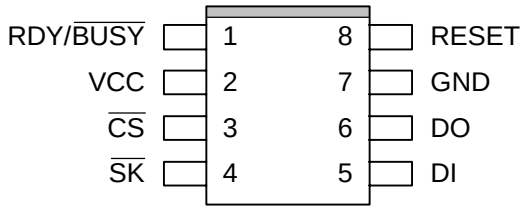
・Ready/ $\overline{Busy}$ status signal
During the automatic write time-out period ($\overline{Busy}$ status), the AK6480C/81C can't accept the other instructions. The AK6480C/81C has 2 functions to know the $\overline{Busy}$ status from exterior.
The RDY/ $\overline{BUSY}$ pin indicates the $\overline{Busy}$ status regardless of the $\overline{CS}$ pin status. The RDY/ $\overline{BUSY}$ pin outputs the low level regardless of the $\overline{CS}$ pin status during $\overline{Busy}$ status. Except the above status, this pin outputs high level.
Also the DO pin indicates the $\overline{Busy}$ status. When input level of $\overline{SK}$ pin is low level and input level of $\overline{CS}$ pin is changed from high level to low level, the AK6480C/81C is in the status output mode and the DO pin indicates the Ready/ $\overline{Busy}$ status. The Ready/ $\overline{Busy}$ status outputs on DO pin until $\overline{CS}$ pin is changed from low level to high level, or first bit ("1") of op-code of next instruction is given to the part. Except when the device is in the status output mode or outputs data, the DO pin is in the high impedance state.

■ Type of Products

Model	Temp.Range	VCC	Package
AK6480CF	-40°C to 85°C	1.8V to 5.5V	8pin Plastic SOP
AK6480CM	-40°C to 85°C	1.8V to 5.5V	8pin Plastic SSOP
AK6480CH	-40°C to 85°C	1.8V to 5.5V	8pin Plastic MSOP
AK6480CL	-40°C to 85°C	1.8V to 5.5V	8pin Plastic SON
AK6481CM	-40°C to 85°C	1.8V to 5.5V	8pin Plastic SSOP
AK6481CH	-40°C to 85°C	1.8V to 5.5V	8pin Plastic MSOP

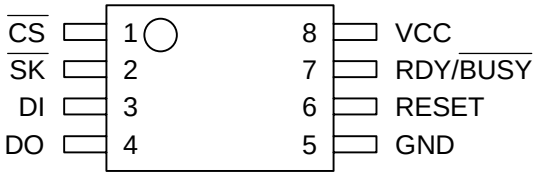
Pin Arrangement

AK6480CF



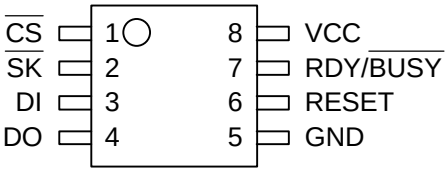
8pin SOP

AK6480CM/81CM



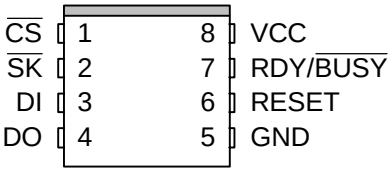
8pin SSOP

AK6480CH/81CH



8pin MSOP

AK6480CL



8pin SON

■ Pin Function

Pin name	Functions
$\overline{CS}$	Chip Select input
$\overline{SK}$	Serial Clock input
DI	Serial Data input
DO	Serial Data output
RESET	RESET input
RDY/$\overline{BUSY}$	RDY/$\overline{BUSY}$ output
VCC	Power Supply
GND	Ground

■ Pin Description

$\overline{\text{CS}}$ (Chip Select)
When $\overline{\text{SK}}$ is high level and $\overline{\text{CS}}$ is changed from high level to low level, AK6480C/81C can receive the instructions. $\overline{\text{CS}}$ should be kept low level while receiving op-code, address and data and while outputting data. If $\overline{\text{CS}}$ is changed to high level during the above period, AK6480C/81C stops the instruction execution. When $\overline{\text{SK}}$ is low and $\overline{\text{CS}}$ is changed from high level to low level, AK6480C/81C will be in status output mode. The $\overline{\text{CS}}$ need not be low level during the automatic write time-out period ($\overline{\text{Busy}}$ status).

$\overline{\text{SK}}$ (Serial Clock)
The $\overline{\text{SK}}$ clock pin is the synchronous clock input for input/output data. At write operation, AK6480C/81C takes in the write data from data input pin (DI) synchronously with rising edge of input pulse of serial clock pin ($\overline{\text{SK}}$). And at read operation, AK6480C/81C takes out the read data to data output pin (DO) synchronously with falling edge of $\overline{\text{SK}}$. The $\overline{\text{SK}}$ clock is not needed during the automatic write time-out period ($\overline{\text{Busy}}$ status), the status output period and when the device isn't selected ($\overline{\text{CS}}$ = high level).

DI (Data Input)
The op-code, address and write data is input to the DI pin.

DO (Data Output)
The DO pin outputs the read data and status signal and will be high impedance except for this timing.

RDY/ $\overline{\text{BUSY}}$ (Ready/ $\overline{\text{Busy}}$ status)
This pin outputs the internal programming status. When the AK6480C/81C is in the automatic write time-out period, this pin outputs the low level ($\overline{\text{Busy}}$ status), and outputs the high level except for this timing.

RESET (Reset)
The AK6480C/81C stops executing the write instruction when the RESET pin is high level. The RESET pin should be low level while the write instruction input period and the page write instruction input period and the automatic write time-out period. If the RESET pin is high level while the automatic write time-out period, the AK6480C/81C stops execution of internal programming and the device returns to ready status. In this case the word data of the specified address will be incomplete. When inputting the new instruction after RESET, the $\overline{\text{CS}}$ pin should be set to high level. The read, write enable and write disable instructions are not affected by RESET pin status.

VCC (Power Supply)

GND (Ground)

Functional Description

The AK6480C/81C has 5 instructions such as READ, WRITE, Page Write, WREN (write enable) and WRDS (write disable). Each instruction is organized by op-code block (8bits), address block (8bits) and data (8bits x 2). When input level of $\overline{SK}$ pin is high level and input level of chip select ($\overline{CS}$) pin is changed from high level to low level, AK6480C/81C can receive the instructions.
When the instructions are executed consecutively, the $\overline{CS}$ pin should be brought to high level for a minimum of 250ns(tCS) between consecutive instruction cycle.

■ Instruction Set For AK6480C

Instruction	Op-Code	Address	Data
WRITE	1 0 1 0 0 1 0 A8	A7 A6 A5 A4 A3 A2 A1 A0	D15 – D0
Page Write	1 0 1 1 0 1 0 A8	A7 A6 A5 A4 A3 A2 A1 A0	D15 – D0
READ	1 0 1 0 1 0 0 A8	A7 A6 A5 A4 A3 A2 A1 A0	D15 – D0
WREN	1 0 1 0 0 0 1 1	X X X X X X X X	
WRDS	1 0 1 0 0 0 0 0	X X X X X X X X	
(WRAL)	1 0 1 0 1 1 1 1	X X X X X X X X	D15 – D0

X: don't care

■ Instruction Set For AK6481C

Instruction	Op-Code	Address	Data
WRITE	1 0 1 0 0 1 0 A0	A1 A2 A3 A4 A5 A6 A7 A8	D0 – D15
Page Write	1 0 1 1 0 1 0 A0	A1 A2 A3 A4 A5 A6 A7 A8	D0 – D15
READ	1 0 1 0 1 0 0 A0	A1 A2 A3 A4 A5 A6 A7 A8	D0 – D15
WREN	1 0 1 0 0 0 1 1	X X X X X X X X	
WRDS	1 0 1 0 0 0 0 0	X X X X X X X X	
(WRAL)	1 0 1 0 1 1 1 1	X X X X X X X X	D0 – D15

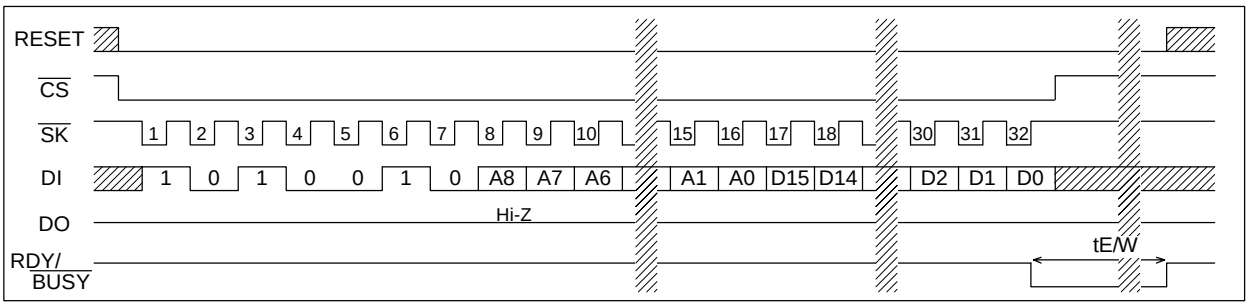
X: don't care

(Note) The WRAL instruction is used for factory function test only. User can't use this instruction.

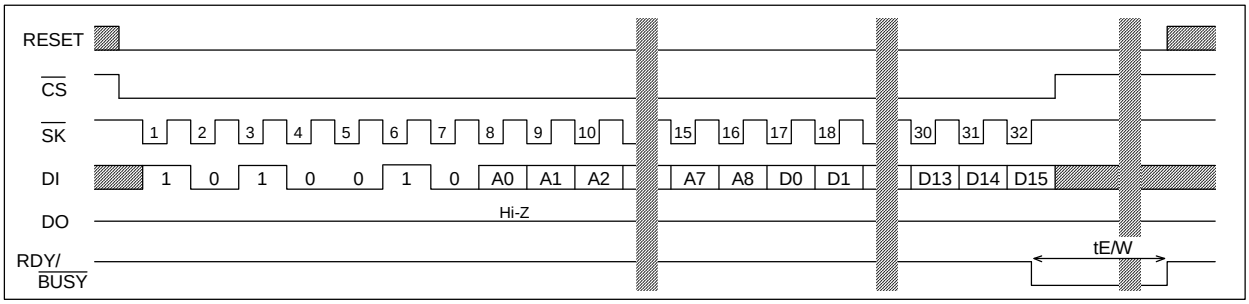
Write

The write instruction is followed by 16 bits of data to be written into the specified address. After the 32nd rising edge of $\overline{SK}$ to read D0 in, the AK6480C/81C will be put into the automatic write time-out period. During the automatic write time-out period ($\overline{Busy}$ status) and while entering write instruction, the RESET pin should be low level. If the RESET pin is set to high level during the automatic write time-out period, the AK6480C/81C stops execution of internal programming and the device returns to ready status. In this case the word data of the specified address will be incomplete. When inputting the new instruction after RESET, the $\overline{CS}$ pin should be set to high level. When the RESET pin is kept at high level, the write is not executed. This becomes write protection function.

The $\overline{CS}$ pin need not be high level during automatic write time-out period ($\overline{Busy}$ status).



WRITE (AK6480C)



WRITE (AK6481C)

Page Write

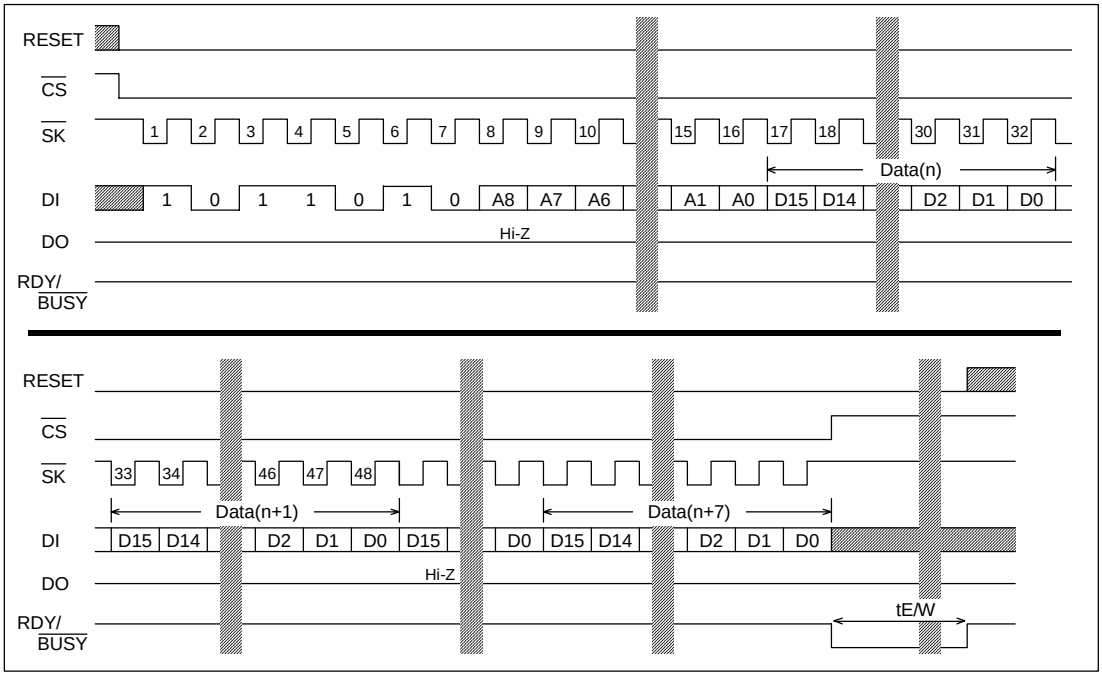
AK6480C/81C has Page Write mode, which can write the data within 8 words with one programming cycle. The input data sent to the shift register within 8 words. After the instruction input, the internal programming cycle starts when $\overline{CS}$ pin changes low to high. After the instructions are inputted, $\overline{CS}$ pin should change low to high after the last data bit (D0, AK6481C: D15) inputs and before next SCK clock rises. Page Write function can start only at this timing.

After the receipt of each word, the three lower order address pointer bits internally incremented by one. The higher order seven bits of the word address remains constant. When the highest address is reached "XX XXXX X111", the address counter rolls over to address "XX XXXX X000" allowing the page write cycle to be continued indefinitely.

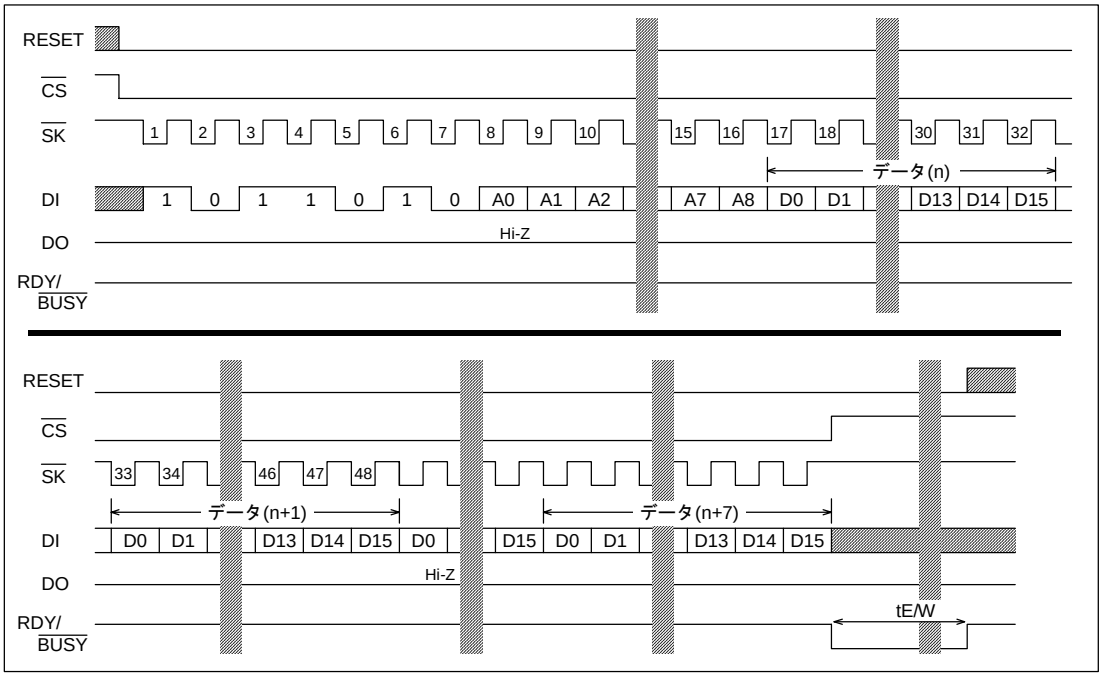
If AK6480C/81C is transmitted more than 8 words, the address counter will "roll over" and the previously written data will be overwritten. When AK6480C/81C is transmitted 10 words, ninth word will be overwritten to first word, and tenth word will be overwritten to second word.

During the automatic write time-out period ($\overline{Busy}$ status) and while entering Page Write

instruction, the RESET pin should be low level. If the RESET pin is set to high level during the automatic write time-out period, the AK6480C/81C stops execution of internal programming and the device returns to ready status. In this case the word data of the specified address will be incomplete. When inputting the new instruction after RESET, the $\overline{CS}$ pin should be set to high level. When the RESET pin is kept at high level, the Page Write is not executed. This becomes write protection function.
The $\overline{CS}$ pin need not be high level during automatic write time-out period ($\overline{Busy}$ status).



PAGE WRITE (AK6480C)

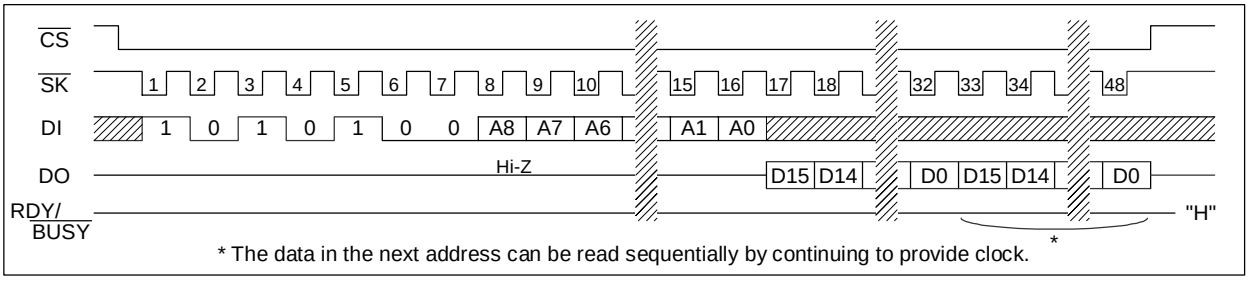


PAGE WRITE (AK6481C)

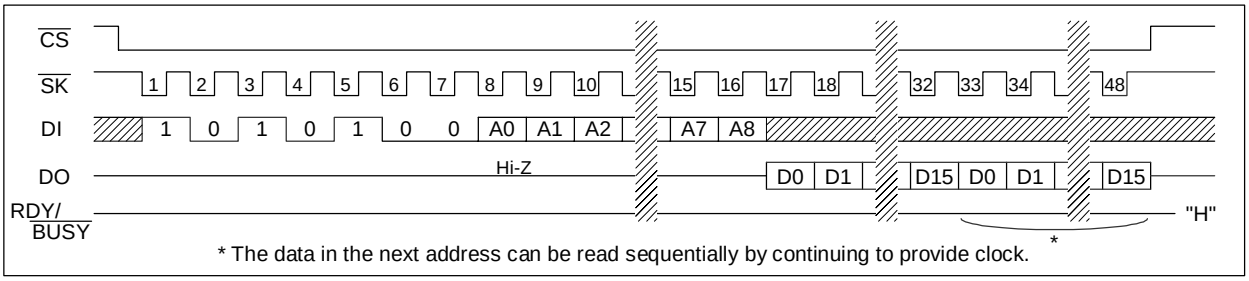
Read

The read instruction is the only instruction which outputs serial data on the DO pin. When the 17th falling edge of $\overline{SK}$ is received , the DO pin will come out of high impedance state and shift out the data from D15 (AK6481C: D0) first in descending order which is located at the address specified in the instruction.

The data in the next address can be read sequentially by continuing to provide clock. The address automatically cycles to the next higher address after the 16bit data shifted out. When the highest address is reached (A8-A0 : 1 1111 1111), the address counter rolls over to address (A8-A0 : 0 0000 0000) allowing the read cycle to be continued indefinitely.



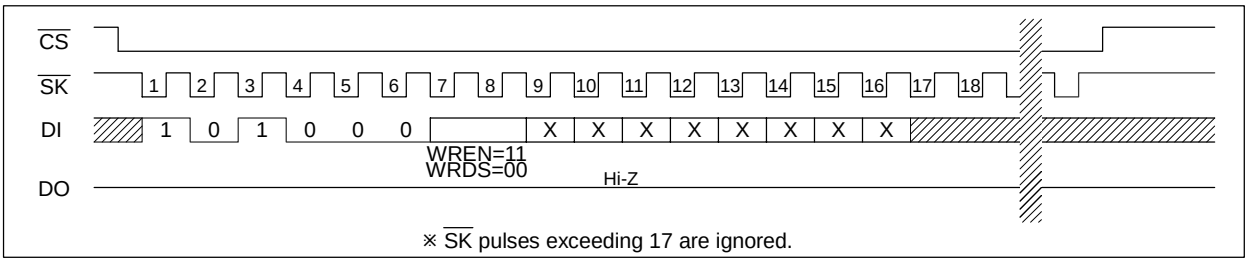
READ (AK6480C)



READ (AK6481C)

WREN / WRDS (Write Enable and Write Disable)

When VCC is applied to the part, it powers up in the programming disable (WRDS) state. Programming must be preceded by a programming enable (WREN) instruction. Programming remains enabled until a programming disable (WRDS) instruction is executed or VCC is removed from the part. The programming disable instruction is provided to protect against accidental data disturb. Execution of a read instruction is not affected by both WREN and WRDS instructions.



WREN / WRDS

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Power Supply	VCC	-0.6	+6.5	V
All Input Voltages with Respect to Ground	VIO	-0.6	VCC+0.6	V
Ambient storage temperature	Tst	-65	+150	°C

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

Recommended Operating Condition

Parameter	Symbol	Min.	Max.	Unit
Power Supply	VCC	1.8	5.5	V
Ambient Operating Temperature	Ta	-40	+85	°C

Electrical Characteristics

(1) D.C. ELECTRICAL CHARACTERISTICS

(1.8V ≤ VCC ≤ 5.5V, -40°C ≤ Ta ≤ 85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.	Unit
Current Dissipation (WRITE)	ICC1	VCC=5.5V,tSKP=200ns *1		2.5	mA
	ICC2	VCC=2.5V,tSKP=400ns *1		2.0	mA
	ICC3	VCC=1.8V,tSKP=1.0μs *1		1.5	mA
Current Dissipation (READ,WREN, WRDS)	ICC4	VCC=5.5V,tSKP=200ns *1		1.0	mA
	ICC5	VCC=2.5V,tSKP=400ns *1		0.2	mA
	ICC6	VCC=1.8V,tSKP=1.0μs *1		0.1	mA
Current Dissipation (Standby)	ICCS	VCC=5.5V *2		0.8	μA
Input High Voltage	VIH1	2.5V ≤ VCC ≤ 5.5V	0.7×VCC	VCC+0.5	V
	VIH2	1.8V ≤ VCC < 2.5V	0.8×VCC	VCC+0.5	V
Input Low Voltage	VIL1	2.5V ≤ VCC ≤ 5.5V	0	0.3×VCC	V
	VIL2	1.8V ≤ VCC < 2.5V	0	0.2×VCC	V
Output High Voltage	VOH1	2.5V ≤ VCC ≤ 5.5V IOH=-50μA	VCC-0.3		V
	VOH2	1.8V ≤ VCC < 2.5V IOH=-50μA	VCC-0.3		V
Output Low Voltage	VOL1	2.5V ≤ VCC ≤ 5.5V IOL=1.0mA		0.4	V
	VOL2	1.8V ≤ VCC < 2.5V IOL=0.1mA		0.4	V
Input Leakage $\overline{CS}$, $\overline{SK}$,DI,RESET	ILI	VCC=5.5V, VIN=5.5V		±1.0	μA
Output Leakage	ILO	VCC=5.5V VOUT=5.5V, $\overline{CS}$=VCC		±1.0	μA

*1 : VIN=VIH/VIL, DO=RDY/ $\overline{BUSY}$ =Open

*2 : $\overline{CS}$ =VCC, $\overline{SK}$ /DI/RESET=VCC/GND, DO= RDY/ $\overline{BUSY}$ =Open

(2) A.C. ELECTRICAL CHARACTERISTICS

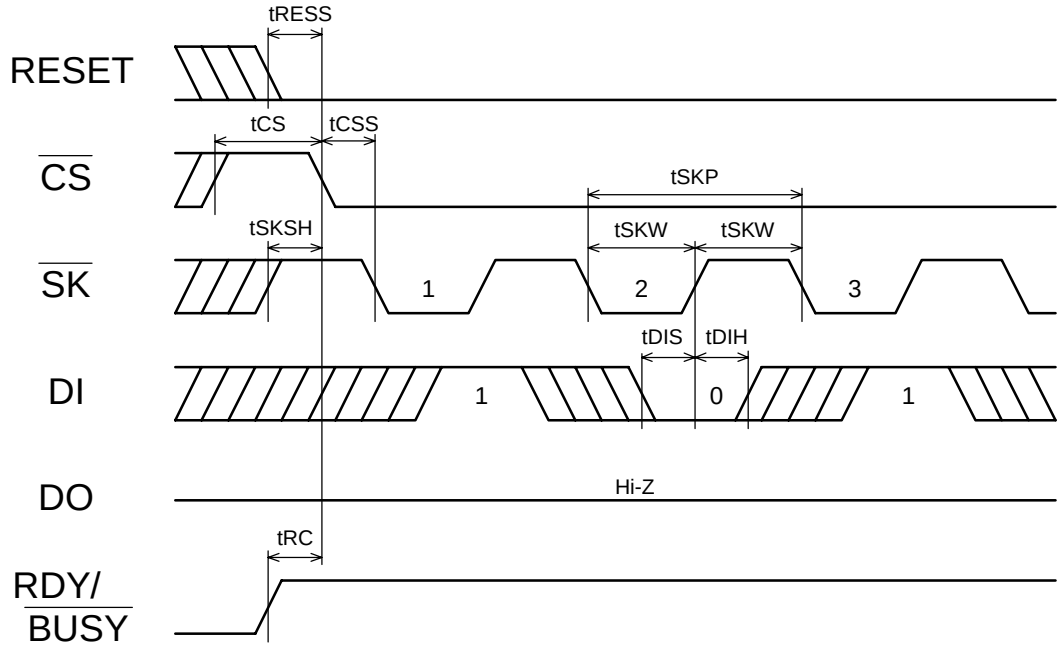
(1.8V ≤ VCC ≤ 5.5V, -40°C ≤ Ta ≤ 85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.	Unit
$\overline{SK}$ Cycle Time	tSKP1	4.5V ≤ VCC ≤ 5.5V	200		ns
	tSKP2	2.5V ≤ VCC < 4.5V	400		ns
	tSKP3	1.8V ≤ VCC < 2.5V	1.0		μs
$\overline{SK}$ Pulse Width	tSKW1	4.5V ≤ VCC ≤ 5.5V	100		ns
	tSKW2	2.5V ≤ VCC < 4.5V	200		ns
	tSKW3	1.8V ≤ VCC < 2.5V	500		ns
$\overline{CS}$ Setup Time	tCSS1	4.5V ≤ VCC ≤ 5.5V	40		ns
	tCSS2	1.8V ≤ VCC < 4.5V	80		ns
$\overline{CS}$ Hold Time	tCSH1	4.5V ≤ VCC ≤ 5.5V	40		ns
	tCSH2	1.8V ≤ VCC < 4.5V	80		ns
$\overline{SK}$ Setup Time	tSKSH/L1	4.5V ≤ VCC ≤ 5.5V	40		ns
	tSKSH/L2	1.8V ≤ VCC < 4.5V	80		ns
RESET Setup Time	tRESS		0		ns
RESET Hold Time	tRESH		0		ns
Data Setup Time	tDIS1	4.5V ≤ VCC ≤ 5.5V	40		ns
	tDIS2	2.5V ≤ VCC < 4.5V	80		ns
	tDIS3	1.8V ≤ VCC < 2.5V	200		ns
Data Hold Time	tDIH1	4.5V ≤ VCC ≤ 5.5V	40		ns
	tDIH2	2.5V ≤ VCC < 4.5V	80		ns
	tDIH3	1.8V ≤ VCC < 2.5V	200		ns
DO pin Output delay	tPD1	4.5V ≤ VCC ≤ 5.5V *3		60	ns
	tPD2	2.5V ≤ VCC < 4.5V *3		150	ns
	tPD3	1.8V ≤ VCC < 2.5V *3		300	ns
RDY/$\overline{BUSY}$ pin Output delay	tPD	CL=100pF		1	μs
Selftimed Programming Time	tE/W			5	ms
Write Recovery Time	tRC		100		ns
Min $\overline{CS}$ High Time	tCS		250		ns
DO High-Z Time	tOZ			500	ns
Endurance *4		5.5V, 25°C, Page Write	1,000,000		E/W cycles / Address

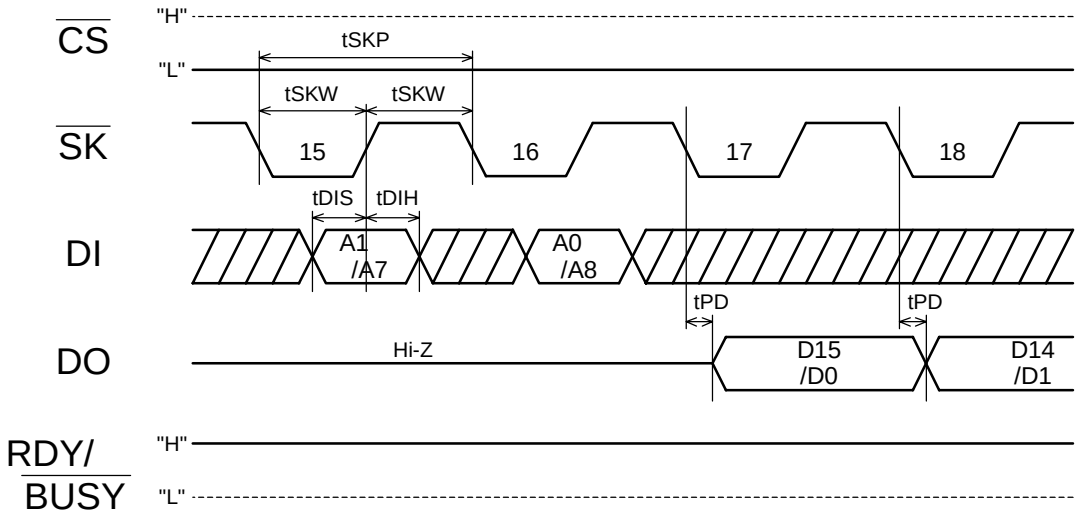
*3 : CL=100pF

*4 : These parameters are not 100% tested. These are the sample value.

Synchronous Data Timing

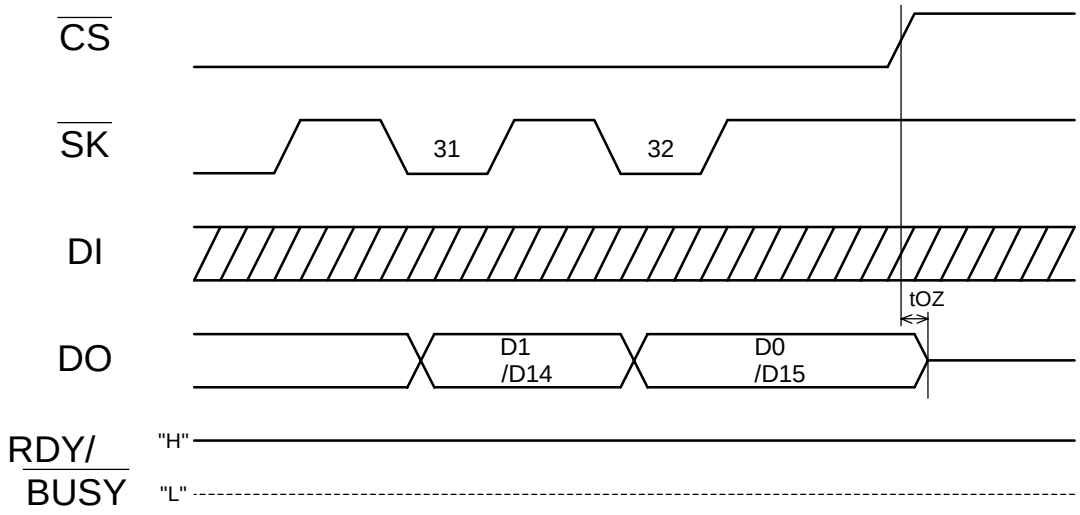


Instruction Input



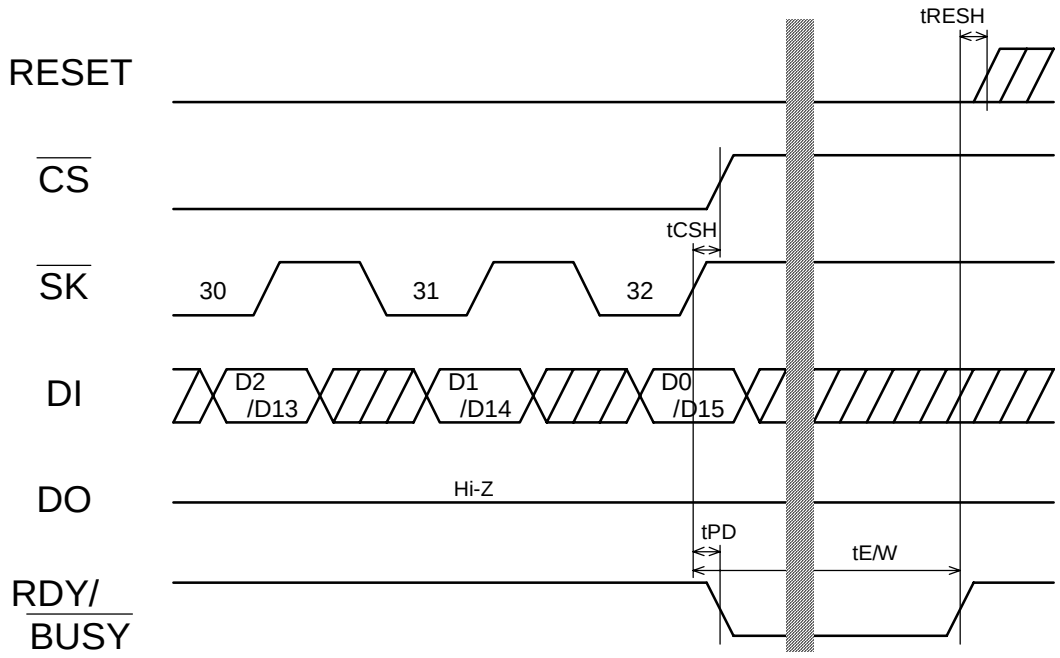
Upper:AK6480C, Lower:AK6481C

Data Output (READ)



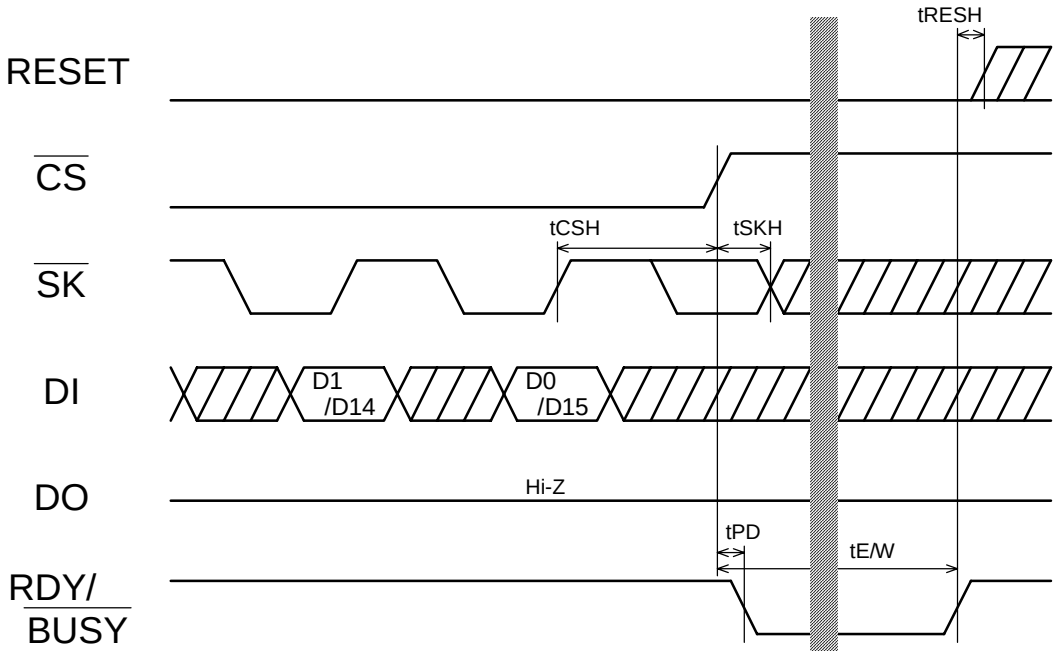
Upper:AK6480C, Lower:AK6481C

Data Output (READ)



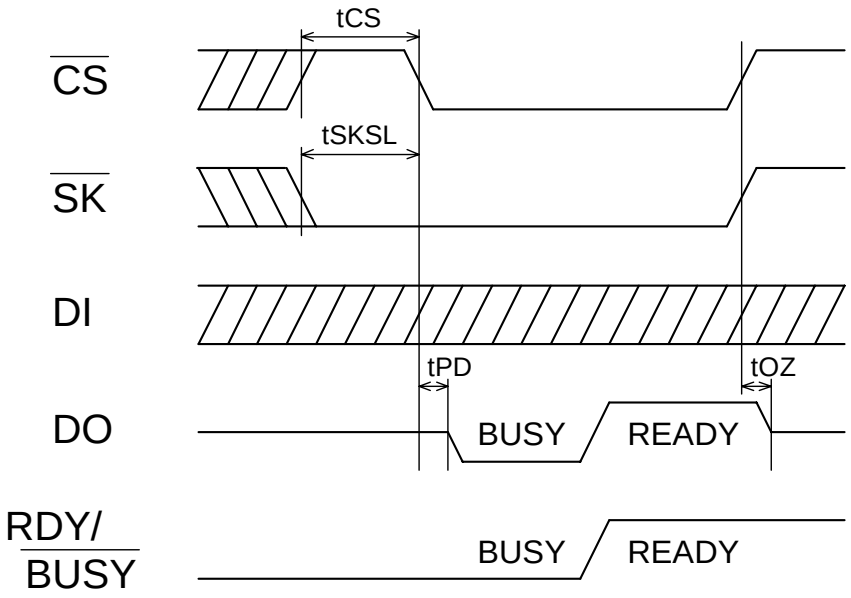
Upper:AK6480C, Lower:AK6481C

WRITE Ready / $\overline{\text{Busy}}$ Signal Output (RDY/ $\overline{\text{BUSY}}$ pin)



Upper:AK6480C, Lower:AK6481C

PAGE WRITE Ready / $\overline{\text{Busy}}$ Signal Output (RDY/ $\overline{\text{BUSY}}$ pin)



Ready/ $\overline{\text{Busy}}$ Signal Output (DO pin)

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