# TC1188/TC1189

## MAX8863/64 Pin Compatible, Low Dropout, 120 mA Linear Regulators

### Features

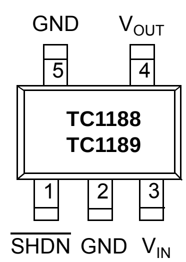
- Input Voltage Range: 2.7 V to 6.0 V
- 120 mA Output Current
- Low Supply Current: 50 µA, (typical)
- Low Dropout Voltage: 110 mV, (typical at 100 mA)
- Fast Turn-On from Shutdown: 140 µsec (typical)
- Low Output Noise
- Over-Current and Over-Temperature Protection
- Low Power Shutdown Mode
- Auto Discharge of Output Capacitor (TC1189)

### Applications

- Battery Powered Systems
- Portable Computers
- Medical Instruments
- Cellular, Cordless Phones
- PDAs
- Pagers

### Package Type

**5-Pin SOT-23A**




**NOTE:** 5-Pin SOT-23A is equivalent to the EIAJ (SC-74A)

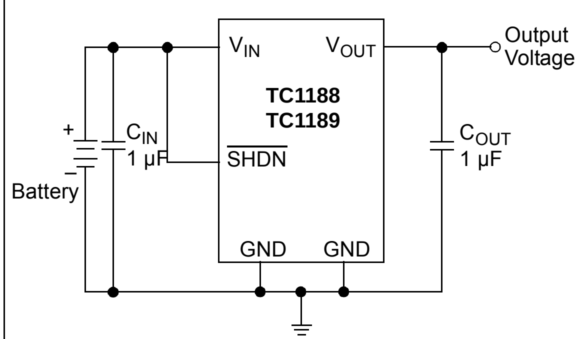
### General Description

The TC1188 and TC1189 are fixed output, low dropout linear regulators that operate from a 2.7V to 6.0V input voltage source. The output is capable of delivering up to 120 mA while consuming only 50 µA of quiescent current. The low dropout voltage, 120 mV, make the TC1188 and TC1189 good choices for battery powered applications. Integrated over-current and over-temperature protection features provide for a fault tolerant solution.

The TC1189 includes an output voltage auto discharge feature. When shutdown, the TC1189 will automatically discharge the output voltage using an internal N-Channel MOSFET switch.

Fixed output voltage options for the TC1188/TC1189 are: 1.80V, 2.80V, 2.84V and 3.15V. Both the TC1188 and TC1189 are available in SOT23-5 packages.

### Typical Application Circuit



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings*

Input Voltage ........................................................6.5V
Output Short-Circuit Duration.............................Infinite
Output Voltage........................... (-0.3V) to ($V_{IN}$ + 0.3V)
Maximum Voltage On Any Pin.... (-0.3V) to ($V_{IN}$ +0.3V)
Continuous Power Dissipation ($T_A$ = +70°C)
SOT-23-5 (derate 7.1 mW/°C above +70°C)
...................................................................571 mW
Operating Temperature Range...............-40°C to 85°C
Storage Temperature..........................-65°C to +160°C
Lead Temperature (Soldering, 10 Sec.) ........... +300°C

***Notice:** *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### DC SPECIFICATIONS

**Electrical Characteristics:** $V_{IN}$ = +3.6V, GND = 0V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C. **(Note 1)**

| Parameters | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Input Voltage | $V_{IN}$ | $V_{OUT}$+0.5V<br>2.7 | —<br>— | 6.0<br>6.0 | V | $V_{OUT} \geq 2.5V$<br>$V_{OUT}$ = 1.8V **(Note 2)** |
| Output Voltage | $V_{OUT}$ | 3.05 | 3.15 | 3.25 | V | 0 mA ≤ $I_{OUT}$ ≤ 50 mA T |
| | | 2.75 | 2.84 | 2.93 | V | 0 mA ≤ $I_{OUT}$ ≤ 50 mA S |
| | | 2.70 | 2.80 | 2.88 | V | 0 mA ≤ $I_{OUT}$ ≤ 50 mA R |
| | | 1.745 | 1.80 | 1.85 | V | 0 mA ≤ $I_{OUT}$ ≤ 50 mA Q |
| Maximum Output Current | $I_{OUT}$ | 120 | — | — | mA | |
| Current Limit | $I_{LIM}$ | — | 280 | — | mA | **Note 3** |
| Input Current | $I_{IN}$ | — | 50 | 90 | µA | $I_{OUT}$ = 0 |
| Dropout Voltage | | — | 1.1 | — | mV | $I_{OUT}$ = 1 mA |
| | | — | 55 | 120 | mV | $I_{OUT}$ = 50 mA |
| | | — | 110 | 240 | mV | $I_{OUT}$ = 100 mA **(Note 4)** |
| Line Regulation | $\Delta V_{LNR}$ | -0.10 | 0.001 | 0.10 | %/V | $V_{IN}$ = $V_{OUT}$ + 0.5V to 6.0V |
| | | — | — | — | %/V | $I_{OUT}$ = 1 mA |
| Load Regulation | $\Delta V_{LDR}$ | — | 0.01 | 0.040 | %/mA | $I_{OUT}$ = 0 mA to 50 mA |
| Output Voltage Noise | | — | 350 | — | $\mu V_{RMS}$ | 10 Hz to 1 MHz, $C_{OUT}$ = 1 MF |
| | | — | 220 | — | $\mu V_{RMS}$ | 10 Hz to 1 MHz $C_{OUT}$ = 100 MF |
| Wake Up Time<br><br>(from Shutdown Mode) | $t_{WK}$ | — | 10 | — | µsec | $V_{IN}$ = 3.6V<br>$C_{IN}$ = 1 µF, $C_{OUT}$ = 1 µF<br>$I_L$ = 30 mA, (See Figure 3-1) |
| Setting Time<br><br>(from Shutdown Mode) | $t_S$ | — | 140 | — | µsec | $V_{IN}$ = 3.6V<br>$C_{IN}$ = 1 µF, $C_{OUT}$ = 1 µF<br>$I_L$ = 30 mA, (See Figure 3-1) |

**Note 1:** Limits are 100% production tested at $T_A$ = +25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.
**2:** Validated by line regulation test.
**3:** Not tested. For design purposes, the current limit should be considered 150 mA minimum to 410 mA maximum.
**4:** The dropout voltage is defined as ($V_{IN}$ – $V_{OUT}$) when $V_{OUT}$ is 100 mV below the value of $V_{OUT}$ for $V_{IN}$ = $V_{OUT}$ +2V.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## DC SPECIFICATIONS (CONTINUED)

**Electrical Characteristics:** $V_{IN}$ = +3.6V, GND = 0V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C. **(Note 1)**

| Parameters | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Shutdown:** | | | | | | |
| $\overline{SHDN}$ Input Threshold | $V_{IH}$ | 2.0 | — | — | V | |
| | $V_{IL}$ | — | — | 0.4 | V | |
| $\overline{SHDN}$ Input Bias Current | $I_{shdn}$ | — | 0.1 | 100 | nA | $V_{SHDN} = V_{IN}$, $T_A$ = +25°C, $T_A = T_{MAX}$ |
| | | — | 50 | — | nA | $V_{SHDN} = V_{IN}$, $T_A$ = +25°C, $T_A = T_{MAX}$ |
| Shutdown Supply Current | $I_{qshdn}$ | — | 0.002 | 1 | µA | $V_{OUT}$ = 0V, $T_A$ = +25°C, $T_A = T_{MAX}$ |
| | | — | 0.02 | — | µA | $V_{OUT}$ = 0V, $T_A$ = +25°C, $T_A = T_{MAX}$ |
| Shutdown to Output Discharge Delay (TC1189) | | — | 1 | — | msec | $C_{OUT}$ = 1 µF, no load at 10% of $V_{OUT}$ |
| **Thermal Protection** | | | | | | |
| Thermal Shutdown Temperature | $T_{SHDN}$ | — | 170 | — | °C | |
| Thermal Shutdown Hysteresis | $\Delta T_{SHDN}$ | — | 20 | — | °C | |

**Note 1:** Limits are 100% production tested at $T_A$ = +25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.

**2:** Validated by line regulation test.

**3:** Not tested. For design purposes, the current limit should be considered 150 mA minimum to 410 mA maximum.

**4:** The dropout voltage is defined as ($V_{IN} – V_{OUT}$) when $V_{OUT}$ is 100 mV below the value of $V_{OUT}$ for $V_{IN} = V_{OUT}$ +2V.

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## 2.0 TYPICAL PERFORMANCE CURVES

| | |
|---|---|
| **Note:** | The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range. |

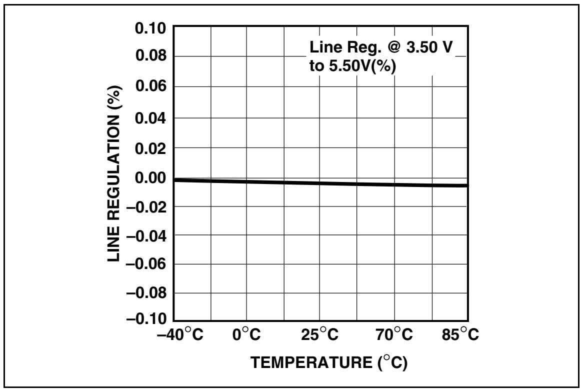


***FIGURE 2-1:*** *Line Regulation vs. Temperature. (TC1188)*

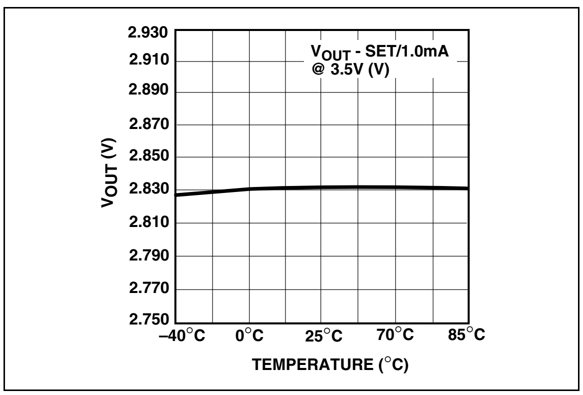


***FIGURE 2-2:*** *Output Voltage vs. Temperature. (TC1188)*

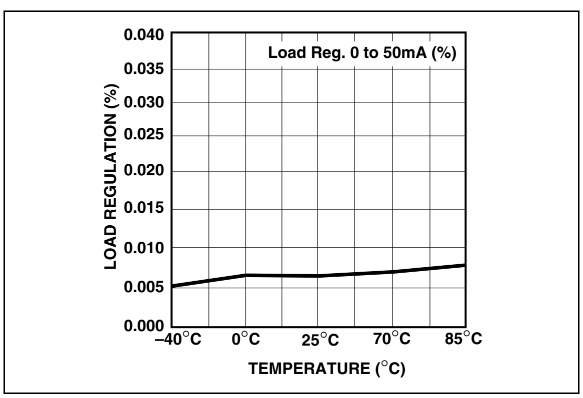


***FIGURE 2-3:*** *Load Regulation vs. Temperature. (TC1188)*

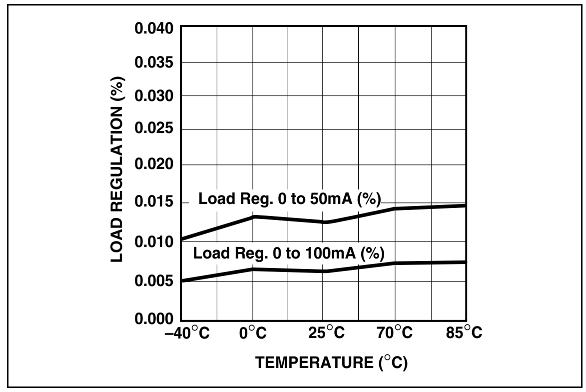


***FIGURE 2-4:*** *Load Regulation vs. Temperature. (TC1188)*

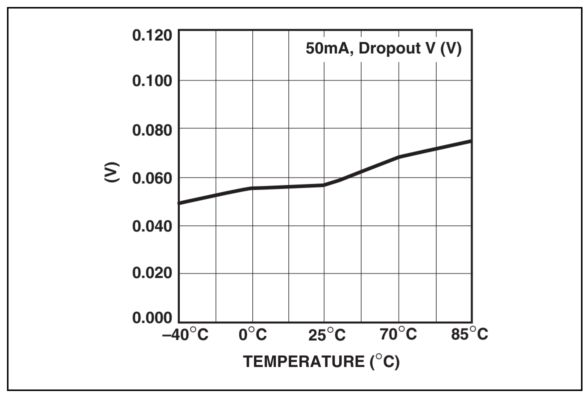


***FIGURE 2-5:*** *Dropout Voltage vs. Temperature. (TC1188)*

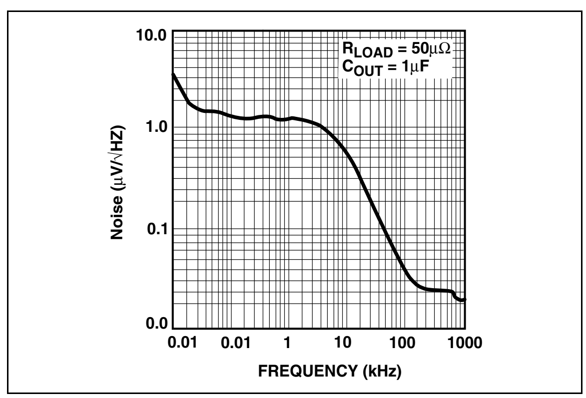


***FIGURE 2-6:*** *Output Noise vs. Frequency. (TC1188)*


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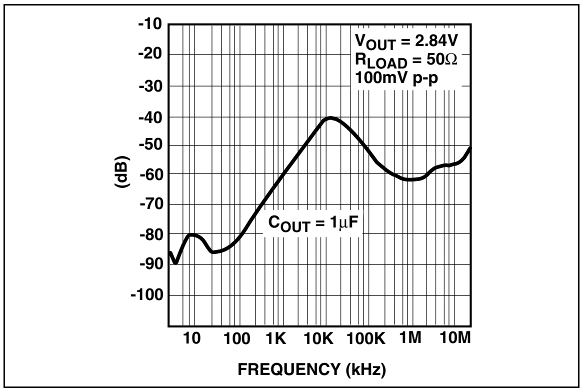


***FIGURE 2-7:*** *Power Supply Rejection Ratio vs. Frequency. (TC1188)*

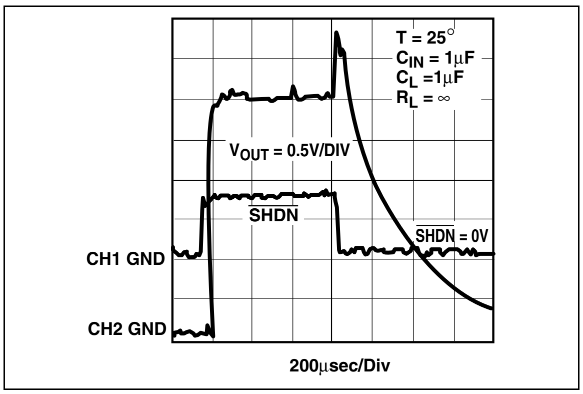


***FIGURE 2-8:*** *TC1189 Shutdown Transient Response.*

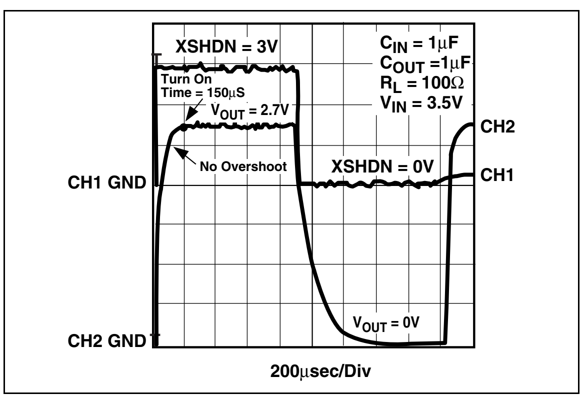


***FIGURE 2-9:*** *TC1189 Shutdown Transient Response.*

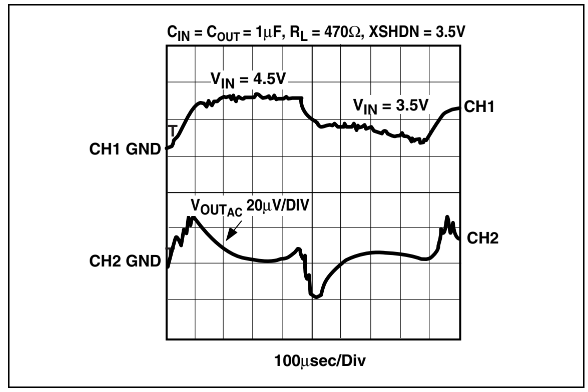


***FIGURE 2-10:*** *TC1189 Line Response.*

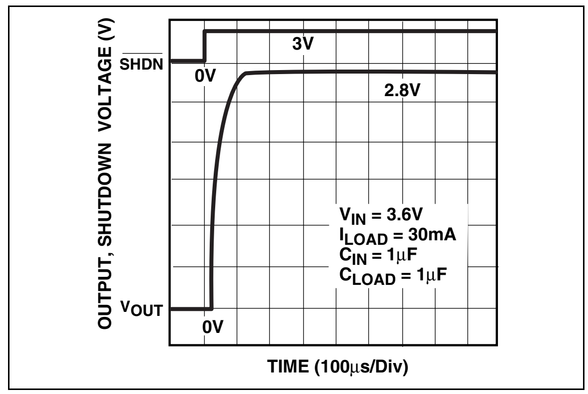


***FIGURE 2-11:*** *Wake-Up Response Time.*

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## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

**TABLE 3-1: PIN FUNCTION TABLE**

| Symbol | Description |
|---|---|
| SHDN | Active Low Shutdown Input. When the $\overline{SHDN}$ input is low (< 0.2V), the quiscent current for the TC1188/TC1189 is reduced to 0.1 nA. When the input voltage to the $\overline{SHDN}$ pin is high (> 2.0V) the output of the TC1188/TC1189 is enabled. For the TC1189 only, the output capacitor is discharged by an internal switch when the $\overline{SHDN}$ is low. |
| GND | Ground. Connect to ground. |
| $V_{IN}$ | Unregulated Input Voltage. The input voltage can range from 2.7V to 6.0V. |
| $V_{OUT}$ | Regulator Output. Sources up to 120 mA. Bypass with a 1 µF, <1 Ω typical ESR capacitor to GND. |
| GND | Connect to GND. |

### 3.1 Detailed Description

The TC1188/TC1189 devices are fixed output, low dropout linear regulators. Utilizing CMOS construction, the internal quiescent current consumed by the regulator is minimized when compared to older bipolar low dropout regulators.

The LDO output voltage is sensed at the non-inverting pin of the internal error amplifier. The internal voltage reference is sensed at the inverting pin of the internal error amplifier. The error amplifier adjusts the gate source voltage of the internal P-channel pass device until the divided down output voltage matches the internal reference voltage. When it does, the LDO output voltage is in regulation.

The $\overline{SHDN}$, when pulled low, is used to turn off the P-Channel MOSFET and lower the internal quiescent current to less than 1 µA maximum. For normal operation, the $\overline{SHDN}$ pin is pulled to a high level. (> 2.0V).

The TC1189 incorporates an internal N-Channel MOSFET, which is used to discharge the output capacitor when shutdown. The TC1188 does not have the internal N-Channel MOSFET, therefore, when the device is shutdown, the output voltage will decrease at a rate which is dependant on the load current.

### 3.2 Turn-On Response

The turn-on response is defined as two separate response categories: Wake-Up Time ($t_{WK}$) and Settling Time ($t_S$).

The TC1188/TC1189 have fast wake-up times (10 µsec typical) when released from shutdown. See Figure 3-1 for the wake-up time, designated as $t_{WK}$. The wake-up time is defined as the time it takes for the output to rise to 2% of the $V_{OUT}$ value after being released from shutdown.

The total turn on response is defined as the Settling Time ($t_S$) (Figure 3-1). Settling Time (inclusive with $t_{WK}$) is defined as the condition when the output is within 2% of its fully enabled value (140 µsec typical) when released from shutdown. The settling time of the output voltage is dependent on load conditions and output capacitance on $V_{OUT}$ (RC response).

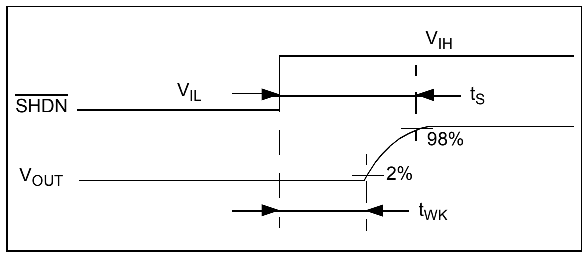


*FIGURE 3-1: Wake-Up Response Time.*

### 3.3 Internal P-Channel Pass Transistor

The Internal P-Channel MOSFET is operated in the linear region to regulate the LDO output voltage. The RDSon of the P-Channel MOSFET is approximately 1.1 Ω, making the LDO able to regulate with little input to output voltage differential, "Low Dropout". Another benefit of using CMOS construction is that the P-Channel MOSFET is a voltage controlled device, so it doesn't consume a fraction of the bias current required of bipolar PNP LDOs.

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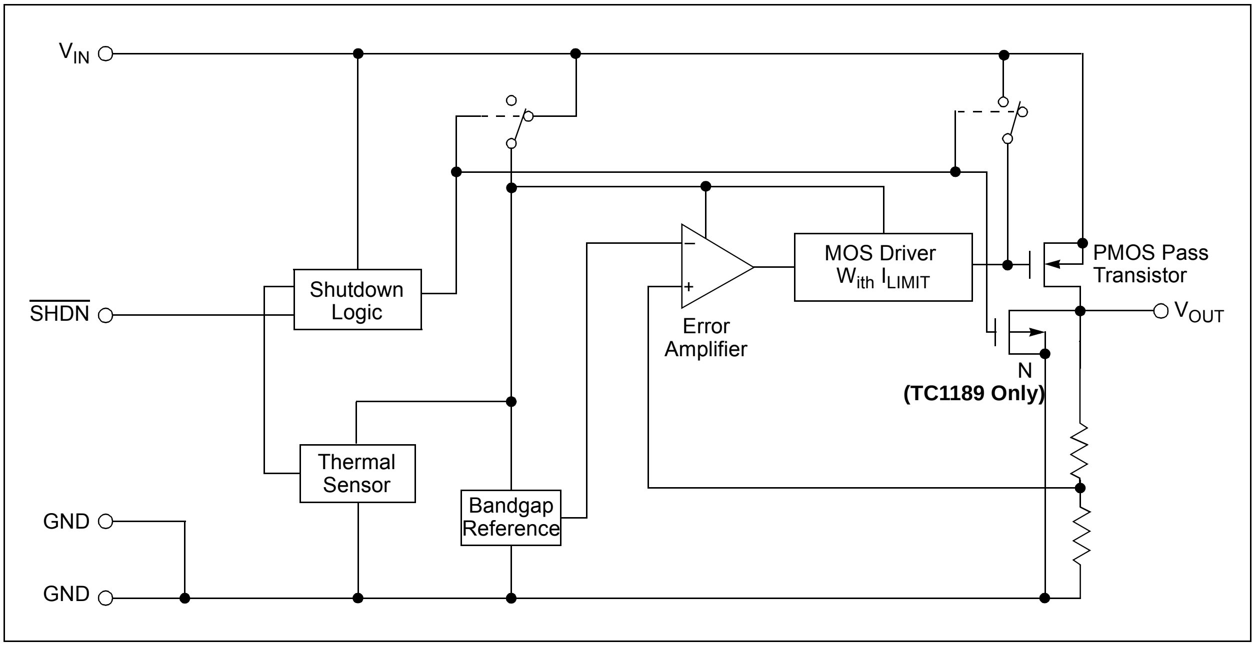


*FIGURE 3-2: Functional Block Diagram.*

## 3.4 Shutdown

The $\overline{SHDN}$ input is used to turn off the LDO P-Channel pass MOSFET and internal bias. When shutdown, the typical quiescent current consumed by the LDO is 0.1 nA. A logic low (< 0.4V) at the $\overline{SHDN}$ input will cause the device to operate in the shutdown mode. A logic high (> 2.0V) at the $\overline{SHDN}$ input will cause the device to operate in the normal mode.

## 3.5 Current Limit

The LDO output current is monitored internal to the TC1188/TC1189. The internal current sense will limit the LDO output current to a typical value of 280 mA. The current limit can range from approximately 50 mA to 410 mA from device to device. The internal current limit protects the device from a continuous output short circuit.

## 3.6 Thermal Overload Protection

Integrated thermal protection circuitry shuts the TC1188/TC1189 off when the internal die temperature exceeds approximately 170°C. The regulator output remains off until the internal die temperature drops to approximately 150°C.

## 3.7 Operating Region and Power Dissipation

The internal power dissipation to the LDO is primarily determined by the input voltage, output voltage and output current. The following equation is used to approximate the worst case for power dissipation:

**EQUATION**

$$P_D = V_{IN(MAX)} - V_{OUT(MIN)} \times I_{LOAD(MAX)}$$

Where:

$P_D$ = Worst case internal power dissipation.

$V_{IN(MAX)}$ = Maximum input voltage.

$V_{OUT(MIN)}$ = Minimum output voltage.

$I_{LOAD(MAX)}$ = Maximum output current.

The maximum power dissipation is a function of the maximum ambient temperature, $T_{A(MAX)}$, the maximum junction temperature, $T_{J(MAX)}$, and the package thermal resistance from junction to air, $\theta_{JA}$. The 5-Pin SOT23A package has a $\theta_{JA}$ of approximately 220°C/Watt.

**EQUATION**

$$P_D = (T_{J(MAX)} - T_{A(MAX)})/\theta_{JA}$$

Where all terms are previously defined.

**EXAMPLE 3-1:**

The previously defined power dissipation equations can be used to ensure that the regulator thermal operation is within limits.

Given:

$V_{IN(MAX)}$ = 3.0V +10%

$V_{OUT(MAX)}$ = 2.7V - 2.5%

$I_{LOAD(MAX)}$ = 40 MA

$T_{J(MAX)}$ = 125°C

$T_{A(MAX)}$ = 55°C

### Find:

1. Actual power dissipation.
2. Maximum allowable dissipation.

### Actual power dissipation:

$$P_D = V_{IN(MAX)} - V_{OUT(MIN)} \times I_{LOAD(MAX)}$$
$$P_D = ((3.0 * 1.1) - (2.7 * 0.975)) * 40 \text{ mA}$$
$$P_D = 26.7 \text{ mWatts}$$

### Maximum allowable power dissipation:

$$P_D = (T_{J(MAX)} - T_{A(MAX)})/\theta_{JA}$$
$$P_{D(MAX)} = (125 - 55) / 220$$
$$P_{D(MAX)} = 318 \text{ mWatts.}$$

In this example, the TC1188/TC1189 dissipates a maximum of 26.7 mW below the allowable limit of 318 mW. In a similar manner, the power dissipation equation, as a function of $V_{IN}$, $V_{OUT}$ and $I_{LOAD,}$ along with the power dissipation equation, as a function of maximum junction temperature, maximum ambient temperature and junction to air thermal resistance, can be used to calculate maximum current and/or maximum input voltage limits.

# 4.0 APPLICATIONS INFORMATION

## 4.1 Input Capacitor

A 1 µF (or larger) capacitor is recommended to bypass the LDO input and lower input impedance for circuit stability when operating from batteries or high impedance sources. The input capacitor can be ceramic, tantalum or aluminum electrolytic. For applications that require low noise and input power supply rejection, low effective series resistance (ESR) ceramic capacitors are recommended over higher ESR electrolytic capacitors. Larger value input capacitors can be used to improve circuit performance.

## 4.2 Output Capacitor

A 1 µF (minimum) capacitor is required from $V_{OUT}$ to ground to ensure circuit stability. The output capacitor should have an ESR greater than 0.1 ohms and less than 2 ohm. Tantalum or aluminum electrolytic capacitors are recommended. Since many aluminum electrolytic capacitors freeze at approximately -30°C, solid tantalums are recommended for applications operating below 25°C.


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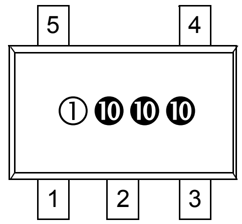
# 5.0 PACKAGING INFORMATION

## 5.1 Package Marking Information




| Part Number | (V) | Code |
|---|---|---|
| TC1188-XECT | 1.80 | G4 |
| TC1188-XECT | 2.80 | G3 |
| TC1188-XECT | 2.84 | G2 |
| TC1188-XECT | 3.15 | G1 |
| | | |
| TC1189-XECT | 1.80 | H4 |
| TC1189-XECT | 2.80 | H3 |
| TC1189-XECT | 2.84 | H2 |
| TC1189-XECT | 3.15 | H1 |

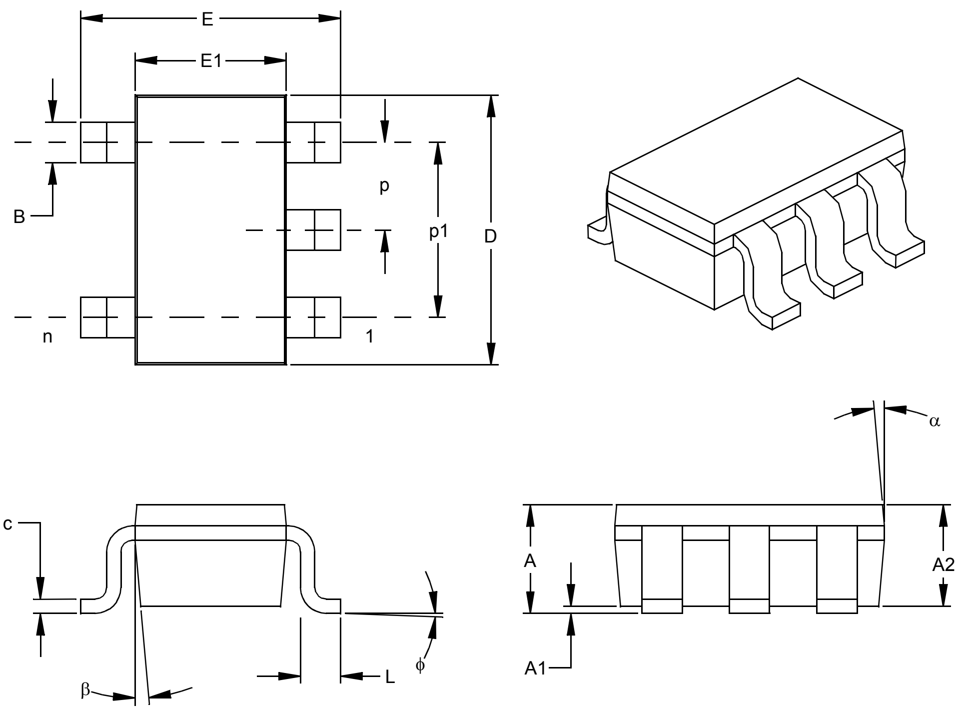
**Legend:**

| | |
|---|---|
| XX...X | Customer-specific information |
| Y | Year code (last digit of calendar year) |
| YY | Year code (last 2 digits of calendar year) |
| WW | Week code (week of January 1 is week '01') |
| NNN | Alphanumeric traceability code |
| (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 5-Lead Plastic Small Outline Transistor (OT) (SOT23)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 5 | | | 5 | |
| Pitch | p | | .038 | | | 0.95 | |
| Outside lead pitch (basic) | p1 | | .075 | | | 1.90 | |
| Overall Height | A | .035 | .046 | .057 | 0.90 | 1.18 | 1.45 |
| Molded Package Thickness | A2 | .035 | .043 | .051 | 0.90 | 1.10 | 1.30 |
| Standoff § | A1 | .000 | .003 | .006 | 0.00 | 0.08 | 0.15 |
| Overall Width | E | .102 | .110 | .118 | 2.60 | 2.80 | 3.00 |
| Molded Package Width | E1 | .059 | .064 | .069 | 1.50 | 1.63 | 1.75 |
| Overall Length | D | .110 | .116 | .122 | 2.80 | 2.95 | 3.10 |
| Foot Length | L | .014 | .018 | .022 | 0.35 | 0.45 | 0.55 |
| Foot Angle | φ | 0 | 5 | 10 | 0 | 5 | 10 |
| Lead Thickness | c | .004 | .006 | .008 | 0.09 | 0.15 | 0.20 |
| Lead Width | B | .014 | .017 | .020 | 0.35 | 0.43 | 0.50 |
| Mold Draft Angle Top | α | 0 | 5 | 10 | 0 | 5 | 10 |
| Mold Draft Angle Bottom | β | 0 | 5 | 10 | 0 | 5 | 10 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-178
Drawing No. C04-091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## REVISION HISTORY

### Revision C (November 2012)

Added a note to the package outline drawing.

**NOTES:**


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2. How does this document meet your hardware and software development needs?

____________________________________________

____________________________________________

3. Do you find the organization of this document easy to follow? If not, why?

____________________________________________

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4. What additions to the document do you think would enhance the structure and subject?

____________________________________________

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5. What deletions from the document could be made without affecting the overall usefulness?

____________________________________________

____________________________________________

6. Is there any incorrect or misleading information (what and where)?

____________________________________________

____________________________________________

7. How would you improve this document?

____________________________________________

____________________________________________


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## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | /XX |
|---|---|---|
| Device | Voltage Output | Package |

| | |
|---|---|
| Device: | TC1188: 100 mA, MAX8863/64 Pin Compatible LDO<br>TC1189: 100 mA, MAX8863/64 Pin Compatible LDO |
| Voltage Output Options: | Q = 1.80V<br>R = 2.80V<br>S = 2.84V<br>T = 3.15V |
| Package: | ECTTR = SOT-23A, 5-Pin (Tape and Reel) |

**Examples:**

a) TC1188QECTTR: 1.80V, 100 mA, MAX8863/64 Pin Compatible LDO
b) TC1188RECTTR: 2.80V, 100 mA, MAX8863/64 Pin Compatible LDO
c) TC1188SECTTR: 2.84V, 100 mA, MAX8863/64 Pin Compatible LDO
d) TC1188TECTTR: 3.15V, 100 mA, MAX8863/64 Pin Compatible LDO

a) TC1189QECTTR: 1.80V, 100 mA, MAX8863/64 Pin Compatible LDO
b) TC1189RECTTR: 2.80V, 100 mA, MAX8863/64 Pin Compatible LDO
c) TC1189SECTTR: 2.84V, 100 mA, MAX8863/64 Pin Compatible LDO
d) TC1189TECTTR: 3.15V, 100 mA, MAX8863/64 Pin Compatible LDO

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Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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