

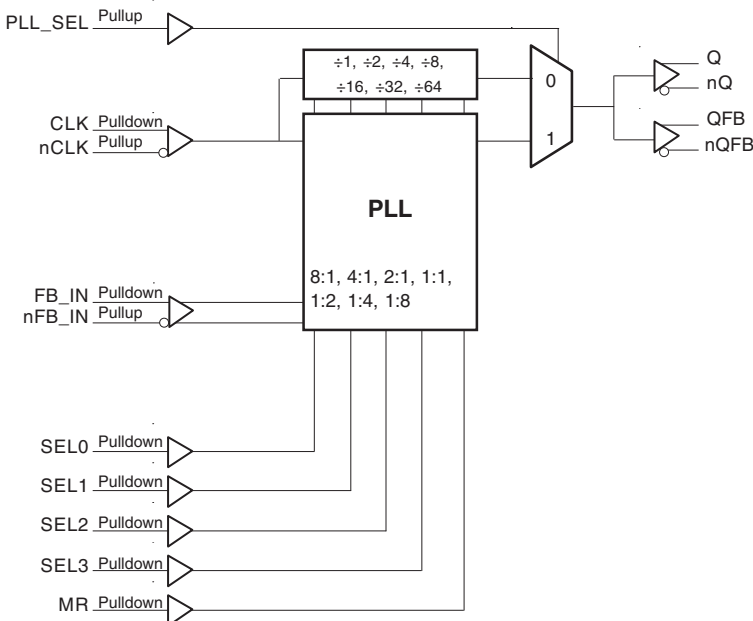
General Description

The 874S02I is a highly versatile 1:1 Differential-to-LVDS Clock Generator and a member of the family of High Performance Clock Solutions from IDT. The 874S02I has a fully integrated PLL and can be configured as a zero delay buffer, multiplier or divider, and has an output frequency range of 62.5MHz to 1GHz. The reference divider, feedback divider and output divider are each programmable, thereby allowing for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8. The external feedback allows the device to achieve “zero delay” between the input clock and the output clocks. The PLL_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.

Features

- One differential LVDS output pair and one differential feedback output pair
- One differential clock input pair
- CLK/nCLK can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL
- Input frequency range: 62.5MHz to 1GHz
- Output frequency range: 62.5MHz to 1GHz
- VCO range: 500MHz - 1GHz
- External feedback for "zero delay" clock regeneration with configurable frequencies
- Programmable dividers allow for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8
- Cycle-to-cycle jitter: 35ps (maximum)
- Static phase offset: ± 100 ps
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free packages

Block Diagram



Pin Assignment

| | | | |
|--------|----|----|---------|
| CLK | 1 | 20 | SEL1 |
| nCLK | 2 | 19 | SEL0 |
| MR | 3 | 18 | VDD |
| nFB_IN | 4 | 17 | PLL_SEL |
| FB_IN | 5 | 16 | VDDA |
| SEL2 | 6 | 15 | SEL3 |
| VDDO | 7 | 14 | GND |
| nQFB | 8 | 13 | Q |
| QFB | 9 | 12 | nQ |
| GND | 10 | 11 | VDDO |

874S02I

20-Lead SOIC

7.5mm x 12.8mm x 2.3mm package body

M Package

Top View

Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---------------|------------------------|--------|----------|---|
| 1 | CLK | Input | Pulldown | Non-inverting differential clock input. |
| 2 | nCLK | Input | Pullup | Inverting differential clock input. |
| 3 | MR | Input | Pulldown | Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Q and QFB to go low and the inverted outputs nQ and nQFB to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTTL interface levels. |
| 4 | nFB_IN | Input | Pullup | Inverting differential feedback input to phase detector for regenerating clocks with "Zero Delay." Connect to pin 8. |
| 5 | FB_IN | Input | Pulldown | Non-inverted differential feedback input to phase detector for regenerating clocks with "Zero Delay." Connect to pin 9. |
| 6, 15, 19, 20 | SEL2, SEL3, SEL0, SEL1 | Input | Pulldown | Determines output divider values in Table 3. LVCMOS / LVTTTL interface levels. |
| 7, 11 | V _{DDO} | Power | | Output supply pins. |
| 8, 9 | nQFB, QFB | Output | | Differential feedback output pair. HSTL interface levels. |
| 10, 14 | GND | Power | | Power supply ground. |
| 12, 13 | nQ, Q | Output | | Differential clock output pair. HSTL interface levels. |
| 16 | V _{DDA} | Power | | Analog supply pin. |
| 17 | PLL_SEL | Input | Pullup | PLL select. Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock. When HIGH, selects PLL. LVCMOS/LVTTTL interface levels. |
| 18 | V _{DD} | Power | | Core supply pin. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 2 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 50 | | kΩ |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 50 | | kΩ |

Function Tables

Table 3A. Control Input Function Table

| Inputs | | | | | Outputs PLL_SEL = 1 PLL Enable Mode |
|--------|------|------|------|----------------------------------|---|
| SEL3 | SEL2 | SEL1 | SEL0 | Reference Frequency Range (MHz)* | Q/nQ |
| 0 | 0 | 0 | 0 | 500 - 1000 | ÷1 |
| 0 | 0 | 0 | 1 | 250 - 500 | ÷1 |
| 0 | 0 | 1 | 0 | 125 - 250 | ÷1 |
| 0 | 0 | 1 | 1 | 62.5 - 125 | ÷1 |
| 0 | 1 | 0 | 0 | 500 - 1000 | ÷2 |
| 0 | 1 | 0 | 1 | 250 - 500 | ÷2 |
| 0 | 1 | 1 | 0 | 125 - 250 | ÷2 |
| 0 | 1 | 1 | 1 | 500 - 1000 | ÷4 |
| 1 | 0 | 0 | 0 | 250 - 500 | ÷4 |
| 1 | 0 | 0 | 1 | 500 - 1000 | ÷8 |
| 1 | 0 | 1 | 0 | 250 - 500 | x2 |
| 1 | 0 | 1 | 1 | 125 - 250 | x2 |
| 1 | 1 | 0 | 0 | 62.5 - 125 | x2 |
| 1 | 1 | 0 | 1 | 125 - 250 | x4 |
| 1 | 1 | 1 | 0 | 62.5 - 125 | x4 |
| 1 | 1 | 1 | 1 | 62.5 - 125 | x8 |

*NOTE: VCO frequency range for all configurations above is 500MHz to 1GHz.

Table 3B. PLL Bypass Function Table

| Inputs | | | | Outputs PLL_SEL = 0 PLL Bypass Mode |
|--------|------|------|------|---|
| SEL3 | SEL2 | SEL1 | SEL0 | Q/nQ |
| 0z | 0 | 0 | 0 | ÷4 |
| 0 | 0 | 0 | 1 | ÷4 |
| 0 | 0 | 1 | 0 | ÷4 |
| 0 | 0 | 1 | 1 | ÷8 |
| 0 | 1 | 0 | 0 | ÷8 |
| 0 | 1 | 0 | 1 | ÷8 |
| 0 | 1 | 1 | 0 | ÷16 |
| 0 | 1 | 1 | 1 | ÷16 |
| 1 | 0 | 0 | 0 | ÷32 |
| 1 | 0 | 0 | 1 | ÷64 |
| 1 | 0 | 1 | 0 | ÷2 |
| 1 | 0 | 1 | 1 | ÷2 |
| 1 | 1 | 0 | 0 | ÷4 |
| 1 | 1 | 0 | 1 | ÷1 |
| 1 | 1 | 1 | 0 | ÷2 |
| 1 | 1 | 1 | 1 | ÷1 |

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|--|--------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_I | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, I_O (LVDS) Continuous Current Surge Current | 10mA 15mA |
| Package Thermal Impedance, θ_{JA} | 64.7°C/W (0 lfpm) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

DC Electrical Characteristics

Table 4A. LVDS Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|-----------------|---------|----------|-------|
| V_{DD} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDA} | Analog Supply Voltage | | $V_{DD} - 0.20$ | 3.3 | V_{DD} | V |
| V_{DDO} | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{DD} | Power Supply Current | | | | 97 | mA |
| I_{DDA} | Analog Supply Current | | | | 20 | mA |
| I_{DDO} | Output Supply Current | | | | 40 | mA |

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|-----------------|--------------------------------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | 2.2 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | MR, SEL[0:3] | $V_{DD} = V_{IN} = 3.465V$ | | 150 | μA |
| | | PLL_SEL | $V_{DD} = V_{IN} = 3.465V$ | | 10 | μA |
| I_{IL} | Input Low Current | MR, SEL[0:3] | $V_{DD} = 3.465V, V_{IN} = 0V$ | -10 | | μA |
| | | PLL_SEL | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150 | | μA |

Table 4C. Differential DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|--------------------------------------|-----------------|--------------------------------|---------|-----------------|---------------|
| I_{IH} | Input High Current | CLK, FB_IN | $V_{DD} = V_{IN} = 3.465V$ | | 150 | μA |
| | | nCLK, nFB_IN | $V_{DD} = V_{IN} = 3.465V$ | | 10 | μA |
| I_{IL} | Input Low Current | CLK, FB_IN | $V_{DD} = 3.465V, V_{IN} = 0V$ | -10 | | μA |
| | | nCLK, nFB_IN | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150 | | μA |
| V_{PP} | Peak-to-Peak Input Voltage; NOTE 1 | | 0.15 | | 1.3 | V |
| V_{CMR} | Common Mode Input Voltage; NOTE 1, 2 | | GND + 0.5 | | $V_{DD} - 0.85$ | V |

 NOTE 1: V_{IL} should not be less than -0.3V.

 NOTE 2: Common mode input voltage is defined as V_{IH} .

Table 4D. LVDS DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|---------|---------|---------|-------|
| V_{OD} | Differential Output Voltage | | 350 | 450 | 550 | mV |
| ΔV_{OD} | V_{OD} Magnitude Change | | | | 50 | mV |
| V_{OS} | Offset Voltage | | 1.20 | 1.33 | 1.45 | V |
| ΔV_{OS} | V_{OS} Magnitude Change | | | | 50 | mV |

Table 5. Input Frequency Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-----------------|-----------------|-------------|---------|---------|-------|
| F_{IN} | Input Frequency | CLK/nCLK | PLL_SEL = 1 | 62.5 | 1000 | MHz |
| | | | PLL_SEL = 0 | | 1000 | MHz |

Table 6. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

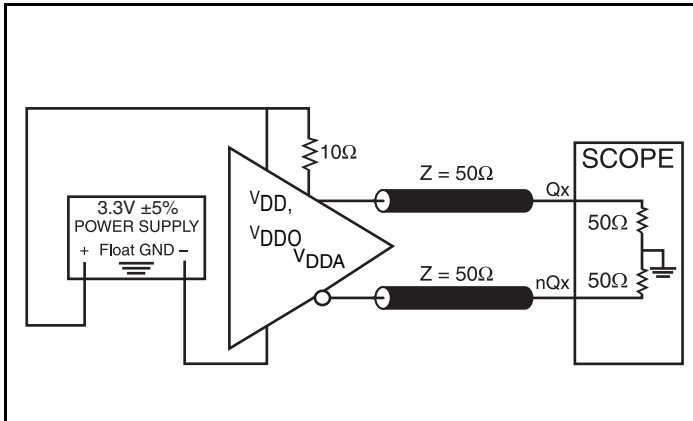
| Parameter | Symbol | Test Conditions | Minimum | Typical | Maximum | Units |
|---------------------|--------------------------------|-----------------|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | | 62.5 | | 1000 | MHz |
| $t_{sk}(\emptyset)$ | Static Phase Offset; NOTE 1, 2 | PLL_SEL = 1 | -100 | | 100 | ps |
| $f_{jit}(cc)$ | Cycle-to-Cycle Jitter; NOTE 2 | | | | 35 | ps |
| t_L | PLL Lock Time | | | | 1 | ms |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 50 | | 250 | ps |
| odc | Output Duty Cycle | | 47 | | 53 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. Device will meet specifications after thermal equilibrium has been reached under these conditions.

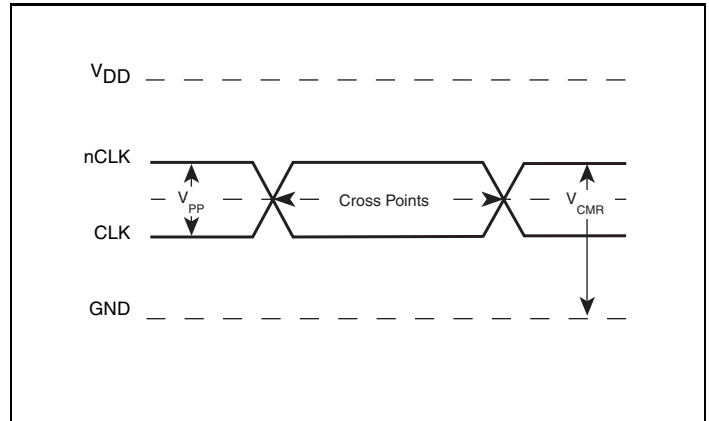
NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal, when the PLL is locked and the input reference frequency is stable.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

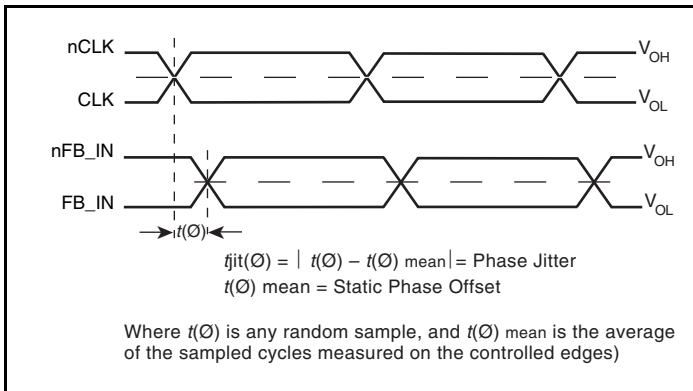
Parameter Measurement Information



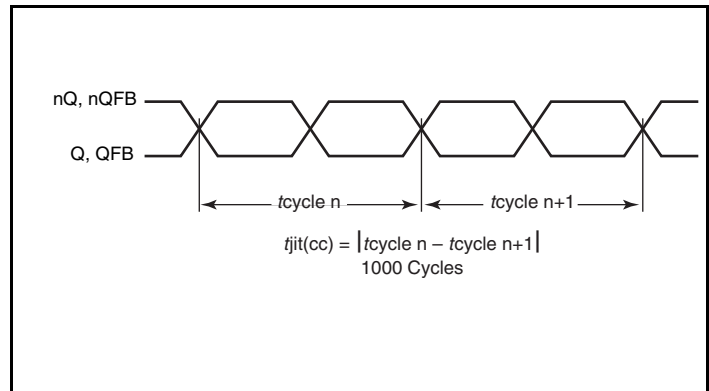
3.3V LVDS Output Load AC Test Circuit



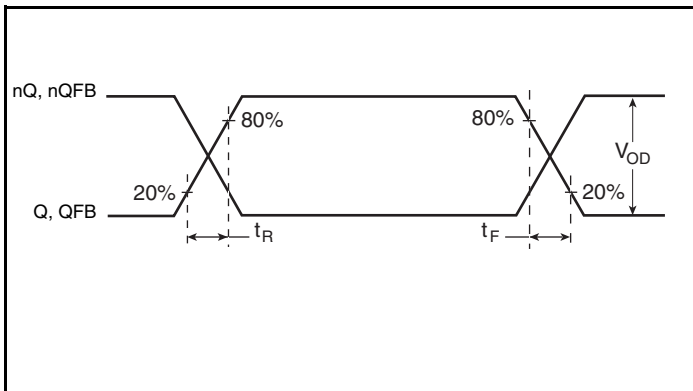
Differential Input Level



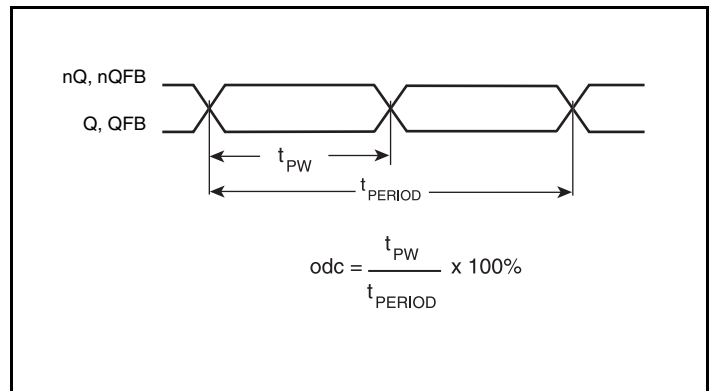
Static Phase Offset



Cycle-to-Cycle Jitter

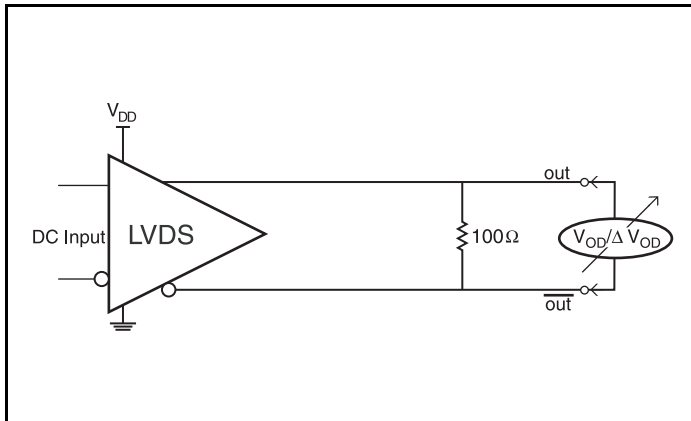


Output Rise/Fall Time

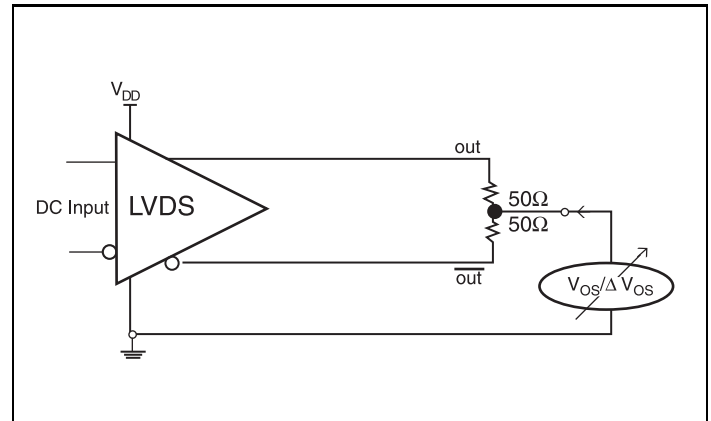


Output Duty Cycle/Pulse Width/Period

Parameter Measurement Information, continued



Differential Output Voltage Setup



Offset Voltage Setup

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

LVC MOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 874S02I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} , V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and $0.01\mu\text{F}$ bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a $10\mu\text{F}$ bypass capacitor be connected to the V_{DDA} pin.

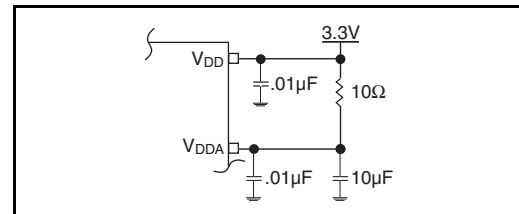


Figure 1. Power Supply Filtering

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how the differential input can be wired to accept single-ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors $R1$, $R2$ and $C1$. This bias circuit should be located as close as possible to the input pin. The ratio of $R1$ and $R2$ might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD} = 3.3\text{V}$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.

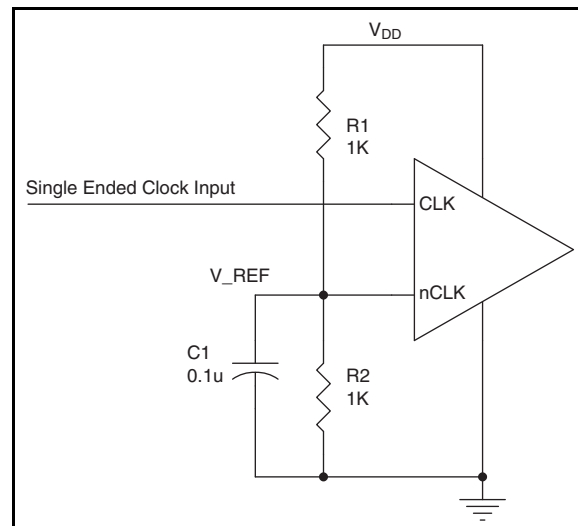
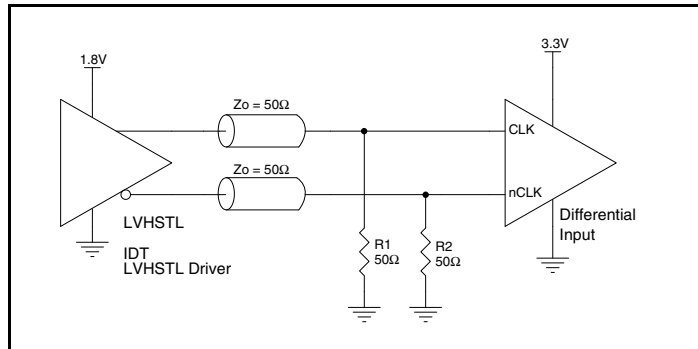


Figure 2. Single-Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver



3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

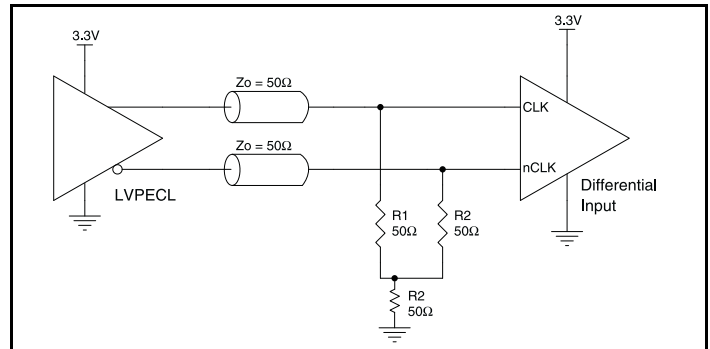


Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

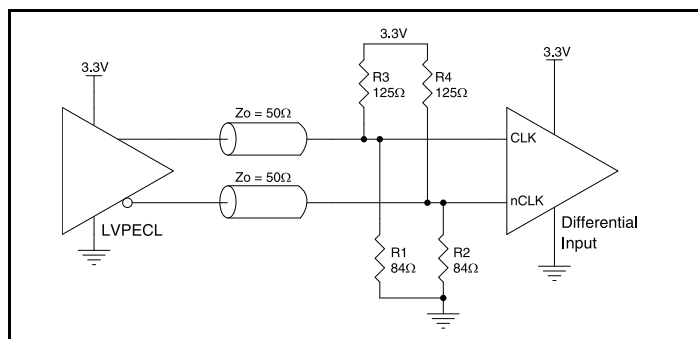


Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

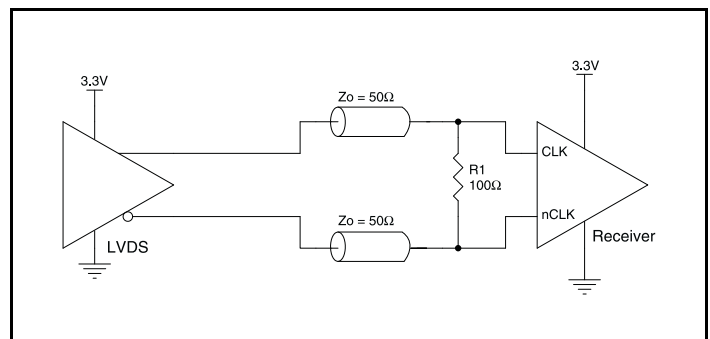


Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

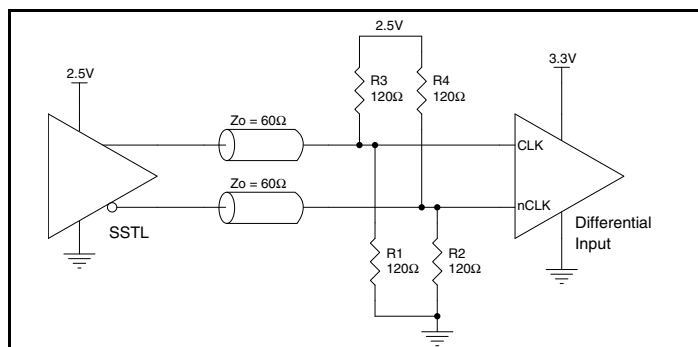


Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 4*. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input.

For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

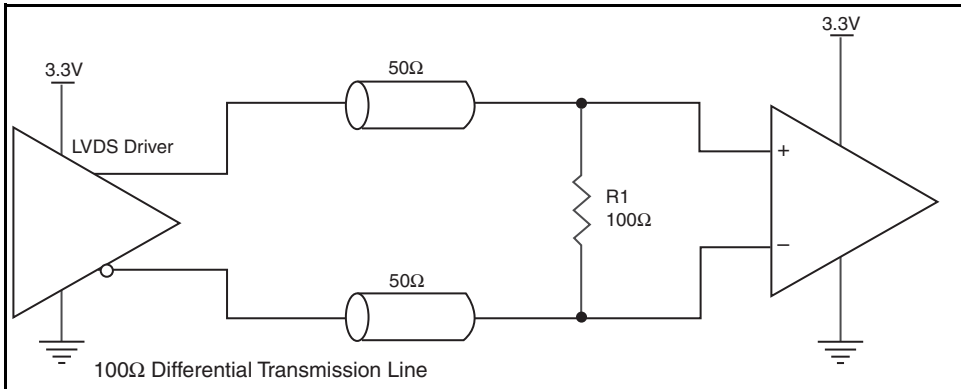


Figure 4. Typical LVDS Driver Termination

Schematic Example

The schematic of the 874S02I layout example is shown in *Figure 5A*. The 874S02I recommended PCB board layout for this example is shown in *Figure 5B*. This layout example is used as a general

guideline. The layout in the actual system will depend on the selected component types and the density of the P.C. board.

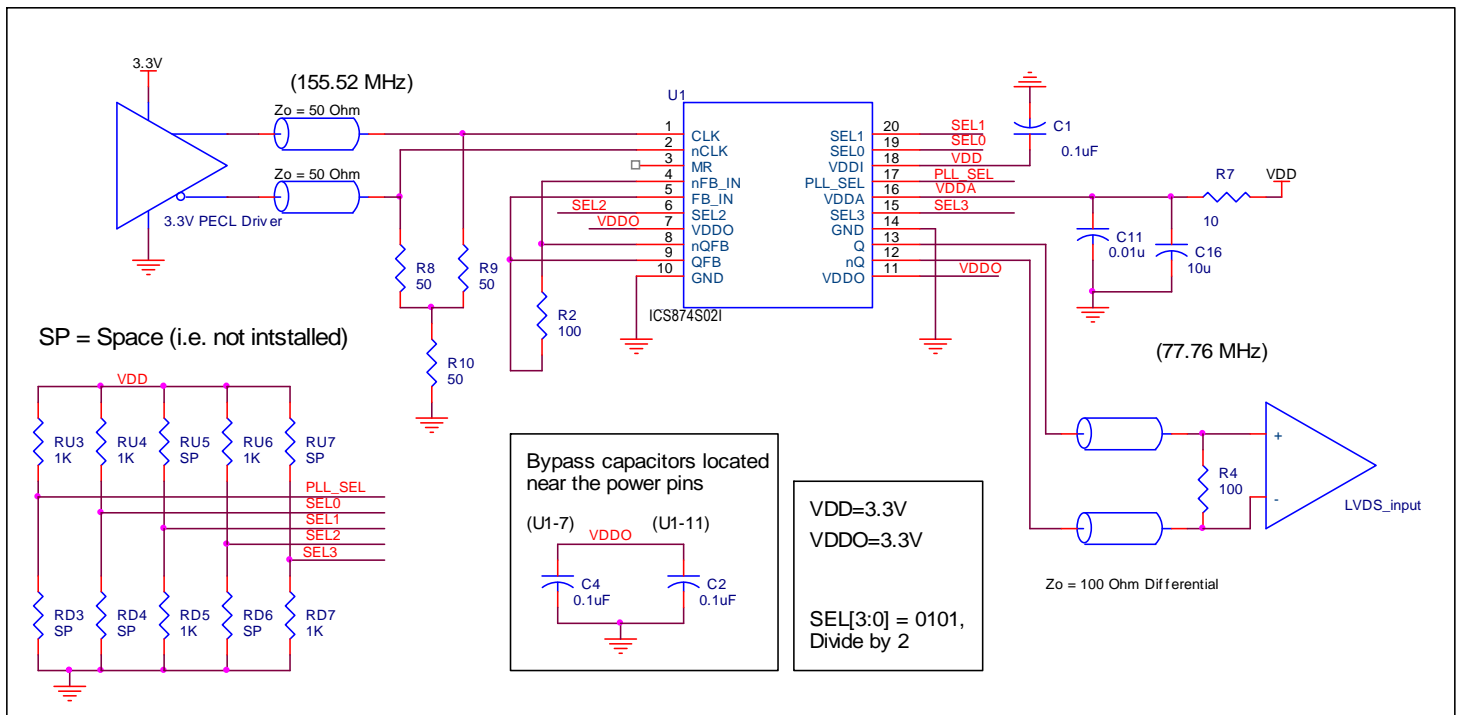


Figure 5A. 874S02I LVDS Zero Delay Buffer Schematic Example

The following component footprints are used in this layout

example.

All the resistors and capacitors are size 0603.

Power and Grounding

Place the decoupling capacitors as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the V_{DDA} pin as possible.

Clock Traces and Termination

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the

trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The 100Ω differential output traces should have the same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The series termination resistors should be located as close to the driver pins as possible.

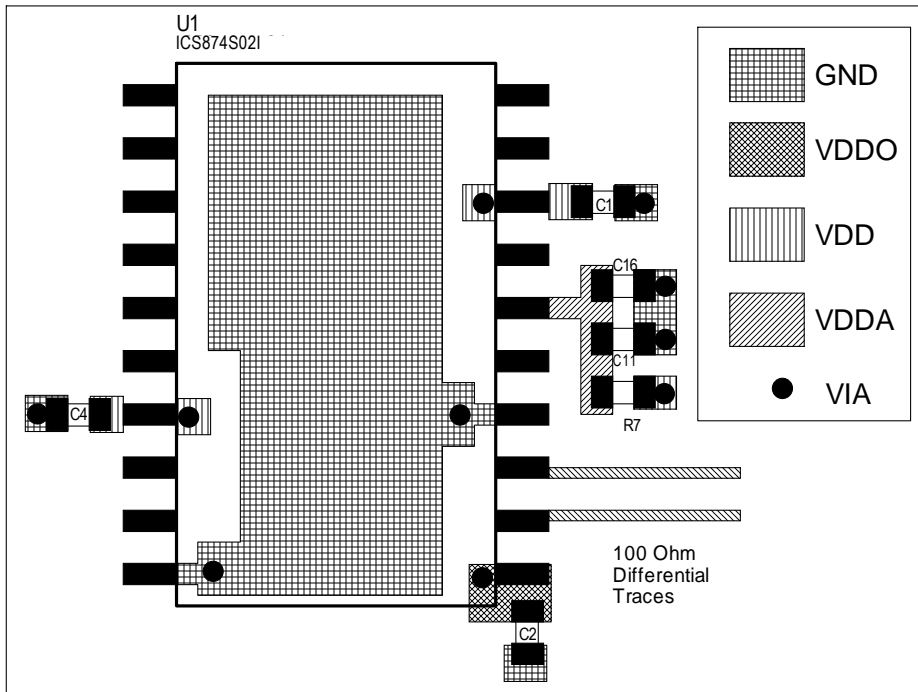


Figure 5B. PCB Board Layout for 874S02I

Power Considerations

This section provides information on power dissipation and junction temperature for the 874S02I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 874S02I is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

- The maximum current at 85°C is as follows:
 $I_{DD_MAX} = 93mA$
 $I_{DDA_MAX} = 19mA$
 $I_{DDO_MAX} = 36mA$
- Power (core)_{MAX} = $V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (93mA + 19mA) = \mathbf{388.08mW}$
- Power (outputs)_{MAX} = $V_{DDO_MAX} * I_{DDO_MAX} = 3.465V * 36mA = \mathbf{124.74mW}$

Total Power_{MAX} = 388.08mW + 124.74mW = 512.82mW

•

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 64.7°C/W per Table 7 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.513W * 64.7^\circ C/W = 118.2^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 7. Thermal Resistance θ_{JA} for 20 Lead SOIC, Forced Convection

| Linear Feet per Minute | θ_{JA} by Velocity | | |
|---|---------------------------|----------|----------|
| | 0 | 200 | 500 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 64.7°C/W | 56.7°C/W | 53.5°C/W |

Reliability Information

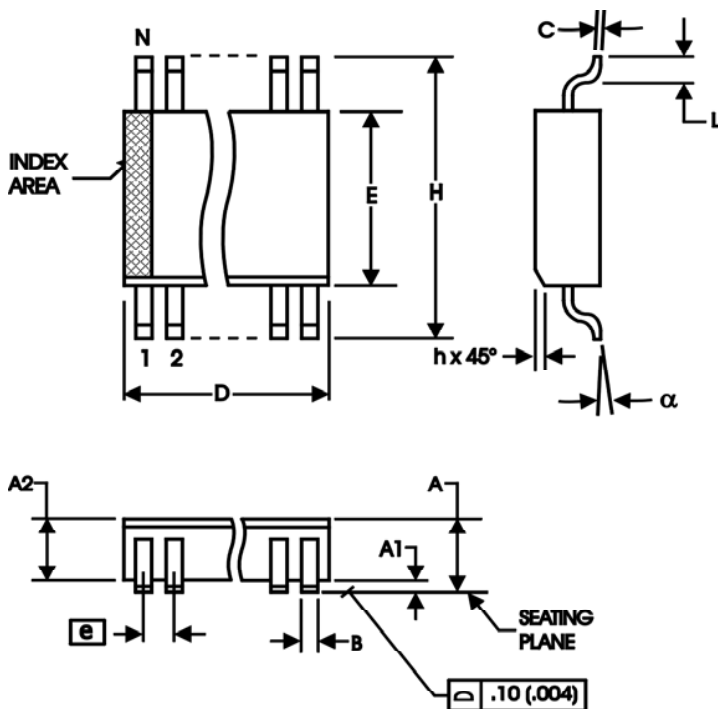
Table 8. θ_{JA} vs. Air Flow Table for a 20 Lead SOIC

| θ_{JA} by Velocity | | | |
|---|----------|----------|----------|
| Linear Feet per Minute | 0 | 200 | 500 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 64.7°C/W | 56.7°C/W | 53.5°C/W |

Transistor Count

The transistor count for 874S02I is: 1358

Package Outline and Package Dimensions

Package Outline - M Suffix for 20 Lead SOIC

Table 9. Package Dimensions for 20 Lead SOIC

| 300 Millimeters All Dimensions in Millimeters | | |
|--|------------|---------|
| Symbol | Minimum | Maximum |
| N | 20 | |
| A | | 2.65 |
| A1 | 0.10 | |
| A2 | 2.05 | 2.55 |
| B | 0.33 | 0.51 |
| C | 0.18 | 0.32 |
| D | 12.60 | 13.00 |
| E | 7.40 | 7.60 |
| e | 1.27 Basic | |
| H | 10.00 | 10.65 |
| h | 0.25 | 0.75 |
| L | 0.40 | 1.27 |
| α | 0° | 8° |

Reference Document: JEDEC Publication 95, MS-013, MS-119

Ordering Information

Table 10. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|----------------|-------------------------|--------------------|---------------|
| 874S02BMILF | ICS874S02BMILF | Lead-Free, 20 Lead SOIC | Tube | -40°C to 85°C |
| 874S02BMILFT | ICS874S02BMILF | Lead-Free, 20 Lead SOIC | Tape & Reel | -40°C to 85°C |

Revision History]

| Revision Date | Description of Change |
|------------------|---|
| January 26, 2016 | <ul style="list-style-type: none"> ▪ Removed ICS from the part number where needed. ▪ General Description - Removed ICS Chip and HiPerClockS. ▪ Ordering Information - removed quantity from tape and reel. ▪ Updated data sheet header and footer. |



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