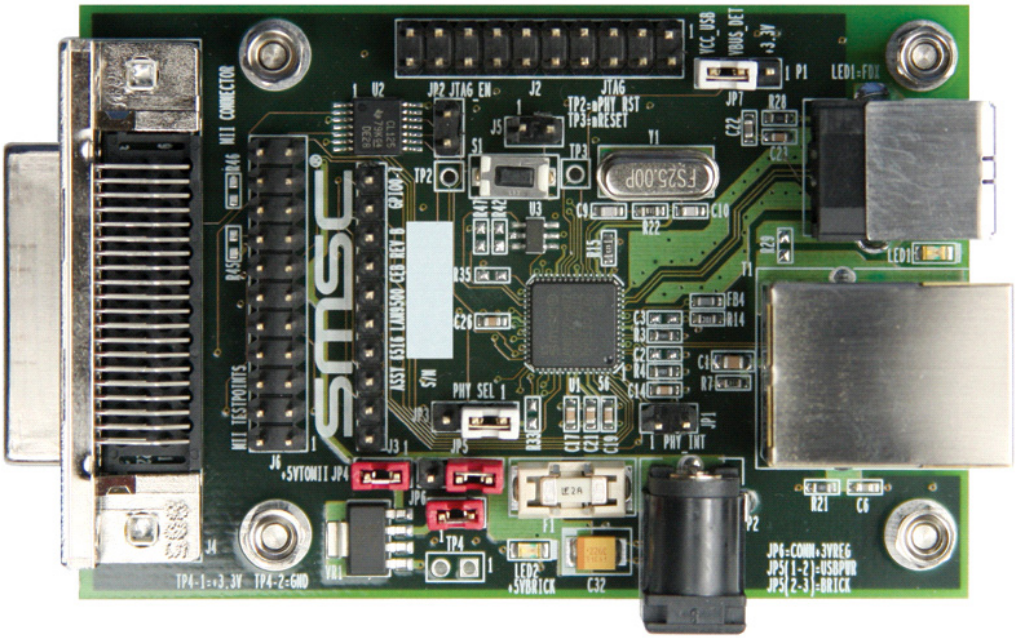
EVB-LAN9500A-MII Evaluation Board User Manual



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1 Introduction

The LAN9500A is a high performance, small form factor solution for USB to 10/100 Ethernet port bridging. With applications ranging from embedded systems, set-top boxes, and PVR's, to USB port replicators, USB to Ethernet adapters, PC docking stations, and test instrumentation, the LAN9500A is targeted as a high performance, low cost USB/Ethernet connectivity solution.

The LAN9500A contains an integrated 10/100 Ethernet PHY, USB PHY, Hi-Speed USB 2.0 device controller, 10/100 Ethernet MAC, TAP controller, EEPROM controller, and a FIFO controller with a total of 30 KB of internal packet buffering. The LAN9500A complies with the IEEE 802.3 (full/half-duplex 10BASE-T and 100BASE-TX) Ethernet protocol and USB 2.0 specification, enabling compatibility with industry standard Fast Ethernet and USB 2.0 applications.

The EVB-LAN9500A-MII is an Evaluation Board (EVB) that utilizes the LAN9500A to provide a fully functional, USB to Ethernet interface. The EVB-LAN9500A-MII provides fully integrated Ethernet and USB ports via the onboard RJ45 and USB Type B connectors. The EVB-LAN9500A-MII can be configured for bus- or self-powered operation and supports internal and external PHY modes. An external PHY may be connected via the onboard 40-pin female MII connector. The onboard 256x8 EEPROM is used to load the EVB-LAN9500A-MII's USB configuration parameters and MAC address.

LAN9500A software drivers are available for Windows XP, Windows Vista, Mac OS X, Linux, and Windows CE. Additional manufacturing and diagnostic tools are available for debugging and external EEPROM configuration. For complete details, refer to the "LAN9500A Software User Manual".

A simplified block diagram of the EVB-LAN9500A-MII can be seen in Figure 1.1.

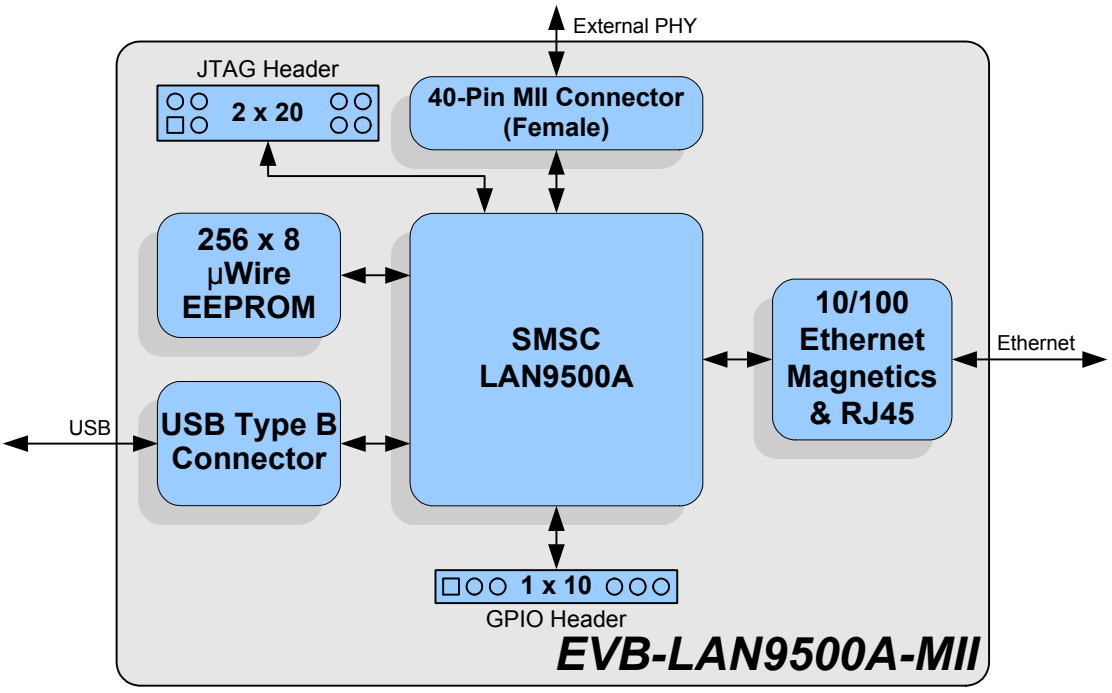

Figure 1.1 EVB-LAN9500A-MII Block Diagram

1.1 References

Concepts and material available in the following documents may be helpful when using the EVB-LAN9500A-MII.

Table 1.1 References

DOCUMENT	LOCATION
SMSC LAN9500A Datasheet	http://www.smsc.com/lan9500a
AN8-13 Suggested Magnetics	http://www.smsc.com/lan9500a
SMSC EVB-LAN9500A-MII Evaluation Board Schematic	http://www.smsc.com/lan9500a
SMSC LAN9500A Software User Manual	http://www.smsc.com/lan9500a

2 Board Details

This section includes the following EVB-LAN9500A-MII board details:

- Configuration
- Mechanicals

2.1 Configuration

The following sub-sections describe the various board features including jumpers, LEDs, test points, and system connections. A top view of the EVB-LAN9500A-MII is shown in Figure 2.1.

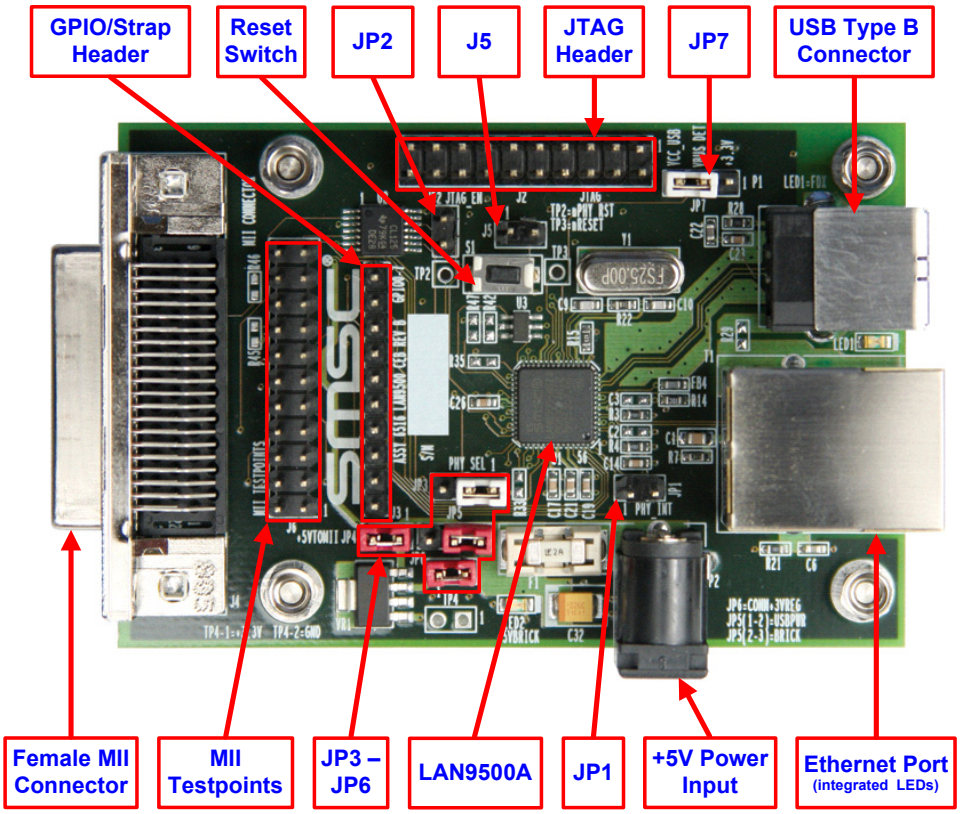

Figure 2.1 EVB-LAN9500A-MII Top View

Note: The EVB-LAN9500A-MII includes a 2A fuse (F1) to protect from overcurrent conditions. If this fuse becomes damaged, it can be replaced with a 2A Littlefuse-154002.

2.1.1 Jumpers

The following table details the jumper definitions and default settings for the EVB-LAN9500A-MII.

Jumper settings may be changed as needed. However, any deviation from the default settings should be approached with care and knowledge of the schematics and datasheet. An incorrect jumper setting may disable the board.

Note: A dashed line in the *Settings* column indicates an installed jumper. All jumper settings are shown in their default state (self-powered, internal Ethernet PHY operation).

Table 2.1 Jumpers

JUMPER	DESCRIPTION	SETTINGS	
JP2	JTAG Header Connect	1 2	**IN:** Connects shared JTAG signals to JTAG header J2 **OUT:** Disconnects shared JTAG signals from JTAG header J2
JP3	Ethernet PHY Select	1 2	Selects external Ethernet PHY
		2---3	Selects internal LAN9500A Ethernet PHY

Table 2.1 Jumpers (continued)

JUMPER	DESCRIPTION	SETTINGS	
JP4	MII Connector +5V Select	1 2	**IN:** Onboard +5V supplied to MII connector pins 1, 20, 21, and 40 **OUT:** Onboard +5V not supplied to MII connector pins 1, 20, 21, and 40
JP5	+5V Power Supply Select (Note 2.1)	1 2	Populate when bus-powered. Connects VCC_USB from the upstream host USB connector to the onboard +3.3V voltage regulator input.
		2---3	Populate when self-powered. Connects +5V from the external power supply to the onboard +3.3V voltage regulator input.
JP6	Onboard +3.3V Regulator Output Connect (Note 2.2)	1---2	**IN:** Connects output of onboard +3.3V regulator to the +3.3V power plane **OUT:** Disconnects output of onboard +3.3V regulator from the +3.3V power plane
JP7	VBUS_DET Input Select (Note 2.1)	1 2	Populate when bus-powered. Connects +3.3V voltage regulator output to VBUS_DET.
		2---3	Populate when self-powered. Connects VCC_USB from the upstream host USB connector to VBUS_DET through a voltage divider and transient filter.

Note 2.1 JP5 and JP7 must be populated indentically.

Note 2.2 This jumper should only be removed if the customer supplies +3.3V from an external source.

2.1.2 LEDs

Table 2.2 LEDs

REFERENCE	COLOR	INDICATION
LED1	Green	Ethernet Full Duplex
LED2	Green	+5V External Power Active **Note:** This LED will not illuminate when in bus-powered mode.
T1	Green	Ethernet Link/Activity **Solid:** Link established **Blinking:** Link activity **OFF:** No link
T1	Yellow	Ethernet Speed **ON:** 100BASE-TX **OFF:** 10BASE-T

2.1.3 Test Points

Table 2.3 Test Points

TEST POINT	DESCRIPTION	CONNECTION
TP2	TDO/nPHY_RST Pin of LAN9500A (unpopulated)	TDO/nPHY_RST
TP3	nRESET Pin of LAN9500A (Unpopulated)	nRESET
TP4	+3.3V Test Point (Unpopulated) (Note 2.3)	**PIN 1:** +3.3V **PIN 2:** GND

Note 2.3 Pin 1 of this test point can be used by the customer to provide an external +3.3V supply. This option may be useful in cases where the customer desires operation in self-powered permanently attached mode. If used in this fashion, **JP6 must be removed**.

2.1.4 System Connections

Table 2.4 System Connections

PLUG/HEADER	DESCRIPTION	PART
P1	USB Type B Right Angle Connector	AMP 292304-1
P2	+5V Power Supply Barrel Connector	CUI PJ-102AH
T1	RJ45 Ethernet Port with Integrated Magnetics & LEDs	Pulse J0011D01B
JP1	1x2 nPHY_INT Header **PIN 1:** nPHY_INT **PIN 2:** Ground **Note:** In internal PHY mode, nPHY_INT is a configurable output. In external PHY mode, nPHY_INT is an input	Adam Tech PH1-2-U-A
J2	2x10 JTAG Header for IEEE 1149.1 Compliant TAP Controller **Note:** Refer Table 2.5 to for a full pin list.	Adam Tech PH2-20-U-A
J3	1x10 GPIO/Strap Header **Note:** Refer Table 2.6 to for a full pin list.	Adam Tech PH1-10-U-A
J4	40-pin Female MII Connector **Note:** This connector follows the standardized MII pinout. Refer to the EVB-LAN9500A-MII schematic for additional information.	AMP 5787170-4

Table 2.4 System Connections (continued)

PLUG/HEADER	DESCRIPTION	PART
J5	1x2 External Reset Header **PIN 1:** GND **PIN 2:** Reset Generator Input	Adam Tech PH1-2-U-A
J6	2x11 MII Test Point Header **Note:** Refer Table 2.7 to for a full pin list	Adam Tech PH2-22-U-A

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Table 2.5 2x10 JTAG Header Pinout

HEADER PIN	DESCRIPTION	HEADER PIN	DESCRIPTION
1	nTRST	11	No Connect
2	Ground	12	Ground
3	TDO	13	No Connect
4	Ground	14	Ground
5	TDI	15	No Connect
6	Ground	16	Ground
7	TMS	17	No Connect
8	Ground	18	Ground
9	TCK	19	No Connect
10	Ground	20	+3.3V

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Table 2.6 1x10 GPIO/Strap Header Pinout

HEADER PIN	DESCRIPTION	HEADER PIN	DESCRIPTION
1	+3.3V	6	TXD0/GPIO4/EEP_DISABLE
2	COL/GPIO0	7	TXD1/GPIO5/RMT_WKP
3	MDIO/GPIO1	8	TXD2/GPIO6/PORT_SWAP
4	MDC/GPIO2	9	TXD3/GPIO7/EEP_SIZE
5	CRS/GPIO3	10	Ground

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Table 2.7 2x11 MII Header Pinout

HEADER PIN	DESCRIPTION	HEADER PIN	DESCRIPTION
1	Ground	12	TXER (Ground)
2	Ground	13	TXCLK
3	MDIO/GPIO1	14	TXEN
4	MDC/GPIO2	15	TXD0/GPIO4/EEP_DISABLE
5	TDI/RXD3	16	TXD1/GPIO5/RMT_WKP
6	TMS/RXD2	17	TXD2/GPIO6/PORT_SWAP
7	TCK/RXD1	18	TXD3/GPIO7/EEP_SIZE
8	nTRST/RXD0	19	COL/GPIO0
9	RXDV	20	CRS/GPIO3
10	RXCLK	21	Ground
11	RXER	22	Ground

2.1.5 Switches

Table 2.8 Switches

SWITCH	DESCRIPTION	FUNCTION
S1	Reset switch	When pressed, triggers a board reset

2.2 Mechanicals

Figure 2.2 details the EVB-LAN9500A-MII mechanical dimensions.

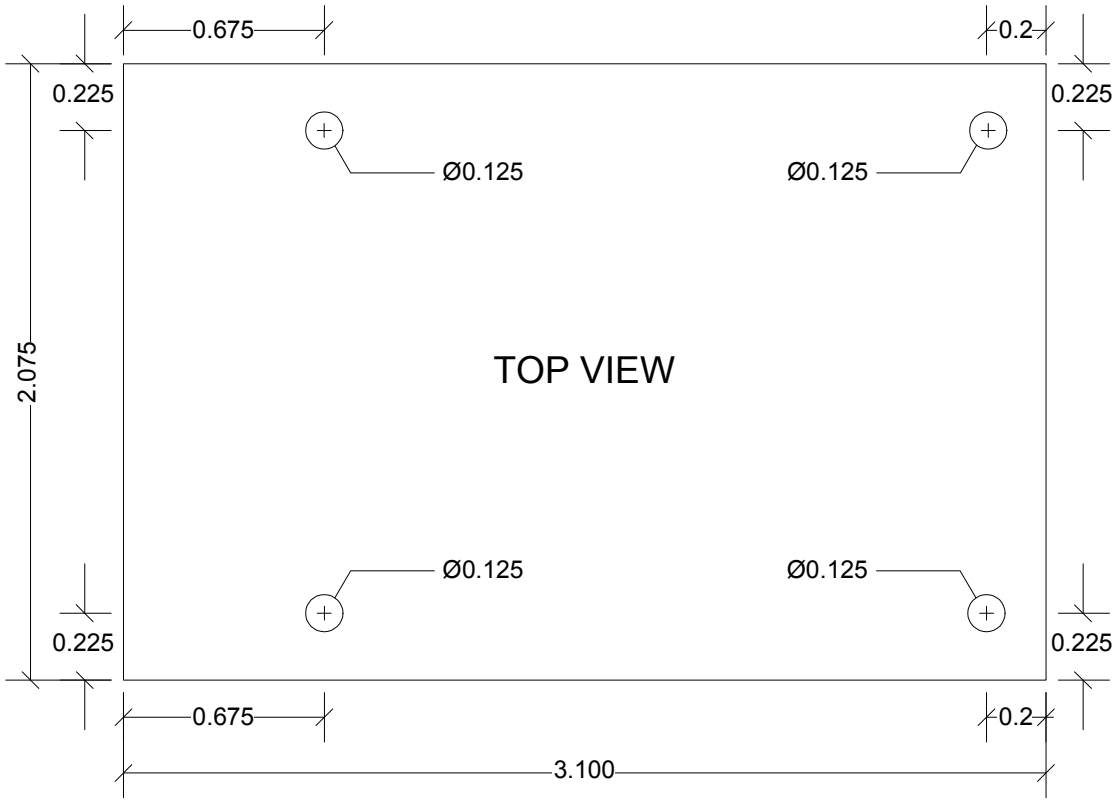

Figure 2.2 EVB-LAN9500A-MII Mechanicals

3 Revision History

Table 3.1 Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.0 (12-04-12)	Document co-branded: Microchip logo added, modification to legal disclaimer.	
Rev. 1.0 (02-02-10)	Initial Release	