Evaluation Boards for DVD-Recordable Audio Codec

EVAL-ADAV801/ADAV803

FEATURES

Full-featured evaluation boards for the ADAV80x
Standalone capability
Optical input and output interface
Filtered analog inputs and outputs
Various linking options
PC software for register programming

GENERAL DESCRIPTION

This data sheet describes the EVAL-ADAV801/ADAV803 evaluation boards. Throughout the data sheet, ADAV80x refers to the ADAV801 and ADAV803 codecs. The evaluation boards allow the user to easily evaluate the functionality and performance of these parts. Access to the control registers of the ADAV80x is made easier with the PC software provided, which can be used to program and read the control registers via the printer port of the PC.

FUNCTIONAL BLOCK DIAGRAM

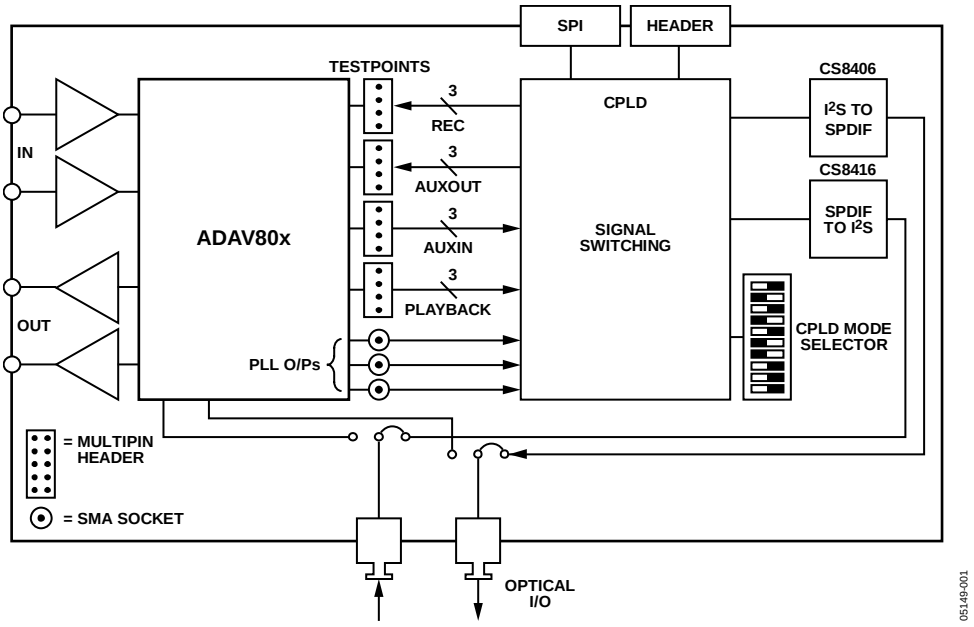

Figure 1.

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EVALUATION BOARD HARDWARE

POWER SUPPLIES

The evaluation boards require a power supply of ±7 V to ±12 V. The voltage supplied is used to power the op amps on the analog input and output sections. The positive supply is regulated to 5 V and is used to supply power to some of the digital sections of the evaluation boards. This supply is also regulated to 3.3 V to power the ADAV80x and some of the digital sections.

Shorted links allow the user to separate the ADAV80x from the on-board supplies for extra experimentation. All the supplies are decoupled with 47 μF tantalum and 0.1 μF ceramic capacitors.

Extensive ground planes are used on these boards to minimize the effect of high frequency noise interference. The two ground planes, AGND and DGND, are connected at one location close to the ADAV80x.

Table 1. Evaluation Board Link Settings

Link	Default	Description
LK1, LK2, LK9, LK19	Not used	These links are not used by default. However, you can make use of these links to measure supply currents on the evaluation board by cutting the track connecting the link pins and placing a current meter in the circuit. Restore normal board operation by inserting a link, if required.
LK3	B	This link enables/disables the crystal oscillator, Y1. In Position A, the crystal oscillator is enabled. In Position B, the crystal oscillator is disabled.
LK4	A	This link selects the clock source for the MCLKI pin. In Position A, the crystal oscillator is selected. In Position B, an external MCLK can be used. In Position C, the MCLKI pin is connected to the ground.
LK5, LK6	In	These links allow the use of the 27 MHz crystal as part of the ADAV80x oscillator circuit.
LK7	A	This link selects the SPDIF source for the optical transmitter, U9. In Position A, the SPDIF source originates from one of the record SPORTs. In Position B, the SPDIF source originates from the SPDIF transmitter in the ADAV80x.
LK8	A	This link determines the SPDIF source for the DIRIN input. Position A selects the optical receiver, U13. Position B selects DITOUT. Position C selects the output of the CS8406 SPDIF transmitter, U16.
LK10	B	This link allows you to buffer the internal reference before using it to bias the DAC output circuitry.
LK11	B	This link selects the reference source for the DAC output circuitry. In Position A, the internal reference is used. In Position B, an external reference can be used.
LK12, LK13, LK14, LK15		These links allow you to choose various routing options for the DAC output circuitry depending on your requirements. See the Analog DAC Section for details.
LK16	Out	This shorted link can be used if you need to measure the ODVDD current. This link removes the pull-up resistors from the I^2C interface, leaving the ADAV80x as the only current draw on the ODVDD supply.
LK17	In	This link controls the buffered output of the MCLKO pin. When the link is connected, a buffered version of MCLKO appears at the MCLKO SMA connector. When the link is disconnected, the output of U6-B is three-stated.
LK20, LK21	B	These links should be in Position B for single-ended DACs.
LK22	In	This link controls the buffered output of the PLL SYSCLK1 to SYSCLK3 pins. When the link is connected, buffered versions of the PLL clocks appear at the CLK0, CLK1, and CLK2 SMA connectors. When the link is disconnected, the output of U6-A is three-stated.
LK23	In	This link connects the MCLKI pin to the CPLD. Depending on the circumstances, the CPLD pin can be an input or an output. When the CPLD pin is an output, LK4 should be disconnected to prevent the oscillator from attempting to drive the MCLKI pin as well.
LK24, LK25	B, A	These links select the serial audio format of the output of the CS8416 SPDIF receiver, U14. In Position A-A, the serial format is left justified, 24-bit data. In Position A-B, the serial format is right justified, 24-bit data. In Position B-A, the serial format is I^2S, 24-bit data. In Position B-B, the serial format is Direct AES3.

Link	Default	Description
LK26, LK27	Both out	These links select the serial audio format of the input of the CS8406 SPDIF transmitter, U16. When LK26 is disconnected and LK27 is disconnected, the serial format is I²S. When LK26 is connected and LK27 is disconnected, the serial format is right justified, 16-bit data. When LK26 is disconnected and LK27 is connected, the serial format is left justified. When LK26 is connected and LK27 is connected, the serial format is right justified, 24-bit data.
LK28	Out	This link selects the SPDIF source to be decoded by U14. When the link is connected, the ADAV80x SPDIF output is used. When the link is disconnected, the SPDIF source originates from the SPDIF receiver, U13.

ANALOG SECTION

The evaluation boards have on-board circuitry for signal conditioning and filtering of the analog inputs and outputs. The connectors for analog inputs and outputs are standard RCA/phono connectors. Link options allow users to bypass some sections of the analog filter circuitry, and through-hole components can be used for experimentation purposes.

Analog ADC Section

The analog ADC section of the evaluation boards contains an LC antialias filter and an ac coupling capacitor for each channel. Additional through-hole footprints are in place but not populated, allowing users to experiment with different component values, if required.

Analog DAC Section

The analog DAC section lets users choose the amount of filtering that is required. The simplest configuration gives an RC filter with a 3 dB point of 46.8 kHz. An active Bessel filter is also available using the link options. Additional through-hole component footprints are in place, but not populated, allowing experimentation with different component values, if required. The link positions and descriptions are listed in Table 2.

Table 2. Optional Evaluation Board Link Settings

Link	Description
LK12, LK13	Position A allows users to add resistors and capacitors to the signal chain for the left DAC. Note that the metal connection under the link (Position B) should be cut to use this option. Position B gives a direct connection from the DAC output pins to the Bessel filter.
LK14, LK15	Position A allows users to add resistors and capacitors to the signal chain for the right DAC. Note that the metal connection under the link (Position B) should be cut to use this option. Position B gives a direct connection from the DAC output pins to the Bessel filter.
LK20, LK21	These links should be in Position B for single-ended output DACs.

DIGITAL SECTION

The evaluation boards can accept a number of digital input sources for control and audio data. A Lattice® CPLD is used to route the digital signals for the desired effect. Various modes are available, such as connecting the ADC digital outputs to the DAC digital inputs to create a loop-back effect connecting the ADC outputs to an SPDIF transmitter connecting an SPDIF receiver to the DAC inputs and so on. These modes make it easier for users to supply audio data from whatever sources are available. The following sections describe these options.

Configuring the CPLD

The CPLD on the evaluation boards is used to switch digital signals among various points on the board. Use the 12-way DIP switch to select the required configuration, as shown in Figure 2.

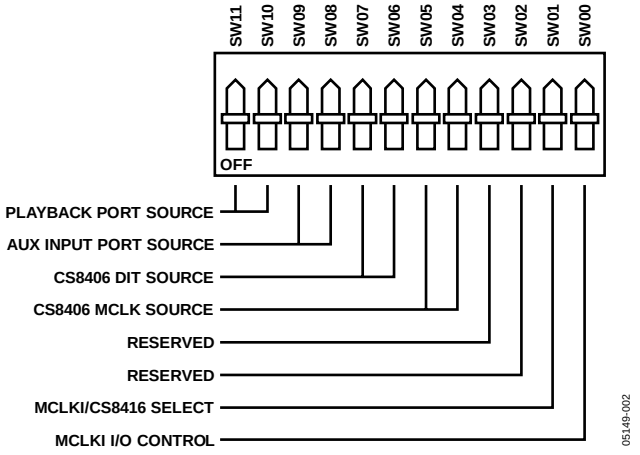

Figure 2. Switches Configuration

Optical Interfaces

The evaluation boards contain a TOSHIBA Toslink optical transmitter (U9, TOTX173) and receiver (U13, TORX173), and associated SPDIF decoder (U14) and encoder (U16) chips. These can be used to transmit and receive audio data from readily available sources such as CD players, audio precision test equipment, and others. The SPDIF decoder, CS8416, and encoder, CS8406, can handle I²S and left- and right-justified data. Table 3 and Table 4 list the appropriate link settings to select a required mode. Figure 3 shows the positions of the links on the evaluation boards.

Table 3. Optical Receiver Links Settings

LK24	LK25	Format
A	A	Left justified, 24-bit data
A	B	Right justified, 24-bit data
B	A	I²S, 24-bit data
B	B	Direct AES3

Table 4. Optical Transmitter Links Settings

LK26	LK27	Format
OUT	OUT	I²S compatible
IN	OUT	Right justified, 16-bit data
OUT	IN	Left justified
IN	IN	Right justified, 24-bit data

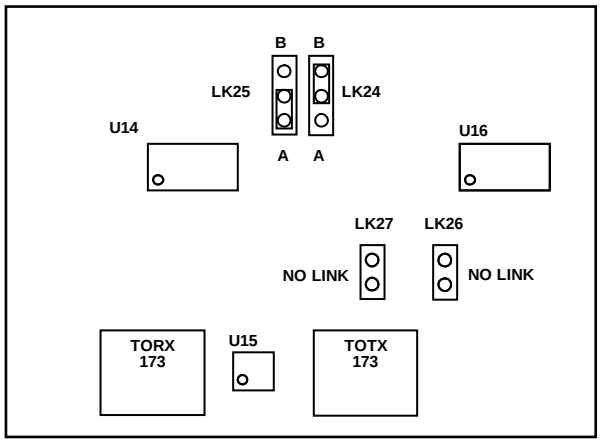

Figure 3. Link Positions

DAC Audio Input

By default, the data from the Toslink optical transmitter is routed to the DIRIN (internal SPDIF receiver) pin of the ADAV80x and to the CPLD via the SPDIF decoder (U14 - CS8416). The CPLD can pass the audio data on to the ADAV80x with the appropriate selection of SW11 to SW08 on the DIP switch. When SW11 = 1 and SW10 = 1, the data from the Toslink receiver is sent to the ADAV80x playback port. When SW09 = 1 and SW08 = 1, the data is sent to the ADAV80x auxiliary input port.

The playback and auxiliary input ports can also accept audio data from other sources such as the ADAV80x record or auxiliary output ports. The CPLD outputs for the playback and auxiliary input ports can also be three-stated, allowing users to connect an audio data source to the PLAY and APLAY pin headers. Table 5 and Table 6 show the switch settings to select the different sources.

Table 5. Playback Port Source

SW11	SW10	CPLD Mode	Source
0	0	DAC0	Three-state
0	1	DAC1	Record port
1	0	DAC2	Auxiliary output port
1	1	DAC3	SPDIF receiver

Table 6. Auxiliary Input Source

SW9	SW8	CPLD Mode	Source
0	0	AUXDAC0	Three-state
0	1	AUXDAC1	Record port
1	0	AUXDAC2	Auxiliary output port
1	1	AUXDAC3	SPDIF receiver

SPDIF Transmitter Sources

The Toslink optical transmitter can be provided with a selection of audio sources such as the record or auxiliary output ports. The output of the ADAV80x SPDIF transmitter (DITOUT) can also be connected directly to the Toslink transmitter, if required, using LK7. Table 7 shows the switch settings to select the appropriate source.

Table 7. SPDIF Transmitter Source

SW7	SW6	CPLD Mode	Source
0	0	DIT0	Three-state
0	1	DIT1	Record port
1	0	DIT2	Auxiliary output port
1	1	DIT3	Optical input

SPDIF Transmitter Clock Source

The CS8406 is configured to require a master clock source that operates at 128 × f_S. SW5 and SW4 allow users to choose an appropriate clock from the selection available. Suitable clocks can come from the PLL system clock outputs, the MCLKI input, and so on. Typically, these clocks are all 256 × f_S, so the CPLD automatically divides this clock in two before passing it on to the CS8406. Table 8 shows the appropriate switch settings to select the clock source for the SPDIF transmitter. For proper operation of the CS8406, the left/right clock and the master clock provided to it must be synchronous.

Table 8. SPDIF Transmitter MCLK Source

SW5	SW4	CPLD Mode	Source
0	0	MCLKDIT0	SYSCLK1/2
0	1	MCLKDIT1	SYSCLK2/2
1	0	MCLKDIT2	SYSCLK3/2
1	1	MCLKDIT3	MCLKI/2 when SW1 = 1
1	1	MCLKDIT3	MCLK/2 from CS8416 when SW1 = 0

ADAV80x MCLK Source

The ADAV80x can take its MCLK from the following three sources:

- In the default setting, an MCLK is taken from the SPDIF recovered clock. This mode is selected with LK4, LK23, and SW0.
- LK4 selects an MCLK from the crystal oscillator or an external MCLK connected to the SMA connector. To use the recovered MCLK from the SPDIF stream, LK4 should be in Position A or Position B. If LK4 is in Position A, LK3 should be in Position B to disable the output of the crystal oscillator.
- LK23 connects the CPLD to the MCLKI pin of the ADAV80x. When SW0 on the DIP switch is 1, the CPLD pin is an output, providing the recovered SPDIF MCLK to the ADAV80x.

Table 9. MCLKI Control

SW0	Source
0	CPLD is an input pin that receives an MCLK from either the 12.288 MHz oscillator or an external MCLK source.
1	CPLD provides a selected clock to the ADAV80x. Link LK4 and Link LK23 should be set accordingly to prevent multiple sources from attempting to drive the MCLKI pin.

EVALUATION BOARD SOFTWARE

The EVAL-ADAV801/ADAV803 come with PC-compatible software that gives easy access to the control registers of the ADAV80x. The software uses the parallel printer port and is compatible with Windows® 9x/2000/NT/XP. A centronics printer port cable is required to connect the evaluation board to the PC.

INSTALLING THE SOFTWARE

The software is supplied on a CD-ROM.

To install the software, insert the CD-ROM in the CD-ROM drive to automatically start the installation procedure.

If the CD-ROM drive is not set up to do this, double-click the **SETUP.EXE** file in the root directory of the CD-ROM to begin installation.

RUNNING THE SOFTWARE

You can start the software via the shortcuts added to the **Start** menu. The application file has a shortcut located in **:/Program Files/Analog Devices/ADAV80x**.

When the software initializes, it checks to see what operating system is present.

- For PCs that use Windows NT/2000, the printer port address is automatically detected.
- For PCs that use Windows 95/98 and others, you must select the printer port.

The software gives you access to the internal registers of the ADAV80x. Each of the internal blocks of the ADAV80x has an individual control panel where you can change the registers. The control panels give a graphical representation of the registers rather than showing the individual contents of each bit location. A separate control panel is available that shows the contents of all the registers, including the register address. When you select an option on any control panel, the required register change is automatically sent to the evaluation board, allowing you to instantly see the result of the change.

The position of each control panel on the screen is remembered when the panel is closed, and it is placed in the same position when reopened.

The software gives you an easy way to program the control register, but it is not intended to support operations that require continuous and speedy read and write operations such as continuously monitoring SPDIF channel status/user bits or interrupt conditions. Therefore, you have limited ability to evaluate these functions with the software provided.

Once the evaluation board and ADAV80x are set up to a required specification, the register values can be saved to a file, allowing them to be retrieved again at a later time and reloaded to the ADAV80x. This option is available on the **Main Control Panel** menu.

EXAMPLE PROGRAMS

The ADAV80x software comes with several configuration examples. The program name gives an indication of what the program sets the ADAV80x up to do and also gives the switch configuration required for the DIP switch. For example, **adc_&_dac_110001110001.dat** configures the ADC and DAC, provided that the switches are set to 1100 0111 0001.

EDITING THE CPLD CODE

The evaluation boards come with the CPLD programmed to offer enough functionality to allow you to easily evaluate the performance and functionality of the ADAV80x. The configuration program in the CPLD is shown in the CPLD Code section. This code can be used as a template to reprogram the CPLD, if required.

Software to program the CPLD is available on the Lattice Semiconductor website. (Note: This software is not supported by Analog Devices, Inc.) The CPLD used is an M4A5-128/64-10YNC. Download cables, also available from Lattice, connect to Header J5 on the evaluation boards, allowing you to program the CPLD.

CPLD CODE

LISTING 1—ADAV801 CPLD CODE

```
MODULE Src_Sel

TITLE 'ADAV80x Eval Board Source Select Logic (Rev D)'

//*************************************************************************//
//     Title : ADAV800 Evaluation Board Source Select Logic Revision D
//     In this document 'Inputs' are inputs to the CPLD and
//     'Outputs' are outputs from the CPLD
//*************************************************************************//

LIBRARY 'mach';

DECLARATIONS

"INPUTS
       //dedicated inputs

       SW0, SW1, SW2, SW3,SW4,SW5,SW6,SW7,SW8,SW9,SW10,SW11  pin 46,45,44,43,38,37,36,35,34,33,32,31;
       SPI_CIN, SPI_CLATCH, SPI_CCLK, COUT   pin 76,94,95,47;
       RESET, RESET_IN pin 57,58;
       OPTIN_SDATA,OPTIN_LRCLK,OPTIN_SCLK, OPTIN_MCLK pin 72,71,70,69;
       CLK0, CLK1, CLK2 pin 68, 63, 62;

       //dedicated outputs

       CIN, CLATCH, CCLK, SPI_COUT pin 48,49,50,96 istype 'com';
       RESET_DUT, RESET_OUT pin 56,55 istype 'com';
       BCLK_IN, LRCLK_IN,DATAOUT pin 75,74, 73 istype 'com';
       MCLK_DIT pin 59 istype 'com';
       MCLKI pin 61 istype 'com';

       //dedicated I2S inputs

       OSDATA pin 12 istype 'com';
       OAUXSDATA pin 21 istype 'com';

       //dedicated I2S outputs

       ISDATA pin 9 istype 'com';
       ILRCLK,IBCLK,IAUXLRCLK,IAUXBCLK, IAUXSDATA pin 7, 8, 22,23,24 istype 'com';

       //bidirectional I2S pins

       OLRCLK,OBCLK,OAUXLRCLK,OAUXBCLK pin 10,11, 19, 20;


       //additional i/o pins
```

```
        TCLK,RD,RFS,RCLK,IO1,IO2,IO3,IO4,IN1 pin 100,99,98,97,93,88,87,86,85;
        IN2,IN3,OUT1,OUT2 pin 84,83,82,81;
        TFS, TD pin 5,6;

        FF1 node istype 'reg_d, buffer'; "a flip-flop
        MCLKDIT_int node;      "internal node for clock divider

"MACROS
        //PLAYBACK PORT SOURCE (DAC)
        DAC0 = !SW11 & !SW10;  //three-state
        DAC1 = !SW11 & SW10;   //ADC
        DAC2 = SW11 & !SW10;   //AUXADC
        DAC3 = SW11 & SW10;    //CS8416

        //AUXILIARY INPUT SOURCE (AUXDAC)
        AUXDAC0 = !SW9 & !SW8; //three-state
        AUXDAC1 = !SW9 & SW8;  //ADC
        AUXDAC2 = SW9 & !SW8;  //AUXADC
        AUXDAC3 = SW9 & SW8;   //CS8416

        //SPDIF TRANSMITTER CS8406 SOURCE (DIT)
        DIT0 = !SW7 & !SW6;    //three-state
        DIT1 = !SW7 & SW6;     //ADC
        DIT2 = SW7 & !SW6;     //AUXADC
        DIT3 = SW7 & SW6;      //CS8416

        //SPDIF TRANSMITTER CS8406 CLOCK SOURCE (MCLKDIT)
        MCLKDIT0 = !SW5 & !SW4; //CLK0
        MCLKDIT1 = !SW5 & SW4; //CLK1
        MCLKDIT2 = SW5 & !SW4; //CLK2
        MCLKDIT3 = SW5 & SW4;  //MCLKI or OPTIN_MCLK

EQUATIONS
        FF1.set=0;
        FF1.ar=0;

        RESET_DUT=RESET;
        RESET_OUT=RESET;


        //PLAYBACK PORT SOURCE = RECORD PORT (DAC=ADC)
        ILRCLK=OLRCLK & DAC1;
        IBCLK=OBCLK & DAC1;
        ISDATA=OSDATA & DAC1;

        //PLAYBACK PORT SOURCE = AUXILIARY OUTPUT PORT (DAC=AUXADC)
        ILRCLK=OAUXLRCLK & DAC2;
        IBCLK=OAUXBCLK & DAC2;
        ISDATA=OAUXSDATA & DAC2;
```

```
//PLAYBACK PORT SOURCE = SPDIF RECEIVER (DAC=CS8416)
ILRCLK=OPTIN_LRCLK & DAC3;
IBCLK=OPTIN_SCLK & DAC3;
ISDATA=OPTIN_SDATA & DAC3;

//PLAYBACK PORT SOURCE = three-state control
ILRCLK.oe= !DAC0;
IBCLK.oe= !DAC0;
ISDATA.oe=!DAC0;       //pins are three-state in DAC0 mode

//AUXILIARY INPUT SOURCE = RECORD PORT (AUXDAC=ADC)
IAUXLRCLK=OLRCLK & AUXDAC1;
IAUXBCLK=OBCLK & AUXDAC1;
IAUXSDATA=OSDATA & AUXDAC1;

//AUXILIARY INPUT SOURCE = AUXILIARY OUTPUT PORT (DAC=AUXADC)
IAUXLRCLK=OAUXLRCLK & AUXDAC2;
IAUXBCLK=OAUXBCLK & AUXDAC2;
IAUXSDATA=OAUXSDATA & AUXDAC2;

//AUXILIARY INPUT SOURCE = SPDIF RECEIVER (DAC=CS8416)
IAUXLRCLK=OPTIN_LRCLK & AUXDAC3;
IAUXBCLK=OPTIN_SCLK & AUXDAC3;
IAUXSDATA=OPTIN_SDATA & AUXDAC3;

//AUXILIARY INPUT SOURCE = three-state control
IAUXLRCLK.oe= !AUXDAC0;
IAUXBCLK.oe= !AUXDAC0;
IAUXSDATA.oe=!AUXDAC0; //pins are three-state in AUXDAC0 mode

//SPDIF TRANSMITTER SOURCE = RECORD PORT (CS8406=ADC)
BCLK_IN = OBCLK & DIT1;
LRCLK_IN = OLRCLK & DIT1;
DATAOUT = OSDATA & DIT1;

// SPDIF TRANSMITTER SOURCE = AUXILIARY OUTPUT PORT (CS8406=AUXADC)
BCLK_IN = OAUXBCLK & DIT2;
LRCLK_IN = OAUXLRCLK & DIT2;
DATAOUT = OAUXSDATA & DIT2;

// SPDIF TRANSMITTER SOURCE = OPTICAL INPUT (CS8406=CS8416)
BCLK_IN = OPTIN_SCLK & DIT3;
LRCLK_IN = OPTIN_LRCLK & DIT3;
DATAOUT = OPTIN_SDATA & DIT3;

BCLK_IN.oe = (DIT1 # DIT2 # DIT3);
LRCLK_IN.oe = (DIT1 # DIT2 # DIT3);
DATAOUT.oe = (DIT1 # DIT2 # DIT3);
```

```
        //LET MCLKI BE AN ACTIVE ONLY WHEN SW0 IS HIGH
        MCLKI = (OPTIN_MCLK & SW0);
        MCLKI.OE = SW0;

        //SPDIF TRANSMITTER CLOCK SOURCE (MCLK_DIT SOURCE)
        MCLKDIT_int = (MCLKDIT0 & CLK0) # (MCLKDIT1 & CLK1) # (MCLKDIT2 & CLK2)# (MCLKDIT3 & OPTIN_MCLK
&!SW1) # (MCLKDIT3 & SW1 & MCLKI);
        FF1.clk = MCLKDIT_int;
        FF1.d = !FF1.q;
        MCLK_DIT = FF1.q;

//Interface mode depends on ADAV80x part used

        //SPI Mode
        CCLK = !SPI_CCLK;
        CLATCH = SPI_CLATCH;
        CIN = !SPI_CIN;
        SPI_COUT = COUT;

END
```

LISTING 2—ADAV803 CPLD CODE

```
MODULE Src_Sel

TITLE 'ADAV80x Eval Board Source Select Logic (Rev D)'

//*************************************************************************//
//      Title : ADAV800 Evaluation Board Source Select Logic Revision D
//      In this document 'Inputs' are inputs to the CPLD and
//      'Outputs' are outputs from the CPLD
//*************************************************************************//

LIBRARY 'mach';

DECLARATIONS

"INPUTS
        //dedicated inputs for I2C

        SW0, SW1, SW2, SW3,SW4,SW5,SW6,SW7,SW8,SW9,SW10,SW11 pin 46,45,44,43,38,37,36,35,34,33,32,31;
        SPI_CIN, SPI_CLATCH, SPI_CCLK pin 76,94,95; //From parallel port: SPI_CIN is SDA and SPI_CCLK is SCL
        RESET, RESET_IN pin 57,58;
        OPTIN_SDATA,OPTIN_LRCLK,OPTIN_SCLK, OPTIN_MCLK pin 72,71,70,69;
        CLK0, CLK1, CLK2 pin 68, 63, 62;
        I2C_COUT pin 60; // From ADAV803: I2C_COUT is SDA for acknowledges

        //dedicated outputs for I2C

        CIN, CLATCH, COUT, CCLK pin 48,49,47,50 istype 'com'; //To ADAV803: CIN is SDA, CCLK is SCL, CLATCH
is ADO and COUT is AD1
        SPI_COUT pin 96 istype 'com'; //To parallel port: SPI_COUT is SDA for acknowledges
        RESET_DUT, RESET_OUT pin 56,55 istype 'com';
        BCLK_IN, LRCLK_IN,DATAOUT pin 75,74, 73 istype 'com';
        MCLK_DIT pin 59 istype 'com';
        MCLKI pin 61 istype 'com';

        //dedicated I2S inputs

        OSDATA pin 12 istype 'com';
        OAUXSDATA pin 21 istype 'com';

        //dedicated I2S outputs

        ISDATA pin 9 istype 'com';
        ILRCLK,IBCLK,IAUXLRCLK,IAUXBCLK, IAUXSDATA pin 7, 8, 22,23,24 istype 'com';

        //bidirectional I2S pins

        OLRCLK,OBCLK,OAUXLRCLK,OAUXBCLK pin 10,11, 19, 20;
```

```
        //additional i/o pins

        TCLK,RD,RFS,RCLK,IO1,IO2,IO3,IO4,IN1 pin 100,99,98,97,93,88,87,86,85;
        IN2,IN3,OUT1,OUT2 pin 84,83,82,81;
        TFS, TD pin 5,6;

        FF1 node istype 'reg_d, buffer'; "a flip-flop
        MCLKDIT_int node;      "internal node for clock divider


"MACROS
        //PLAYBACK PORT SOURCE (DAC)
        DAC0 = !SW11 & !SW10;  //three-state
        DAC1 = !SW11 & SW10;   //ADC
        DAC2 = SW11 & !SW10;   //AUXADC
        DAC3 = SW11 & SW10;    //CS8416

        //AUXILIARY INPUT SOURCE (AUXDAC)
        AUXDAC0 = !SW9 & !SW8; //three-state
        AUXDAC1 = !SW9 & SW8;  //ADC
        AUXDAC2 = SW9 & !SW8;  //AUXADC
        AUXDAC3 = SW9 & SW8;   //CS8416

        //SPDIF TRANSMITTER CS8406 SOURCE (DIT)
        DIT0 = !SW7 & !SW6;    //three-state
        DIT1 = !SW7 & SW6;     //ADC
        DIT2 = SW7 & !SW6;     //AUXADC
        DIT3 = SW7 & SW6;      //CS8416

        //SPDIF TRANSMITTER CS8406 CLOCK SOURCE (MCLKDIT)
        MCLKDIT0 = !SW5 & !SW4; //CLK0
        MCLKDIT1 = !SW5 & SW4; //CLK1
        MCLKDIT2 = SW5 & !SW4; //CLK2
        MCLKDIT3 = SW5 & SW4;  //MCLKI or OPTIN_MCLK

EQUATIONS
        FF1.set=0;
        FF1.ar=0;

        RESET_DUT=RESET;
        RESET_OUT=RESET;

        //PLAYBACK PORT SOURCE = RECORD PORT (DAC=ADC)
        ILRCLK=OLRCLK & DAC1;
        IBCLK=OBCLK & DAC1;
        ISDATA=OSDATA & DAC1;

        //PLAYBACK PORT SOURCE = AUXILIARY OUTPUT PORT (DAC=AUXADC)
        ILRCLK=OAUXLRCLK & DAC2;
        IBCLK=OAUXBCLK & DAC2;
```

```
ISDATA=OAUXSDATA & DAC2;

//PLAYBACK PORT SOURCE = SPDIF RECEIVER (DAC=CS8416)
ILRCLK=OPTIN_LRCLK & DAC3;
IBCLK=OPTIN_SCLK & DAC3;
ISDATA=OPTIN_SDATA & DAC3;

//PLAYBACK PORT SOURCE = three-state control
ILRCLK.oe= !DAC0;
IBCLK.oe= !DAC0;
ISDATA.oe=!DAC0; //pins are three-state in DAC0 mode

//AUXILIARY INPUT SOURCE = RECORD PORT (AUXDAC=ADC)
IAUXLRCLK=OLRCLK & AUXDAC1;
IAUXBCLK=OBCLK & AUXDAC1;
IAUXSDATA=OSDATA & AUXDAC1;

//AUXILIARY INPUT SOURCE = AUXILIARY OUTPUT PORT (DAC=AUXADC)
IAUXLRCLK=OAUXLRCLK & AUXDAC2;
IAUXBCLK=OAUXBCLK & AUXDAC2;
IAUXSDATA=OAUXSDATA & AUXDAC2;

//AUXILIARY INPUT SOURCE = SPDIF RECEIVER (DAC=CS8416)
IAUXLRCLK=OPTIN_LRCLK & AUXDAC3;
IAUXBCLK=OPTIN_SCLK & AUXDAC3;
IAUXSDATA=OPTIN_SDATA & AUXDAC3;

//AUXILIARY INPUT SOURCE = three-state control
IAUXLRCLK.oe= !AUXDAC0;
IAUXBCLK.oe= !AUXDAC0;
IAUXSDATA.oe=!AUXDAC0; //pins are three-state in AUXDAC0 mode

//SPDIF TRANSMITTER SOURCE = RECORD PORT (CS8406=ADC)
BCLK_IN = OBCLK & DIT1;
LRCLK_IN = OLRCLK & DIT1;
DATAOUT = OSDATA & DIT1;

// SPDIF TRANSMITTER SOURCE = AUXILIARY OUTPUT PORT (CS8406=AUXADC)
BCLK_IN = OAUXBCLK & DIT2;
LRCLK_IN = OAUXLRCLK & DIT2;
DATAOUT = OAUXSDATA & DIT2;

// SPDIF TRANSMITTER SOURCE = OPTICAL INPUT (CS8406=CS8416)
BCLK_IN = OPTIN_SCLK & DIT3;
LRCLK_IN = OPTIN_LRCLK & DIT3;
DATAOUT = OPTIN_SDATA & DIT3;

BCLK_IN.oe = (DIT1 # DIT2 # DIT3);
LRCLK_IN.oe = (DIT1 # DIT2 # DIT3);
DATAOUT.oe = (DIT1 # DIT2 # DIT3);
```

```
        //LET MCLKI BE AN ACTIVE ONLY WHEN SW0 IS HIGH
        MCLKI = (OPTIN_MCLK & SW0);
        MCLKI.OE = SW0;

        //SPDIF TRANSMITTER CLOCK SOURCE (MCLK_DIT SOURCE)
        MCLKDIT_int = (MCLKDIT0 & CLK0) # (MCLKDIT1 & CLK1) # (MCLKDIT2 & CLK2)# (MCLKDIT3 & OPTIN_MCLK
&!SW1) # (MCLKDIT3 & SW1 & MCLKI);
        FF1.clk = MCLKDIT_int;
        FF1.d = !FF1.q;
        MCLK_DIT = FF1.q;

//Interface mode depends on ADAV80x part used

        //I2C Mode
        CCLK = !SPI_CCLK; //SCL
        CIN = !SPI_CIN; //SDA
        CLATCH = 0; //AD0=0
        COUT = 0; //AD1=0
        SPI_COUT = !I2C_COUT; //SCL for acknowledges


END
```

EVALUATION BOARD SCHEMATICS AND ARTWORK

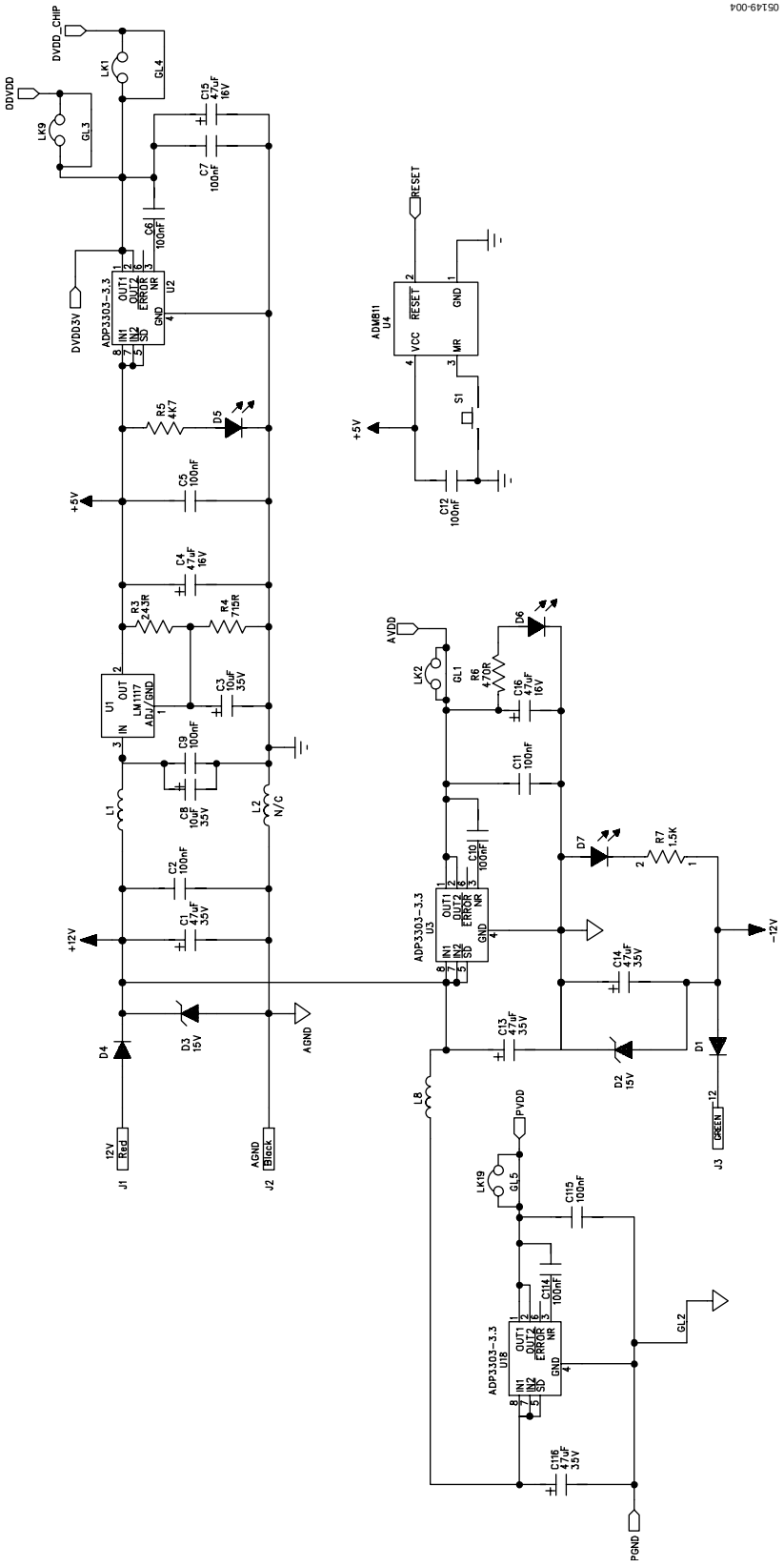

Figure 4. Evaluation Board Schematic (Page 1 of 4)

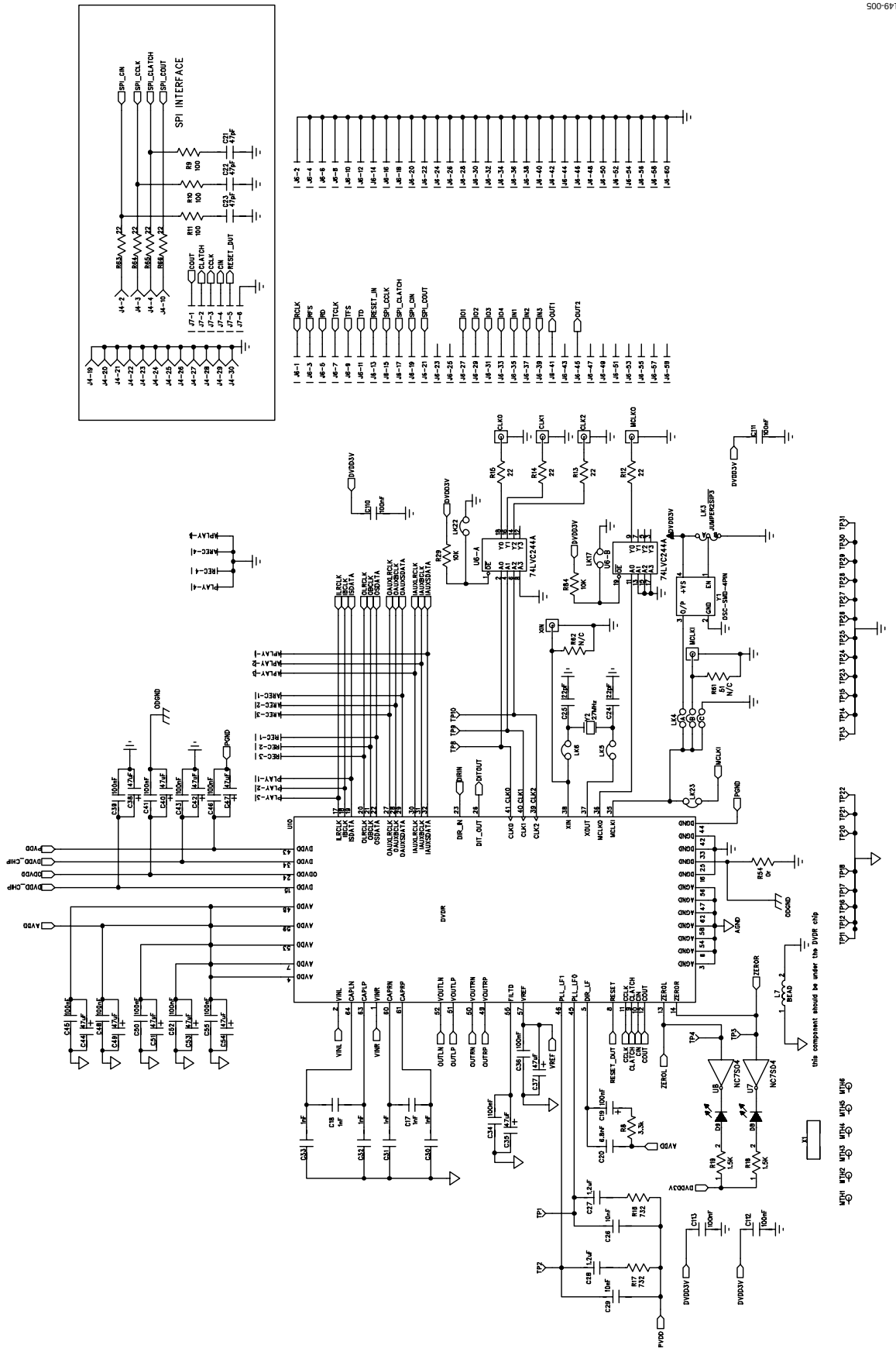

Figure 5. Evaluation Board Schematic (Page 2 of 4)

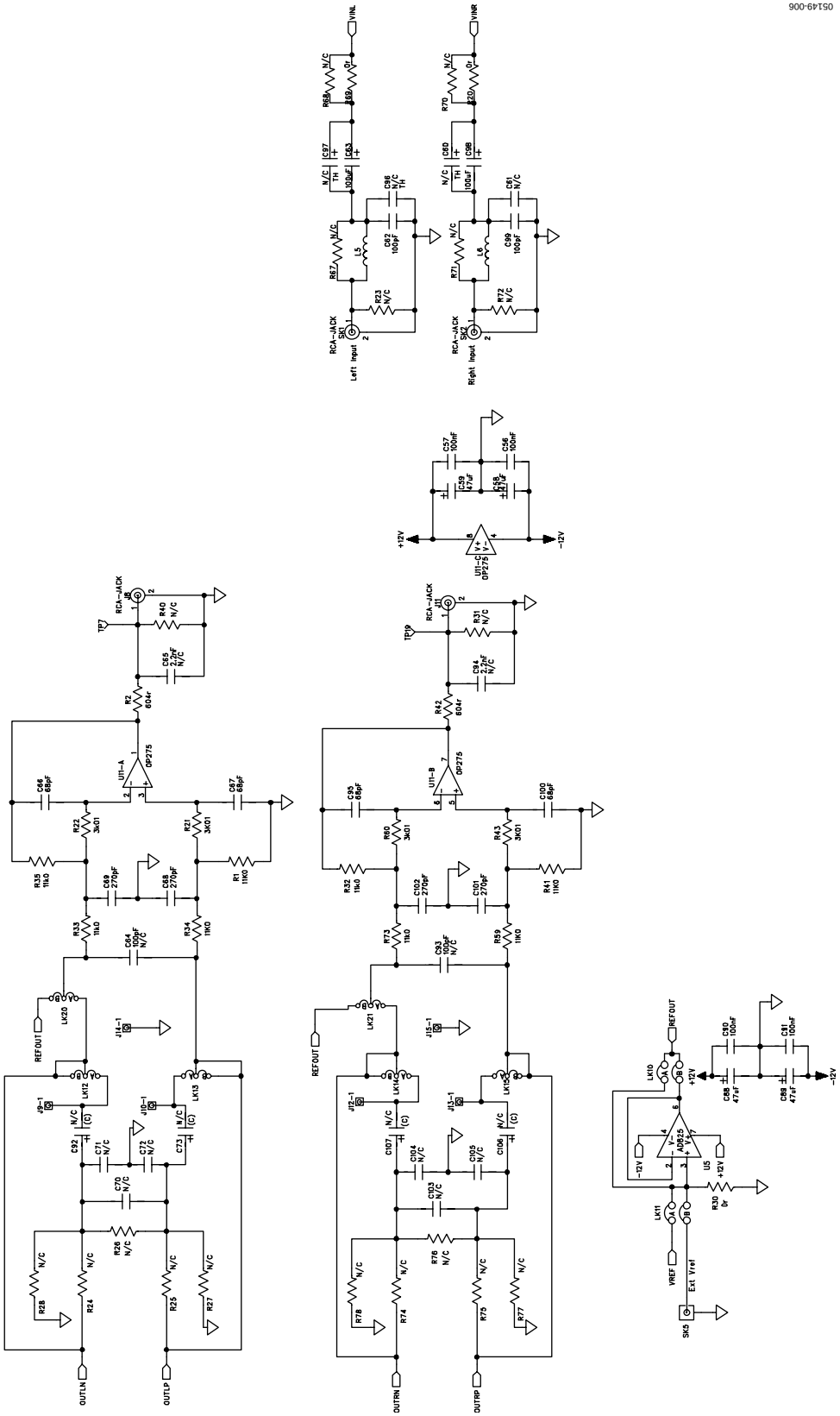

Figure 6. Evaluation Board Schematic (Page 3 of 4)

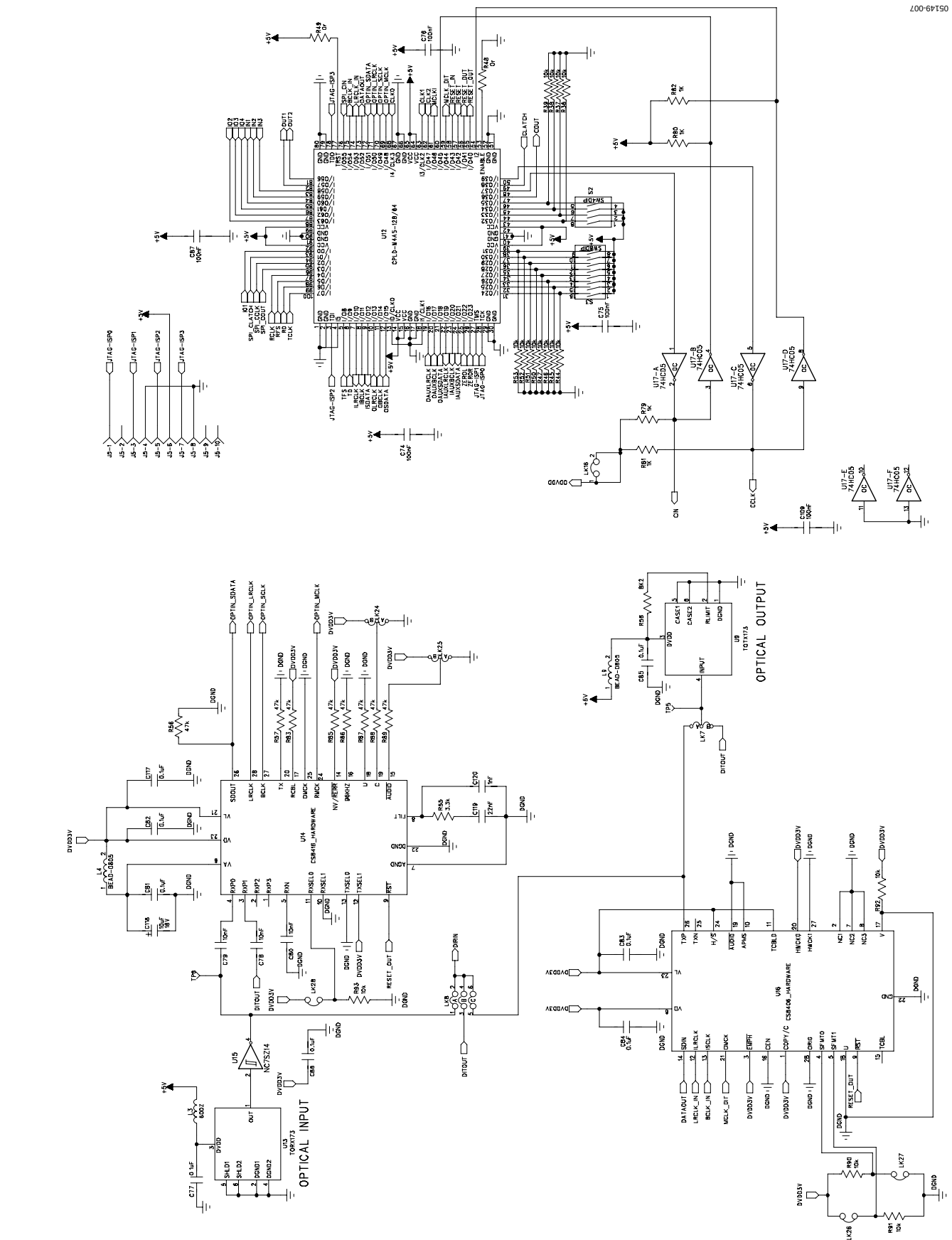

Figure 7. Evaluation Board Schematic (Page 4 of 4)

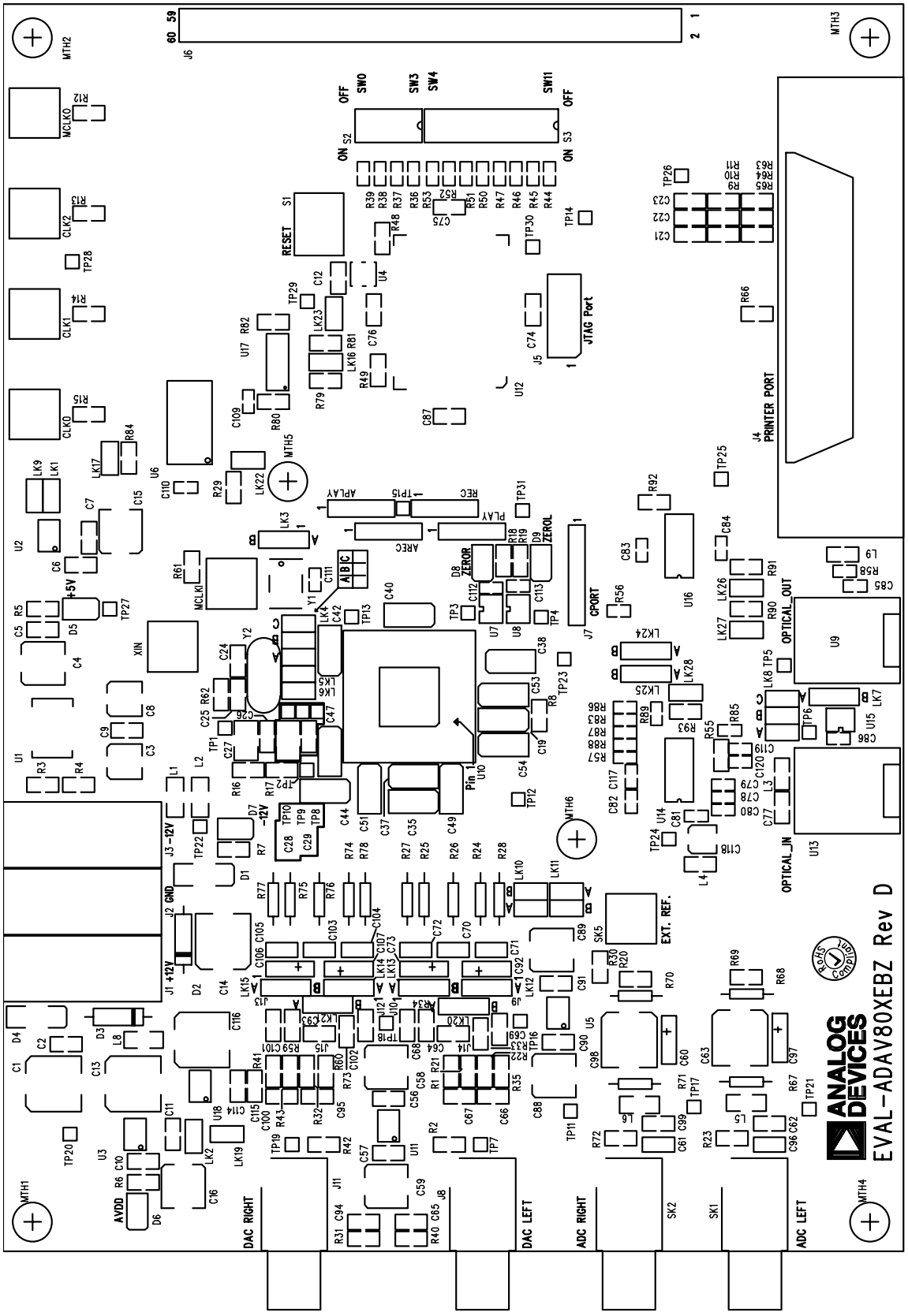

Figure 8. Evaluation Board Silkscreen

ORDERING INFORMATION

BILL OF MATERIALS

Table 10.

Qty	Reference	Part Name	Description	Manufacturer	Order Number
1	X1	52QFP clamp	N/C		N/C
1	J6	60-pin header	N/C		N/C
1	U17	74HC05	Open-drain inverter	Texas Instruments	Farnell 959-0978
1	U6	74LVC244A	8-bit buffer	Texas Instruments	Farnell 110-2982
1	U5	AD825	Single op amp, 8-pin	Analog Devices	Analog Devices supplied
1	U4	ADM811	Voltage monitor	Analog Devices	Analog Devices supplied
3	U2, U3, U18	ADP3303-3.3	Precision low dropout voltage regulator	Analog Devices	Analog Devices supplied
1	J1	Banana	Red banana socket	Deltron	Farnell 110-1127
1	J2	Banana	Black banana socket	Deltron	Farnell 110-1128
1	J3	Banana	Green banana socket	Deltron	Farnell 110-1129
5	L1, L5 to L8	Bead	Surface mount inductor	Murata	Farnell 952-6862
1	L2	Bead	N/C		N/C
3	L3, L4, L9	Bead-0805	Surface mount inductor	Steward	Digikey 240-2399-1-ND
19	C2, C5 to C7, C9 to C12, C56, C57, C74 to C76, C77, C87, C90, C91, C114, C115	Cap, 100 nF, 10%	100 nF X7R surface mount capacitor	EPCOS	Farnell 755-849
23	C34, C36, C39, C41, C43, C45, C46, C48, C50, C52, C55, C81 to C86, C109 to C113, C117	Cap, 100 nF, 10%	100 nF X7R surface mount capacitor	Phycomp	Farnell 432-210
2	C62, C99	Cap, 100 pF, 5%	100 pF NPO surface mount capacitor	Panasonic	Digikey PCC101CGCT-ND
2	C93, C64	Cap, 100 pF, 5%	N/C		N/C
2	C26, C29	Cap, 10 nF, 5%	10 nF X7R surface mount capacitor	Phycomp	Farnell 301-9937
3	C78 to C80	Cap, 10 nF, X7R	10 nF X7R surface mount capacitor	AVX	Farnell 756-9548
7	C17, C18, C30 to C33, C120	Cap, 1 nF, 5%	1 nF COG (NPO) surface mount capacitor	Panasonic	Digikey PCC2151CT-ND
2	C65, C94	Cap, 2.2 nF, 5%	N/C		N/C
1	C119	Cap, 22 nF, 10%	22 nF X7R surface mount capacitor	Panasonic	Digikey PCC1754TR-ND
2	C24, C25	Cap, 22 pF, 5%	22 pF COG (NPO) surface mount capacitor	Yageo	Digikey 311-1103-1-ND
4	C68 to C69, C101, C102	Cap, 270 pF, 5%	270 pF COG (NPO) surface mount capacitor	Panasonic	DigiKey PCC271CGCT-ND
3	C21 to C23	Cap, 47 pF, 5%	47 pF COG (NPO) surface mount capacitor	Kemet	Digikey 399-1117-1-ND
1	C20	Cap, 6.8 nF, 10%	6.8 nF X7R surface mount capacitor	Panasonic	Digikey PCC1990CT-ND
4	C66, C67, C95, C100	Cap, 68 pF, 5%	68 pF COG (NPO) surface mount capacitor	Panasonic	Digikey PCC680CGCT-ND
2	C61, C96	Cap, N/C	N/C		N/C

Qty	Reference	Part Name	Description	Manufacturer	Order Number
6	C70 to C72, C103 to 105	Cap, N/C, 5%	N/C		N/C
1	C19	CAP+, 100 nF, 10%	100 nF X7R 1210 surface mount capacitor	Kemet Corp.	Digikey 399-1268-1-ND
2	C3, C8	CAP+, 10 µF, 20%	10 µF Case C aluminum electrolytic capacitor	Panasonic	Farnell 9694471
1	C118	CAP+, 10 µF, 20%	10 µF Case B aluminum electrolytic capacitor	Panasonic	Farnell 969-3491
11	C35, C37, C38 C40, C42, C44, C47, C49, C51, C53, C54	CAP+, 47 µF	47 µF tantalum electrolytic capacitor	AVX	Farnell 197-324
4	C1, C13, C14, C116	CAP+, 47 µF, 20%	47 µF Case E aluminum electrolytic capacitor	Panasonic	Farnell 969-4501
7	C15, C16, C58, C59, C88, C89, C4	CAP+, 47 µF, 20%	47 µF Case D aluminum electrolytic capacitor	Panasonic	Farnell 969-4382
6	C60, C73, C92, C97, C106, C107	CAP+, N/C	N/C		N/C
2	C63, C98	CAP+ELEK, 100 µF, 20%	100 µF Case E aluminum electrolytic capacitor	Panasonic	Digikey PCE4003CT-ND
2	C27, C28	CAP_1210,1.2 µF, 10%	1.2 µF X5R 1210 surface mount capacitor	Kemet Corp.	Digikey 399-3077-1-ND
1	J4	Centronics	36-pin 90° Centronics connector	Multicomp	Farnell 113-1098
4	APLAY AREC PLAY REC	CON-SIP-4P	4-way pin header	Molex	Farnell 973-3434
1	J7	CON-SIP-6P	6-way pin header	Molex	Farnell 973-3434
1	J5	CON\10HEADER	10-way IDC header	Harwin	Farnell 102-2244 and 150-410
1	U12	CPLD-M4A5-128/64	CPLD-M4A5-128/64-10YNC	Lattice	
1	U16	CS8406	SPDIF transmitter	Cirrus Logic	Farnell 102-3448
1	U14	CS8416	SPDIF receiver	Cirrus Logic	Farnell 102-3452
2	D1, D4	DIODE-DL4001	SMD rectifier diode, 50 V, 1 A	Microsemi	Digikey DL4001-TPMSCT-ND
1	U10	DVDR	ADAV80x	Analog Devices	Analog Devices Supplied
5	GL1 to GL5	GROUNDLINK			
13	LK1, LK2, LK5, LK6, LK9, LK16, LK17, LK19, LK22, LK23, LK26 to LK28	Jumper	Jumper block, 2 pins, 0.1" spacing	Harwin	Farnell 102-2264 and 150-410
2	LK10 to LK11	Jumper-2	2-link block, 4 pins, 0.1" sq. spacing	Harwin	Farnell 102-2244 and 150-410
2	LK4, LK8	Jumper-3	3-link block, 6 pins, 0.1" sq. spacing	Harwin	Farnell 102-2244 and 150-410
10	LK3, LK7, LK12 to LK15, LK20, LK21, LK24, LK25	Jumper2\SIP3	Jumper block using 3-pin sip header	Harwin	Farnell 102-2264 and 150-410
3	D5, D8, D9	LED	Red light emitting diode	Avago Technologies	Farnell 105-8413
1	D6	LED	Yellow light emitting diode	Avago Technologies	Farnell 105-8412
1	D7	LED	Green light emitting diode	Avago Technologies	Farnell 105-8390
1	U1	LM1117	3-terminal adjustable regulator	National Semiconductor	Farnell 948-6267
2	U7, U8	NC7S04	Hex inverter	Fairchild Semiconductor	Farnell 101-4133
1	U15	NC7SZ14	Inverter	Fairchild Semiconductor	Farnell 118-2397
1	U11	OP275	Dual bipolar/JFET audio op amp	Analog Devices	Analog Devices supplied
1	Y1	OSC-SMD-4-pin, 12.288 MHz	SMD crystal oscillator	CTS CORP	Digikey CTX266LVCT-ND

Qty	Reference	Part Name	Description	Manufacturer	Order Number
4	J8, J11, SK1, SK2	RCA-JACK	Audio connector	Unbranded	Farnell 152-396
6	R20, R30, R48, R49, R54, R69	RES, 0r,5%	0 Ω resistor	Panasonic	Digikey P0.0ACT-ND
3	R7, R18, R19	RES, 1.5k,1%	1.5 kΩ resistor	Yageo	Digikey 311-1.50KCRCT-ND
3	R9 to R11	RES, 100,1%	100 Ω resistor	Yageo	Digikey 311-100CRCT-ND
12	R36 to R39, R44 to R47, R50 to R53	RES, 10k,1%	10 kΩ resistor	Multicomp	Farnell 911-355
6	R29, R84, R90 to R93	RES, 10k,1%	10 kΩ resistor	Panasonic	Digikey P10.0KCCT-ND
8	R1, R32, R33, R34, R35, R41, R59, R73	RES, 11k0,1%	11 kΩ resistor	Panasonic	Digikey P11.0KCCT-ND
4	R79 to R82	RES, 1k,1%	1 kΩ resistor	Yageo	Digikey 311-1.00KCRCT-ND
8	R12 to R15, R63 to R66	RES, 22,1%	22 Ω resistor	Yageo	Digikey 311-22.0CRCT-ND
1	R3	RES, 243R,1%	243 Ω resistor	Yageo	Digikey 311-243CRCT-ND
2	R8, R55	RES, 3.3k,5%	3.3 kΩ resistor	Panasonic	Digikey P3.3KATR-ND
4	R21, R22, R43, R60	RES, 3.01k,1%	3.01 kΩ resistor	Panasonic	DigiKey P3.01KCCT-ND
1	R6	RES, 470R,1%	470 Ω resistor	Yageo	Digikey 311-470CRCT-ND
8	R56, R57, R83, R85 to R89	RES, 47k,5%	47 kΩ resistor	Panasonic	Digikey P47KATR-ND
1	R5	RES, 4.7k0,1%	4.7 kΩ resistor	Yageo	Digikey 311-4.70KCRCT-ND
1	R61	RES, 51	N/C		N/C
2	R2, R42	RES, 604R,1%	604 Ω resistor	Panasonic	DigiKey P604CCT-ND
1	R4	RES, 715R,1%	715 Ω resistor	Yageo	Digikey 311-715CRCT-ND
2	R16, R17	RES, 732,1%	732 Ω resistor	Yageo	Digikey 311-732CRCT-ND
1	R58	RES, 8.2k,5%	8.2 kΩ resistor	Panasonic	Digikey P8.2KGTR-ND
5	R23, R31, R40, R62, R72	RES, N/C	N/C		N/C
14	R24 to R26, R27, R28, R67, R68, R70, R71, R74 to R78	RES, N/C	N/C		N/C
6	CLK0 to CLK2, MCLKI, MCLKO, XIN	SMA	SMA connector	Tyco Electronics	Farnell 105-6377
1	SK5	SMB	SMB connector	Johnson/Emerson	Farnell 101-9330
1	S1	SW-PUSH	Push button switch (sealed 6 mm × 6 mm)	Omron	Farnell 176-432
1	S2	SW\4DIP	4-way DIP switch	Erg Components	Farnell 422-642
1	S3	SW\8DIP	8-way DIP switch	Erg Components	Farnell 422-666
31	TP1 to TP31	Test point	Test points	Vero	Farnell 873-1128
1	U13	TORX173	Toslink receiver	Toshiba	
1	U9	TOTX173	Toslink transmitter	Toshiba	
6	J9, J10, J12 to J15	Wire wrap	N/C		N/C
1	Y2	XTAL 1,27 MHz	27 MHz crystal	Citizen	Digikey 300-8515-ND
2	D2, D3	Zener diode	15 V Zener diode	Fairchild Semiconductor	Farnell 984-4511

ORDERING GUIDE

Model	Description
EVAL-ADAV801EBZ[1]	ADAV801 Evaluation Board
EVAL-ADAV803EBZ[1]	ADAV803 Evaluation Board

[1] Z = RoHS Compliant Part.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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