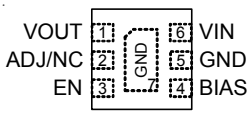
500mA, 5.5V, Ultra Low Dropout Linear Regulator

General Description

The RT9081A is a high performance positive voltage regulator with separated bias voltage (V_{BIAS}), designed for applications requiring low input voltage and ultra low dropout voltage, output current up to 500mA. The feature of ultra low dropout voltage is ideal for applications where output voltage is very close to input voltage. The input voltage can be as low as 0.8V and the output voltage is adjustable by an external resistive divider. The RT9081A features very low quiescent current consumption for portable applications. The device is available in the ZADFN-6L 1.2x1.2 package.

Pin Configuration

(TOP VIEW)



ZADFN-6L 1.2x1.2

Features

- **Input Voltage Range : 0.8V to 5.5V**
- **Bias Voltage Range : 2.4 V to 5.5 V**
- **Output Voltage Fixed and Adjustable Versions**
  - **0.9V to 1.8V (Fixed)**
  - **0.8V to 3.6V (Adjustable)**
- **1.5% Output Voltage Accuracy @ 25°C**
- **Ultra Low Dropout Voltage : 140mV at 500mA**
- **Low Bias Input Current**
- **80μA in Operating Mode**
- **0.5μA in Disable Mode**
- **Enable Control**
- **Output Active Discharge Function (Optional)**
- **Stable with a 1μF Output Ceramic Capacitor**
- **RoHS Compliant and Halogen Free**

Applications

- Battery Powered Systems
- Portable Electronic Device
- Digital Set Top Boxes

Ordering Information

Product No.	Nominal Output Voltage	Option	Package	Lead Plating System	Pin 1 Orientation
RT9081A-09GQZA(2)	0.90V	Output Active Discharge	ZADFN-6L 1.2x1.2 (Z-Type)	G : Green (Halogen Free and Pb Free)	(2): Quadrant 2 Follow EIA-481-D ***Empty means Pin1 orientation is Quadrant 1
RT9081A-10GQZA	1.00V				
RT9081A-1KGQZA	1.05V				
RT9081A-11GQZA	1.10V				
RT9081A-1AGQZA(2)	1.15V				
RT9081A-12GQZA	1.20V				
RT9081A-1BGQZA(2)	1.25V				
RT9081A-13GQZA(2)	1.30V				
RT9081A-15GQZA(2)	1.50V				
RT9081A-18GQZA(2)	1.80V				
RT9081AGQZA(2)	Adjustable				

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Typical Application Circuit

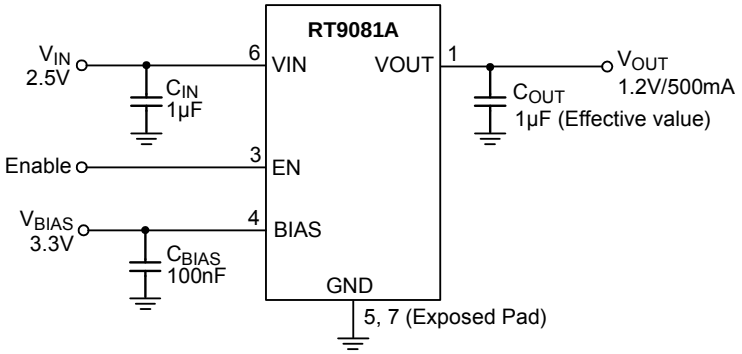


Figure 1. Fixed Voltage Regulator

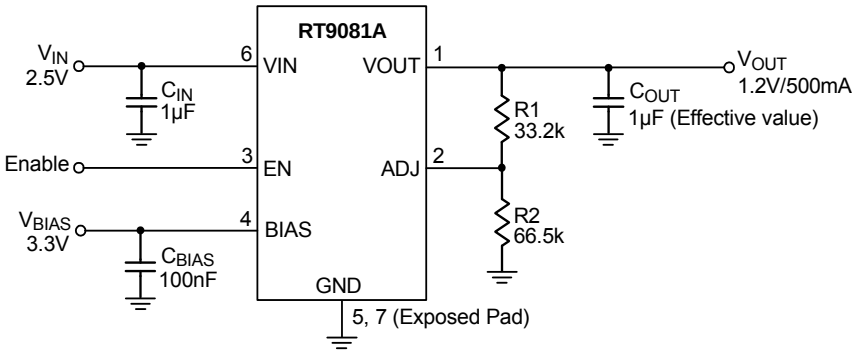


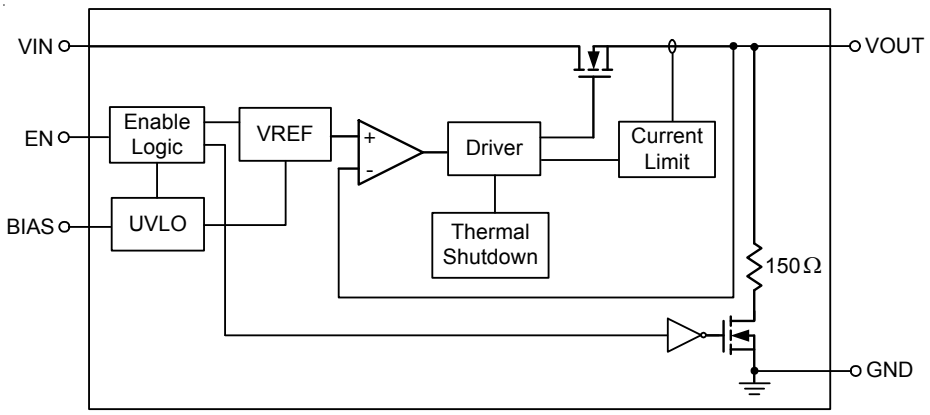
Figure 2. Adjustable Voltage Regulator

Functional Pin Description

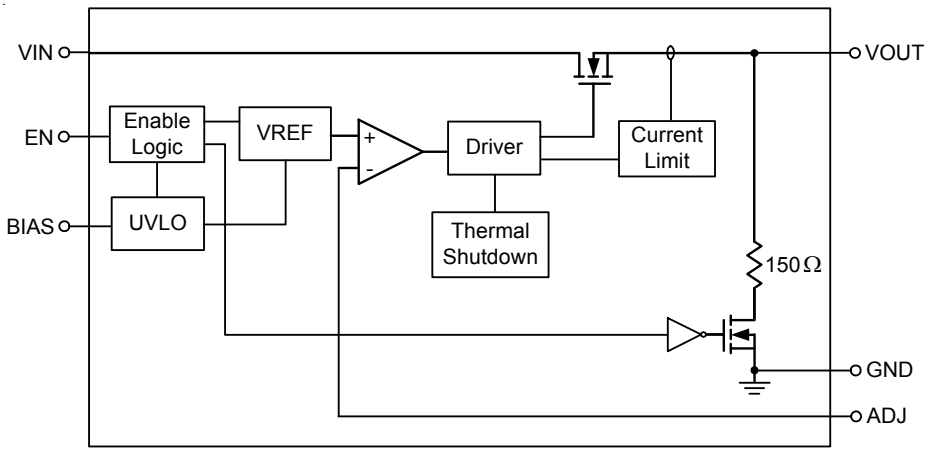
Pin No.	Pin Name	Pin Function
1	VOUT	Power output for the LDO.
2 (Fixed)	NC	Test pin. Internal pull down by 2µA. This pin should be floating or connected to ground.
2 (Adj)	ADJ	Power output for the LDO.
3	EN	LDO enable.
4	BIAS	Supply voltage for the LDO control circuit. Mandatory to power up V_{BIAS} before EN and VIN, this will ensure RT9081A performance follows datasheet spec. For more information please see Chip Enable Operation section.
5, 7 (Expose pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
6	VIN	Power input for the LDO.

Functional Block Diagram

V_{OUT} Fixed Version



V_{OUT} Adjustable Version



Operation

The RT9081A is using N-MOSFET pass transistor for output voltage regulation from VIN voltage. The separated bias voltage (V_{BIAS}) power the low current internal control circuit for applications requiring low input voltage and ultra low dropout voltage.

In steady-state operation, the feedback voltage is regulated to the reference voltage by the internal regulator. When the feedback voltage signal is less than the reference, the output current passes through the power MOSFET will be increased. The extra amount of the current is sent to the output until the voltage level of FB pin returns to the reference. On the other hand, if the feedback voltage is higher than the reference, the power MOSFET current is decreased. The excess charge at the output can be released by the loading current.

Over-Temperature Protection (OTP)

The RT9081A has an over-temperature protection. When the device triggers the OTP, the device shuts down until the temperature back to normal state.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 6V
- All Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  ZADFN-6L 1.2x1.2 ---------- 0.73W
- Package Thermal Resistance (Note 2)
  ZADFN-6L 1.2x1.2, θ_{JA} ---------- 136.5°C/W
  ZADFN-6L 1.2x1.2, θ_{JC} ---------- 0.98°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  CDM (Charged Device Model) ---------- 1kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 0.8V to 5.5V
- Supply Input Voltage, V_{BIAS} ---------- 2.4V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{BIAS} = 2.7V, or (V_{OUT} + 1.6V), whichever is greater, V_{IN} = $V_{OUT(Normal)}$ + 0.3V, I_{OUT} = 1mA, V_{EN} = 1V, C_{IN} = 1µF, C_{OUT} = 1µF (Effective value), T_A = 25°C, unless otherwise specified). (Note 6)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Input Voltage Range	V_{IN}		V_{OUT} + V_{DROP}	--	5.5	V
Operating Bias Voltage Range	V_{BIAS}		(V_{OUT} +1.4) > 2.4	--	5.5	V
Under Voltage Lock-Out	V_{UVLO}	V_{BIAS} rising	--	1.6	--	V
		Hysteresis	--	0.2	--	V
Reference Voltage (Adj devices only)	V_{REF}		--	0.8	--	V
Output Voltage Accuracy	V_{OUT}	(Note 5)	–0.5	--	0.5	%
Output Voltage Accuracy (Note 5)	V_{OUT}	$V_{OUT(Normal)}$ + 0.3V ≤ V_{IN} ≤ $V_{OUT(Normal)}$ + 1V, 2.7V or ($V_{OUT(Normal)}$ + 1.6V), whichever is greater < V_{BIAS} < 5.5V, 1mA < I_{OUT} < 500mA	–1.5	--	1.5	%
V_{IN} Line Regulation	ΔV_{LINE_VIN}	$V_{OUT(NOM)}$ + 0.3V ≤ V_{IN} ≤ 5V	--	0.01	--	%/V
V_{BIAS} Line Regulation	ΔV_{LINE_BIAS}	2.7V or ($V_{OUT(Normal)}$ + 1.6V), whichever is greater < V_{BIAS} < 5.5V	--	0.01	--	%/V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Load Regulation		ΔV_{LOAD}	I_{OUT} = 1mA to 500mA	--	1.5	--	mV
V_{IN} Dropout Voltage		V_{DROP_VIN}	I_{OUT} = 150mA (Note 7)	--	37	75	mV
			I_{OUT} = 500mA (Note 7)	--	140	250	mV
V_{BIAS} Dropout Voltage		V_{DROP_BIAS}	I_{OUT} = 500mA, V_{IN} = V_{BIAS} (Note 7, Note 8)	--	1.1	1.5	V
Output Current Limit		I_{LIM}	V_{OUT} = 90% $V_{OUT(Normal)}$	550	800	1000	mA
ADJ Pin Operating Current (ADJ devices only)		I_{ADJ}		--	0.1	0.5	μA
Bias Pin Operating Current		I_{BIAS}	V_{BIAS} = 2.7V	--	80	110	μA
Bias Pin Disable Current		$I_{BIAS(DIS)}$	$V_{EN} \leq$ 0.4 V	--	0.5	1	μA
VIN Pin Disable Current		$I_{VIN(DIS)}$	$V_{EN} \leq$ 0.4 V	--	0.5	1	μA
EN Input Voltage	Logic_High	V_{IH}		0.9	--	--	V
	Logic_Low	V_{IL}		--	--	0.4	
EN Pull Down Current		I_{EN}	V_{EN} = 5.5V, V_{BIAS} = 5.5V	--	1	--	μA
Turn-On Time		t_{ON}	From assertion of V_{EN} to V_{OUT} = 98% $V_{OUT(NOM)}$. $V_{OUT(NOM)}$ = 1V	--	150	--	μs
Power Supply Rejection Ratio		$PSRR\_V_{IN}$	V_{IN} to V_{OUT}, f = 1kHz, I_{OUT} = 150mA, $V_{IN} \geq V_{OUT}$ + 0.5V	--	70	--	dB
		$PSRR\_V_{BIAS}$	V_{BIAS} to V_{OUT}, f = 1kHz, I_{OUT} = 150mA, $V_{IN} \geq V_{OUT}$ + 0.5V	--	80	--	dB
Output Noise Voltage (Fixed Volt.)		e_{NO_FIXED}	V_{IN} = V_{OUT} + 0.5 V, $V_{OUT(NOM)}$ = 1V, f = 10Hz to 100kHz	--	40	--	μV_{RMS}
Output Noise Voltage (Adj devices)		e_{NO_ADJ}	V_{IN} = V_{OUT} + 0.5V, f = 10Hz to 100kHz	--	50 x V_{OUT}	--	μV_{RMS}
Thermal Shutdown Threshold			Temperature increasing	--	160	--	°C
			Temperature decreasing	--	140	--	°C
Output Discharge Pull-Down		R_{DISCHG}	$V_{EN} \leq$ 0.4V, V_{OUT} = 0.5V	--	150	--	Ω

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a two-layer Richtek Evaluation Board.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Adjustable devices tested at 0.8V; external resistor tolerance is not taken into account.

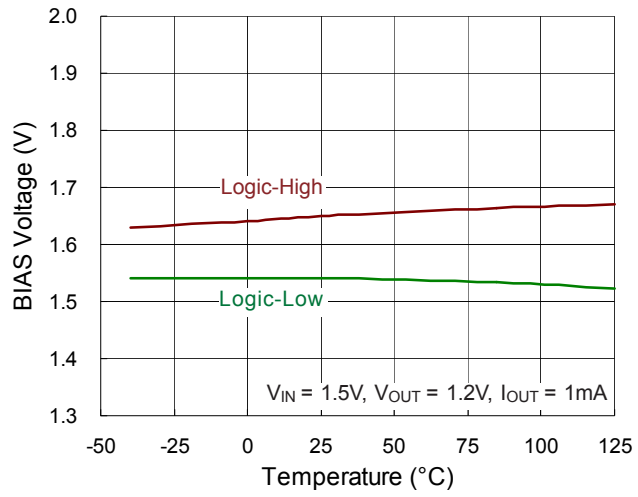
Note 6. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.

Note 7. Dropout voltage is characterized when V_{OUT} falls 3% below $V_{OUT(Normal)}$.

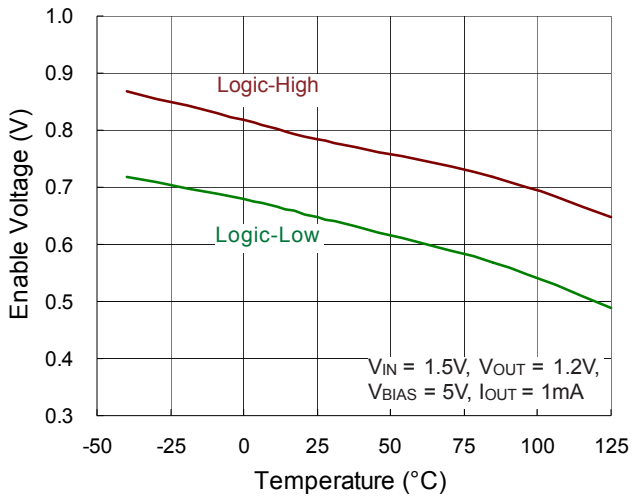
Note 8. For output voltages below 0.9V, V_{BIAS} dropout voltage does not apply due to a minimum Bias operating voltage of 2.4V.

Typical Operating Characteristics

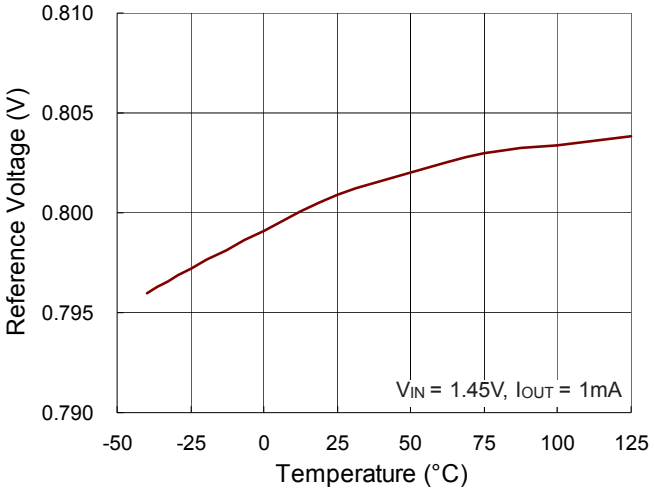
BIAS Voltage UVLO vs. Temperature



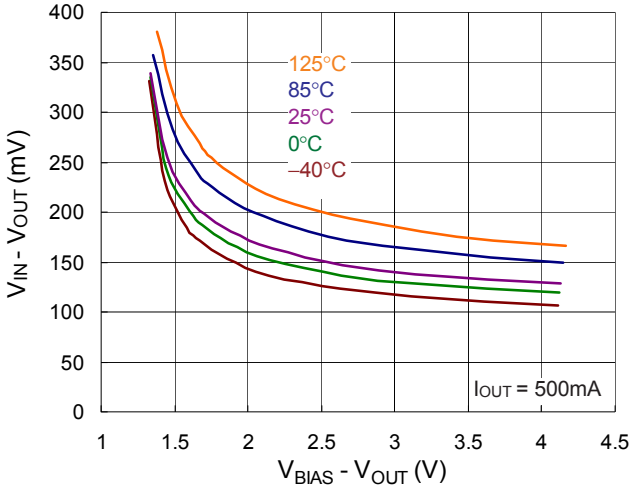
Enable Voltage Threshold vs. Temperature



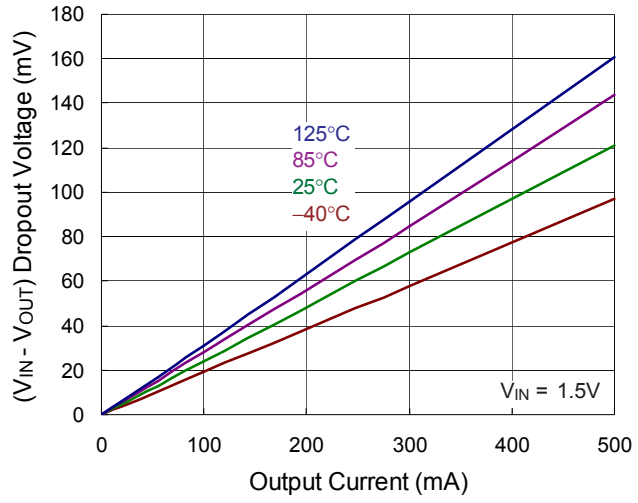
Reference Voltage vs. Temperature



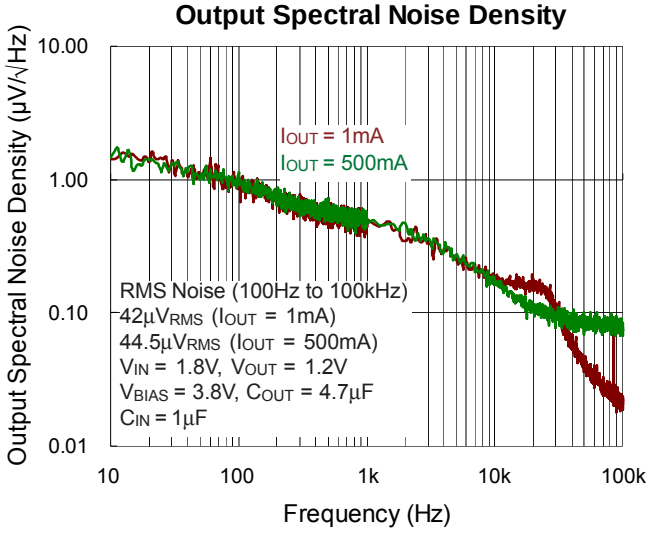
V_{IN} Dropout Voltage vs. (V_{BIAS} - V_{OUT})



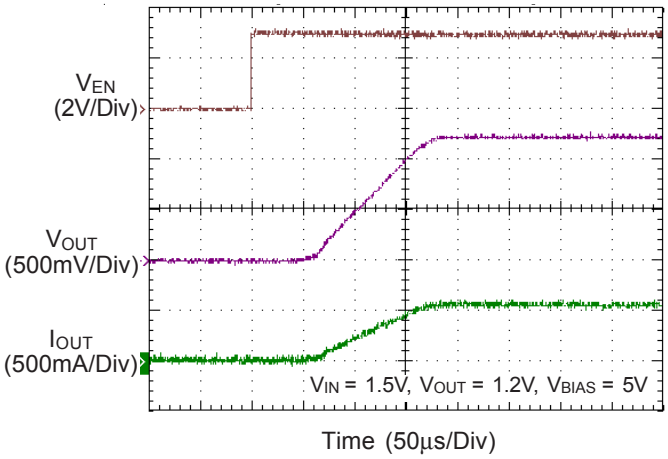
Dropout Voltage vs. Output Current



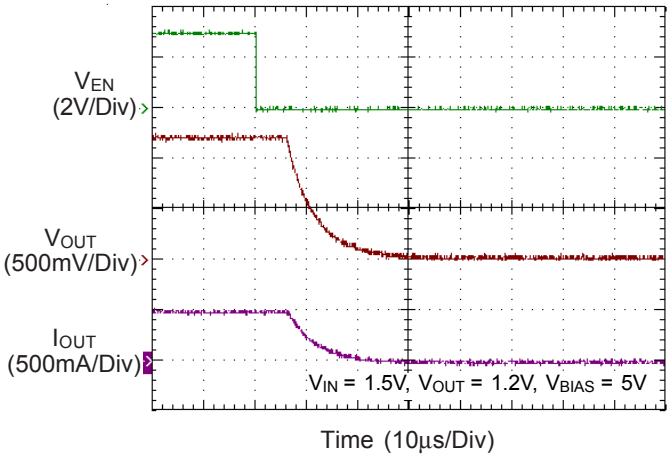
Output Spectral Noise Density



Power On from EN



Power Off from EN



Application Information

The RT9081A is a low voltage, low dropout linear regulator with input voltage V_{IN} from 0.8V to 5.5V, V_{BIAS} from 2.4V to 5.5V and adjusted output voltage from 0.8V to (V_{IN} – V_{DROP}).

Output Voltage Setting

For the RT9081A, the voltage on the ADJ pin sets the output voltage and is determined by the values of R1 and R2. The values of R1 and R2 can be calculated for any voltage using the formula given in Equation :

$$V_{OUT} = 0.8V \times \left(\frac{R1 + R2}{R2} \right)$$

Using lower values for R1 and R2 is recommended to reduces the noise injected from the FB pin. Note that R1 is connected from VOUT pin to ADJ pin, and R2 is connected from ADJ to GND.

Chip Enable Operation

The RT9081A goes into sleep mode when the EN pin is in a logic low condition. In this condition, the pass transistor, error amplifier, and band gap are all turned off.

Dropout Voltage

There are two power supply inputs V_{IN} and V_{BIAS} and only one output V_{OUT} for the RT9081A, the Dropout voltage with these two different input also have different definition. VIN Dropout voltage is the voltage difference between VIN and VOUT when V_{OUT} starts to decrease while reduce V_{IN} level (for this condition, V_{BIAS} needs high enough as specific value published in Electrical Characteristics table). V_{BIAS} dropout voltage is the voltage difference between V_{BIAS} and V_{OUT} while VIN and BIAS pins are connected together and V_{OUT} starts to decrease.

C_{IN} and C_{OUT} Selection

The RT9081A is designed specifically to work with low ESR ceramic output capacitor for space saving and performance consideration. Using a ceramic capacitor with capacitance range from 1μF (Effective value) to 10μF on the RT9081A output ensures stability. The input capacitor must be located at a distance of no more than 0.5 inch from the input pin of the chip. However, a capacitor with larger value and lower ESR (Equivalent Series Resistance) is recommended since it will provide better PSRR and line transient response. Any good quality ceramic capacitor can be used, C_{IN} = 1μF and C_{BIAS} = 0.1μF or greater are recommended.

Chip Enable Operation

The RT9081A goes into sleep mode when the EN pin is in a logic low condition. In this condition, the pass transistor, error amplifier, and band gap are all turned off reducing the supply current to only 1μA (max.).

Consideration should be taken in the power on sequence, it is mandatory to ensure $V_{BIAS} > V_{OUT} + 1.6V$ before both $V_{EN} > V_{IH}$ and $V_{IN} > V_{OUT} + 0.3V$. The BIAS pin supplies voltage for the LDO control circuit, and powering up V_{BIAS} first will ensure turn on time (t_{ON}) and output voltage accuracy (V_{OUT}) to follow datasheet spec.

Current Limit

The RT9081A continuously monitors the output current to protect the pass transistor against abnormal operations. When an overload or short circuit is encountered, the current limit circuitry controls the pass transistor's gate voltage to limit the output within the predefined range.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a

ZADFN-6L 1.2x1.2 package, the thermal resistance, θ_{JA}, is 136.5°C/W on a two-layer Richtek evaluation board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / (136.5°C/W) = 0.73W for a ZADFN-6L 1.2x1.2 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

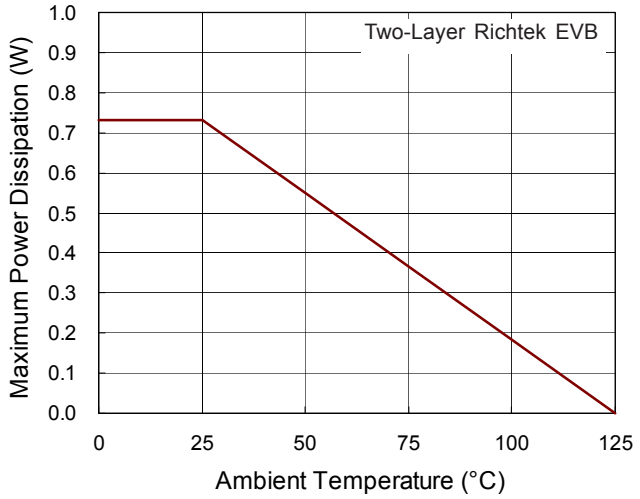
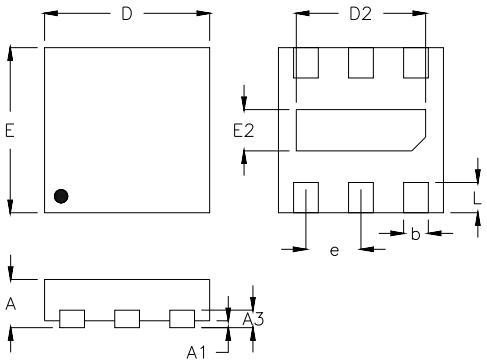
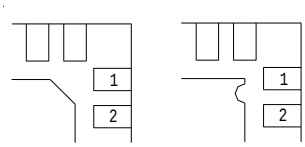


Figure 3. Derating Curve of Maximum Power Dissipation

Outline Dimension





DETAIL A

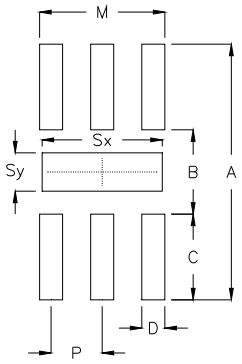
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.280	0.320	0.011	0.013
A1	0.000	0.010	0.000	0.000
A3	0.060		0.002	
b	0.130	0.230	0.005	0.009
D	1.100	1.300	0.043	0.051
D2	0.990	1.040	0.039	0.041
E	1.100	1.300	0.043	0.051
E2	0.350	0.400	0.014	0.016
e	0.400		0.016	
L	0.170	0.270	0.007	0.011

Z-Type 6L ADFN 1.2x1.2 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
U/X/ZADFN1.2*1.2-6	6	0.400	2.000	0.760	0.620	0.180	1.015	0.375	0.980	±0.050

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