NXP

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QorIQ Qonverge

QorIQ Qonverge Platform

QorIQ Qonverge B4860 Baseband Processor

Base station system-on-chip enables processing of three 20 MHz sectors of LTE

Overview

The QorIQ Qonverge B4860 device is a multi-standard wireless base station system-on-chip (SoC) based on 28 nm process technology. The B4860 reduces overall power consumption for high-end wireless macro base stations to deliver the industry's highest performance solution. The multicore SoC includes 10 programmable cores based on a StarCore flexible vector processor (FVP), 64-bit Power Architecture® cores, as well as CoreNet and Multi-Accelerator Platform Engine (MAPLE) technologies. The B4860 targets broadband wireless infrastructure and builds upon our proven success of existing multicore SoCs and DSPs in wireless infrastructure markets.

The B4860 is designed to adapt to the rapidly changing and expanding standards of LTE (FDD and TDD), LTE-Advanced including 3GPP LTE Rel.10/11 and WCDMA, as well as provide simultaneous support for multiple standards.

Layer 1 is implemented using a mix of StarCore SC3900FP high-performance FVP cores and the MAPLE baseband accelerator platform, which provides a highly efficient hardware implementation of standardized algorithms for

each of the air interface standards in single and multi-mode operations. Layer 2 and transport processing are implemented using a mix of e6500 64-bit dual threaded Power Architecture cores, data path and security accelerators.

The B4860 is perfectly suited to meet the performance demands of wireless operators for LTE, WCDMA and LTE-Advanced macro base stations. It includes a combination of fully programmable StarCore FVP cores, Power Architecture cores and powerful baseband acceleration to provide cost-effective, best-in-class performance, power efficiency and connectivity. With four dual-threaded e6500 64-bit cores operating at up to 1.8 GHz and six SC3900FP DSP cores at up to 1.2 GHz, the B4860 provides the required programmable performance. Additionally, the MAPLE hardware accelerators target processing of baseband functions, such as FEC decoding and encoding, FFT, PDSCH and PUSCH embedded data flows, WCDMA chiprate and MiMO equalization, allowing base station manufacturers to deliver higher throughputs, lower latencies and better spectral efficiency.

Target Applications

Macrocell base stations

- LTE (FDD and TDD)
- LTE Advanced
- WCDMA

QorIQ Qonverge B4460 Block Diagram
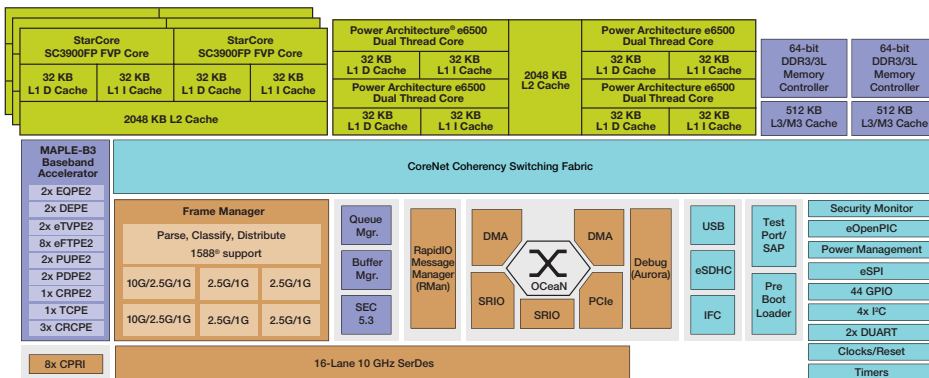
Core Complex (CPU, FVP, L1 and Cache)   Basic Peripherals and Interconnect
Accelerators and Memory Control   Networking Elements

BUILT ON
Power™

While the four Power Architecture cores offer industry-leading processing capacity and a major leap in available processor performance for layer 2 and layer 3 in many throughput-intensive, packet-processing networking applications, raw CPU processing power is not enough to achieve multi-Gb/s data rates. To address this, the B4860 uses Freescale Data Path Acceleration Architecture (DPAA), which significantly reduces data plane instructions per packet and enables more CPU cycles to work on value-added services rather than repetitive low-level tasks. Combined with specialized accelerators for cryptography and pattern matching, the B4860 allows the user's software to perform complex packet processing at high data rates.

The B4860 offloads performance and latency-critical layer 1 functions to MAPLE-B3, which integrates highly optimized and flexible accelerators. The smart partitioning introduced in B4860 provides an excellent balance between OEM intellectual property, hardwired accelerators and algorithms implemented on the fully programmable StarCore FVP and is highly efficient in terms of power dissipation and silicon area utilization.

QorIQ Qonverge B4860 Processor Features

Hardware

- Integrated processor cores and accelerators for layer control and transport processing

  ○ Four e6500 dual-threaded, 64-bit Power Architecture cores

    - Dual threading with simultaneous multi threading (SMT)
    - 128-bit AltiVec SIMD unit
    - 40-bit physical addressing
    - Fully featured MMU with a 1024-entry eight-way set-associative cache
    - Core virtualization supporting hypervisor and logical to real address translation
    - Clustered L2 cache allowing strict allocation or full sharing
    - Hardware support for L1 and L2 cache coherency

  ○ DPAA (frame manager, queue manager, buffer manager) for IP packed acceleration

  ○ Security protocol accelerators: SNOW-3G, Kasumi, ZUC, IPSec, DES, 3DES, AES, MD5, SHA-1/2, HMAC

- Integrated DSP cores and baseband accelerators for layer 1 processing

  ○ Six StarCore SC3900FP FVP programmable cores

    - Up to 32 MAC/cycle of 16-bit and up to 16 FLOP/cycle
    - Eight instructions per cycle
    - Up to eight data lanes vector in a single instruction (SIMD8)
    - State-of-the-art support for control code with branch prediction
    - Fully featured memory management unit and logical to real address translation
    - Clustered L2 cache allowing strict allocation or full sharing
    - Hardware support for L1 and L2 cache coherency

  ○ MAPLE baseband accelerators

    - FEC accelerators for LTE, LTE-Advanced and WCDMA
      ›› Turbo decoder with rate de-matching and HARQ combining
      ›› Turbo encoder with rate matching
      ›› Viterbi decoder
    - FFT/iFFT
    - DFT/iDFT
    - MiMO equalizer MMSE-based supporting IRC, SIC and PIC
    - Matrix inversion and multiplication
    - PUSCH data path embedded flow
    - PDSCH data path embedded flow
    - WCDMA/HSPA+ chip rate and path search
    - CRC

- CoreNet: Internal cache coherent switch fabric enabling full cache coherent system

- Two DDR-3/3L controllers: 64-bit, 1.867 GHz (each with 512 KB L3 cache)

- ECC support for on-chip and off-chip memories

- High-speed interfaces multiplexed into 16 SerDes 10G ports

  ○ Two 10 G/2.5 G/1 G Ethernet controllers

  ○ Four 2.5 G/1 G Ethernet controllers

  ○ IEEE® 1588v2 support

  ○ Two x4 Serial RapidIO controllers 5G (Gen II)

  ○ Eight CPRI v4.2 controllers 9.8G

  ○ Four-lane PCI Express® 5G (Gen II)

  ○ Eight Aurora: Tracing/debug

- Trust architecture with secure boot

- One serial port interface (eSPI)

- One eSD/eMMC interface

- One IFC: 16-bit integrated NAND/NOR flash controller or general-purpose interface

- One USB 2.0 interface

- Four I²C Interfaces

- Four UART ports

- 182 32-bit timers

- 44 general-purpose I/Os

Software

- Development tools from Freescale and partners

  ○ Eclipse IDE

  ○ Compilers

  ○ Debuggers

  ○ Profiling, critical code analysis, call tree, trace points

  ○ Nexus trace viewer, code viewer, performance view, trace analyzer

  ○ Scripting for post-process trace and performance data

  ○ Register analyzer

  ○ Device and core simulators

  ○ Operating systems

  ○ BSP and device drivers

- B4860QDS board: Software and reference application development system

- Freescale's optimized software reference libraries for LTE and WCDMA layer 1 PHY functions

General

- 1020-pin FC-PBGA package, 1 mm pitch

- Core voltage: VID

- I/O voltage: 1, 1.2, 1.35, 1.5, 1.8 and 2.5 nominal

- Industrial temperature range

- 12.3 MB internal memory

- Debug ports: Test access port and boundary scan architecture compliant with IEEE Std. 1149.1™, 1149.6™ and Nexus IEEE-ISTO 5001 trace support

- Lead-free ROHS compliant

For more information, visit freescale.com/QorIQQonverge