

FEATURES

Enhanced product features

- Supports defense and aerospace applications (AQEC)
- Military temperature range (–55°C to +125°C)
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

Low power, smallest pin-compatible octal DAC: 16 bits

16-lead TSSOP

On-chip 1.25 V, 5 ppm/°C reference

Power down to 400 nA at 5 V, 200 nA at 3 V

2.7 V to 5.5 V power supply

Guaranteed monotonic by design

Power-on reset to zero scale or midscale

3 power-down functions

Hardware LDAC and LDAC override function

CLR function to programmable code

Rail-to-rail operation

APPLICATIONS

Process control

Data acquisition systems

Portable battery-powered instruments

GENERAL DESCRIPTION

The **AD5668-EP** is a low power, octal, 16-bit, buffered voltage-output digital-to-analog converter (DAC). It operates from a single 2.7 V to 5.5 V supply and is guaranteed monotonic by design.

The **AD5668-EP** has an on-chip reference with an internal gain of 2. The **AD5668-EP** has a 1.25 V, 5 ppm/°C reference, giving a full-scale output range of 2.5 V. The on-board reference is off at power-up, allowing the use of an external reference, and the internal reference is enabled via a software write.

The part incorporates a power-on-reset circuit that ensures that the DAC output powers up to 0 V and remains powered up at this level until a valid write takes place. The part contains a power-down feature that reduces the current consumption of the device to 400 nA at 5 V and provides software-selectable output loads while in power-down mode for any or all DAC channels. The outputs of all DACs can be updated simultaneously using the LDAC function, with the added functionality of user-selectable

FUNCTIONAL BLOCK DIAGRAM

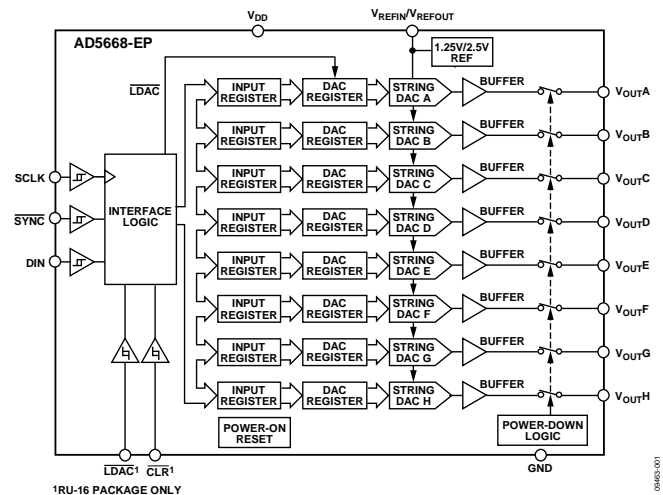


Figure 1.

DAC channels to simultaneously update. There is also an asynchronous CLR that updates all DACs to a user-programmable code—zero scale, midscale, or full scale.

The **AD5668-EP** uses a versatile 3-wire serial interface that operates at clock rates up to 50 MHz and is compatible with standard SPI, QSPI, MICROWIRE, and DSP interface standards.

Additional application and technical information can be found in the **AD5668** data sheet.

PRODUCT HIGHLIGHTS

1. Octal, 16-bit DAC.
2. On-chip 1.25 V/2.5 V, 5 ppm/°C reference.
3. Available in 16-lead TSSOP.
4. Power-on reset to 0 V or midscale.
5. Power-down capability. When powered down, the DAC typically consumes 200 nA at 3 V and 400 nA at 5 V.

Rev. A

Document Feedback

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REVISION HISTORY

| | |
|---------------------------------|----|
| 1/15—Rev. 0 to Rev. A | |
| Changes to Ordering Guide | 14 |

10/10—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 4.5\text{ V to }5.5\text{ V}$, $R_L = 2\text{ k}\Omega$ to GND, $C_L = 200\text{ pF}$ to GND, $V_{REFIN} = V_{DD}$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted. Temperature range is -55°C to $+125^\circ\text{C}$, typical at $+25^\circ\text{C}$.

Table 1.

| Parameter | Min | Typ | Max | Unit | Conditions/Comments |
|--|-------|-----------|----------|------------------------------|--|
| STATIC PERFORMANCE¹ | | | | | |
| Resolution | 16 | | | Bits | |
| Relative Accuracy | | ± 8 | ± 21 | LSB | See Figure 4 |
| Differential Nonlinearity | | | ± 1 | LSB | Guaranteed monotonic by design (see Figure 7) |
| Zero-Code Error | | 1 | 14 | mV | All 0s loaded to DAC register (see Figure 9) |
| Zero-Code Error Drift | | ± 2 | | $\mu\text{V}/^\circ\text{C}$ | |
| Full-Scale Error | | -0.2 | -1 | % FSR | All 1s loaded to DAC register (see Figure 10) |
| Gain Error | | | ± 1 | % FSR | |
| Gain Temperature Coefficient | | ± 2.5 | | ppm | Of FSR/ $^\circ\text{C}$ |
| Offset Error | | ± 1 | ± 14 | mV | |
| DC Power Supply Rejection Ratio | | -80 | | dB | $V_{DD} \pm 10\%$ |
| DC Crosstalk (External Reference) | | 10 | | μV | Due to full-scale output change, $R_L = 2\text{ k}\Omega$ to GND or V_{DD} |
| | | 5 | | $\mu\text{V}/\text{mA}$ | Due to load current change |
| | | 10 | | μV | Due to powering down (per channel) |
| DC Crosstalk (Internal Reference) | | 25 | | μV | Due to full-scale output change, $R_L = 2\text{ k}\Omega$ to GND or V_{DD} |
| | | 10 | | $\mu\text{V}/\text{mA}$ | Due to load current change |
| OUTPUT CHARACTERISTICS² | | | | | |
| Output Voltage Range | 0 | | V_{DD} | V | |
| Capacitive Load Stability | | 2 | | nF | $R_L = \infty$ |
| | | 10 | | nF | $R_L = 2\text{ k}\Omega$ |
| DC Output Impedance | | 0.5 | | Ω | |
| Short-Circuit Current | | 30 | | mA | $V_{DD} = 5\text{ V}$ |
| Power-Up Time | | 4 | | μs | Coming out of power-down mode, $V_{DD} = 5\text{ V}$ |
| REFERENCE INPUTS | | | | | |
| Reference Current | | 40 | 55 | μA | $V_{REF} = V_{DD} = 5.5\text{ V}$ (per DAC channel) |
| Reference Input Range | 0 | | V_{DD} | V | |
| Reference Input Impedance | | 14.6 | | k Ω | |
| REFERENCE OUTPUT | | | | | |
| Output Voltage | 1.247 | | 1.253 | V | At ambient |
| Reference Temperature Coefficient ² | | ± 5 | | ppm/ $^\circ\text{C}$ | |
| Reference Output Impedance | | 7.5 | | k Ω | |
| LOGIC INPUTS² | | | | | |
| Input Current | | | ± 3 | μA | All digital inputs |
| Input Low Voltage, V_{INL} | | | 0.8 | V | $V_{DD} = 5\text{ V}$ |
| Input High Voltage, V_{INH} | 2 | | | V | $V_{DD} = 5\text{ V}$ |
| Pin Capacitance | | 3 | | pF | |
| POWER REQUIREMENTS | | | | | |
| V_{DD} | 4.5 | | 5.5 | V | All digital inputs at 0 or V_{DD} , DAC active, excludes load current |
| I_{DD} (Normal Mode) ³ | | | | | $V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$ |
| $V_{DD} = 4.5\text{ V to }5.5\text{ V}$ | | 1.3 | 1.8 | mA | Internal reference off |
| $V_{DD} = 4.5\text{ V to }5.5\text{ V}$ | | 2 | 2.6 | mA | Internal reference on |
| I_{DD} (All Power-Down Modes) ⁴ | | | | | |
| $V_{DD} = 4.5\text{ V to }5.5\text{ V}$ | | 0.4 | 1 | μA | $V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$ |

¹ Linearity calculated using a reduced code range of AD5668 (Code 512 to 65,024). Output unloaded.

² Guaranteed by design and characterization; not production tested.

³ Interface inactive. All DACs active. DAC outputs unloaded.

⁴ All eight DACs powered down.

AC CHARACTERISTICS

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$, $R_L = 2\text{ k}\Omega$ to GND, $C_L = 200\text{ pF}$ to GND, $V_{REFIN} = V_{DD}$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted. Temperature range is -55°C to $+125^\circ\text{C}$, typical at $+25^\circ\text{C}$.

Table 2.

| Parameter ¹ | Min | Typ | Max | Unit | Conditions/Comments |
|----------------------------------|-----|-----|-----|------------------------------|---|
| Output Voltage Settling Time | | 6 | 10 | μs | $\frac{1}{4}$ to $\frac{3}{4}$ scale settling to ± 2 LSB |
| Slew Rate | | 1.5 | | $\text{V}/\mu\text{s}$ | |
| Digital-to-Analog Glitch Impulse | | 4 | | $\text{nV}\cdot\text{sec}$ | 1 LSB change around major carry (see Figure 24) |
| Digital Feedthrough | | 0.1 | | $\text{nV}\cdot\text{sec}$ | |
| Reference Feedthrough | | -90 | | dB | $V_{REF} = 2\text{ V} \pm 0.1\text{ V p-p}$, frequency = 10 Hz to 20 MHz |
| Digital Crosstalk | | 0.5 | | $\text{nV}\cdot\text{sec}$ | |
| Analog Crosstalk | | 2.5 | | $\text{nV}\cdot\text{sec}$ | |
| DAC-to-DAC Crosstalk | | 3 | | $\text{nV}\cdot\text{sec}$ | |
| Multiplying Bandwidth | | 340 | | kHz | $V_{REF} = 2\text{ V} \pm 0.2\text{ V p-p}$ |
| Total Harmonic Distortion | | -80 | | dB | $V_{REF} = 2\text{ V} \pm 0.1\text{ V p-p}$, frequency = 10 kHz |
| Output Noise Spectral Density | | 120 | | $\text{nV}/\sqrt{\text{Hz}}$ | DAC code = 0x8400, 1 kHz |
| | | 100 | | $\text{nV}/\sqrt{\text{Hz}}$ | DAC code = 0x8400, 10 kHz |
| Output Noise | | 15 | | $\mu\text{V p-p}$ | 0.1 Hz to 10 Hz |

¹ Guaranteed by design and characterization; not production tested.

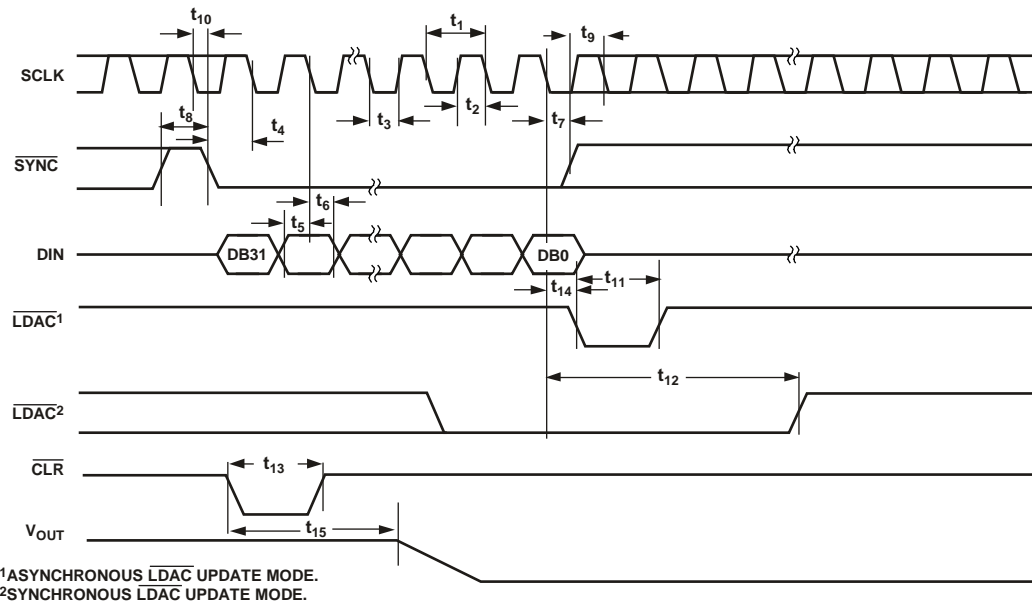
TIMING CHARACTERISTICS

All input signals are specified with $t_r = t_f = 1 \text{ ns/V}$ (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 2. $V_{DD} = 2.7 \text{ V}$ to 5.5 V . All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 3.

| Parameter | Limit at T_{MIN}, T_{MAX} $V_{DD} = 2.7 \text{ V}$ to 5.5 V | Unit | Conditions/Comments |
|-----------|--|--------|--|
| t_1^1 | 20 | ns min | SCLK cycle time |
| t_2 | 8 | ns min | SCLK high time |
| t_3 | 8 | ns min | SCLK low time |
| t_4 | 13 | ns min | $\overline{\text{SYNC}}$ to SCLK falling edge set-up time |
| t_5 | 4 | ns min | Data setup time |
| t_6 | 4 | ns min | Data hold time |
| t_7 | 0 | ns min | SCLK falling edge to $\overline{\text{SYNC}}$ rising edge |
| t_8 | 15 | ns min | Minimum $\overline{\text{SYNC}}$ high time |
| t_9 | 13 | ns min | $\overline{\text{SYNC}}$ rising edge to SCLK fall ignore |
| t_{10} | 0 | ns min | SCLK falling edge to $\overline{\text{SYNC}}$ fall ignore |
| t_{11} | 10 | ns min | $\overline{\text{LDAC}}$ pulse width low |
| t_{12} | 15 | ns min | SCLK falling edge to $\overline{\text{LDAC}}$ rising edge |
| t_{13} | 5 | ns min | $\overline{\text{CLR}}$ pulse width low |
| t_{14} | 0 | ns min | SCLK falling edge to $\overline{\text{LDAC}}$ falling edge |
| t_{15} | 300 | ns typ | $\overline{\text{CLR}}$ pulse activation time |

¹ Maximum SCLK frequency is 50 MHz at $V_{DD} = 2.7 \text{ V}$ to 5.5 V . Guaranteed by design and characterization; not production tested.



¹ASYNCHRONOUS $\overline{\text{LDAC}}$ UPDATE MODE.
²SYNCHRONOUS $\overline{\text{LDAC}}$ UPDATE MODE.

Figure 2. Serial Write Operation

09463-002

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

| Parameter | Rating |
|---|---|
| V_{DD} to GND | -0.3 V to +7 V |
| Digital Input Voltage to GND | -0.3 V to $V_{DD} + 0.3$ V |
| V_{OUT} to GND | -0.3 V to $V_{DD} + 0.3$ V |
| V_{REFIN}/V_{REFOUT} to GND | -0.3 V to $V_{DD} + 0.3$ V |
| Operating Temperature Range Industrial | -55°C to $+125^\circ\text{C}$ |
| Storage Temperature Range | -65°C to $+150^\circ\text{C}$ |
| Junction Temperature ($T_{J\text{ MAX}}$) | 150°C |
| TSSOP Package | |
| Power Dissipation | $(T_{J\text{ MAX}} - T_A)/\theta_{JA}$ |
| θ_{JA} Thermal Impedance | 150.4°C/W |
| Reflow Soldering Peak Temperature | |
| SnPb | 240°C |
| Pb Free | 260°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

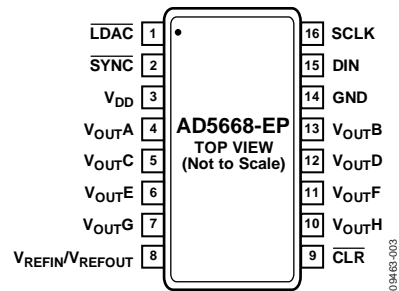


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

| Pin Number | Mnemonic |
|------------|---|
| 1 | LDAC |
| 2 | SYNC |
| 3 | V _{DD} |
| 4 | V _{OUTA} |
| 5 | V _{OUTC} |
| 6 | V _{OUTE} |
| 7 | V _{OUTG} |
| 8 | V _{REFIN} /V _{REFOUT} |
| 9 | CLR |
| 10 | V _{OUTH} |
| 11 | V _{OUTF} |
| 12 | V _{OUTD} |
| 13 | V _{OUTB} |
| 14 | GND |
| 15 | DIN |
| 16 | SCLK |

TYPICAL PERFORMANCE CHARACTERISTICS

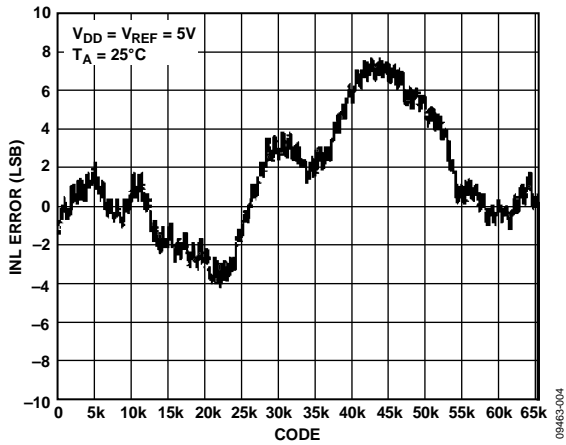


Figure 4. INL—External Reference

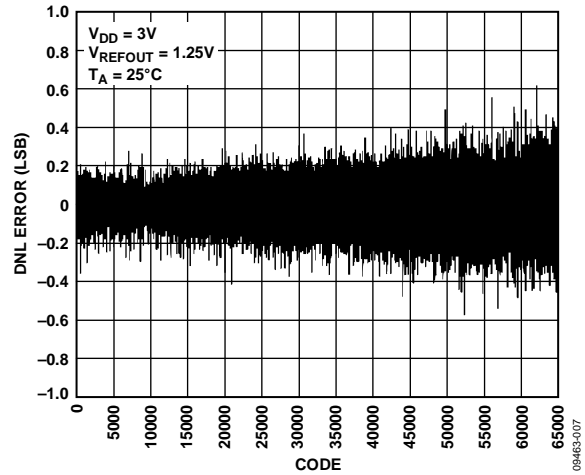


Figure 7. DNL

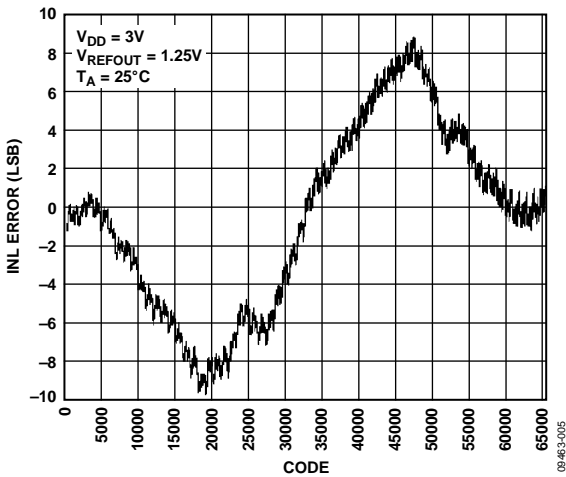


Figure 5. INL

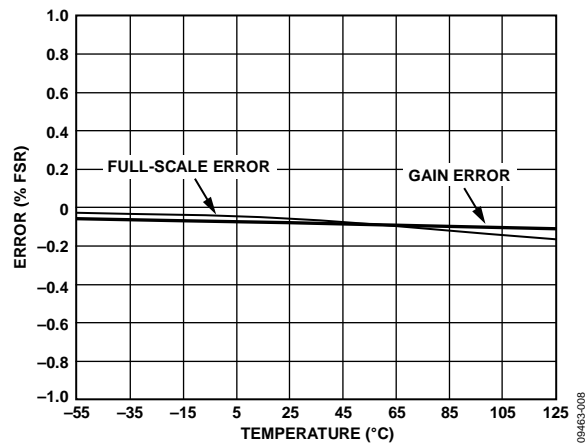


Figure 8. Gain Error and Full-Scale Error vs. Temperature

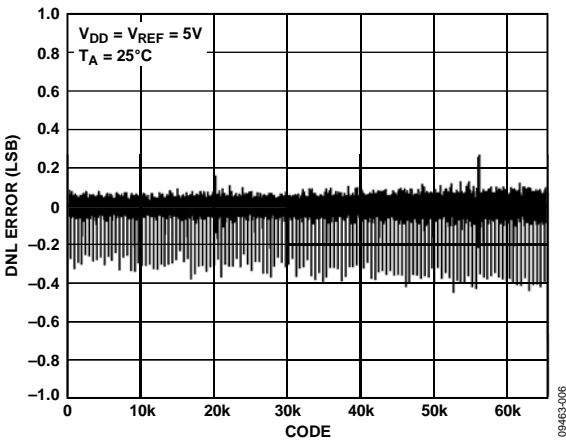


Figure 6. DNL—External Reference

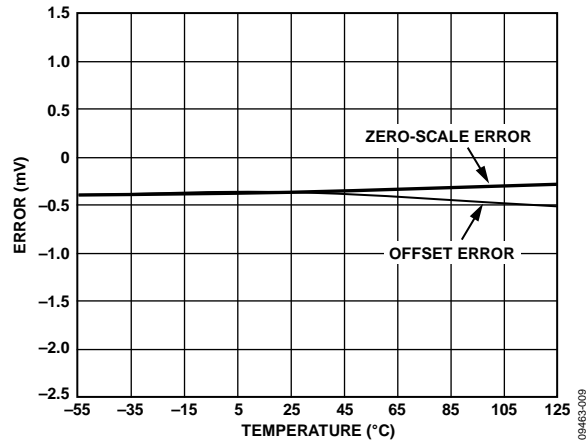


Figure 9. Zero-Scale Error and Offset Error vs. Temperature

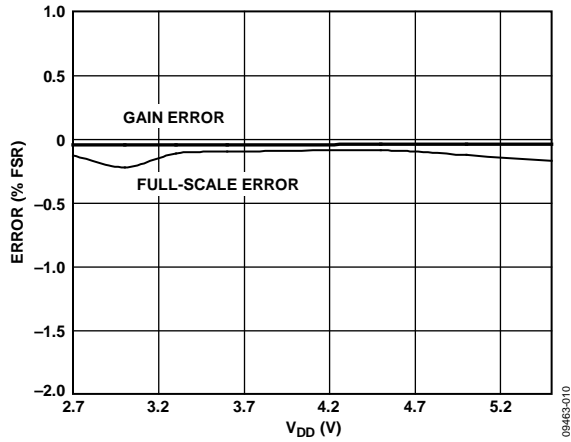


Figure 10. Gain Error and Full-Scale Error vs. Supply Voltage

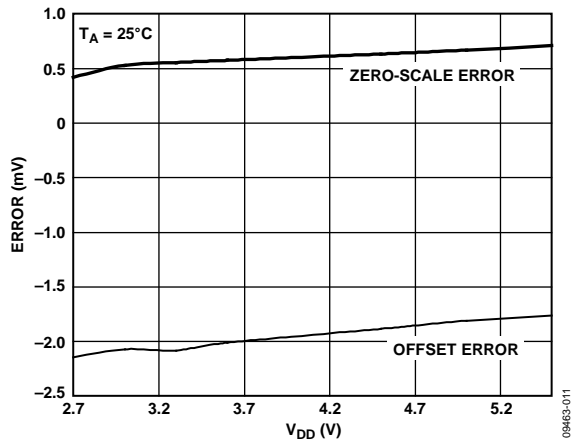


Figure 11. Zero-Scale Error and Offset Error vs. Supply Voltage

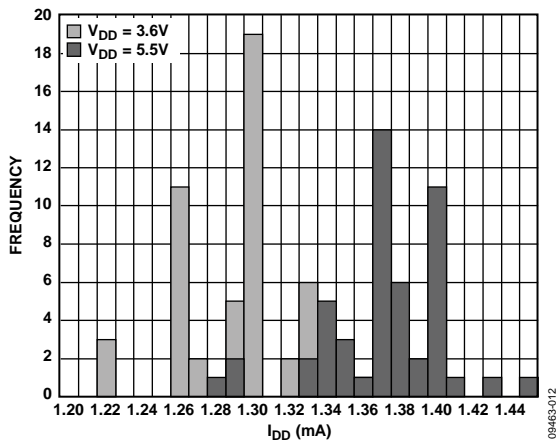


Figure 12. I_{DD} Histogram with External Reference

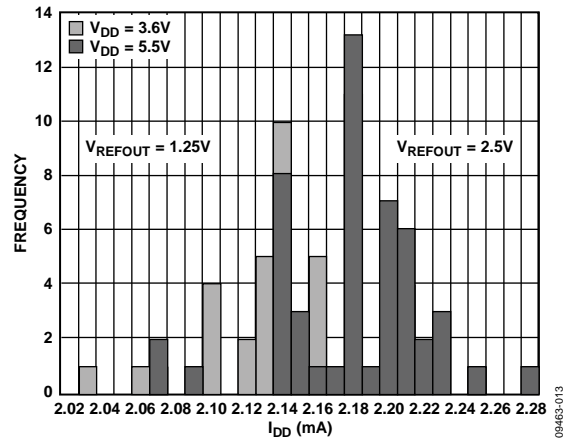


Figure 13. I_{DD} Histogram with Internal Reference

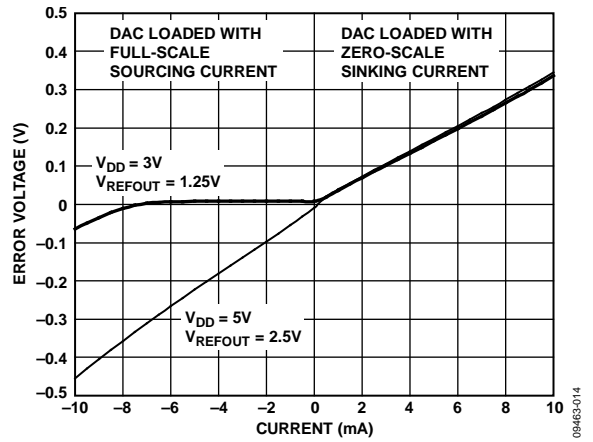


Figure 14. Headroom at Rails vs. Source and Sink

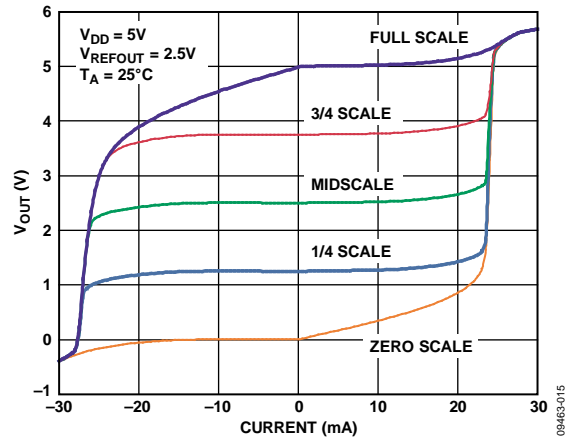


Figure 15. Source and Sink Capability

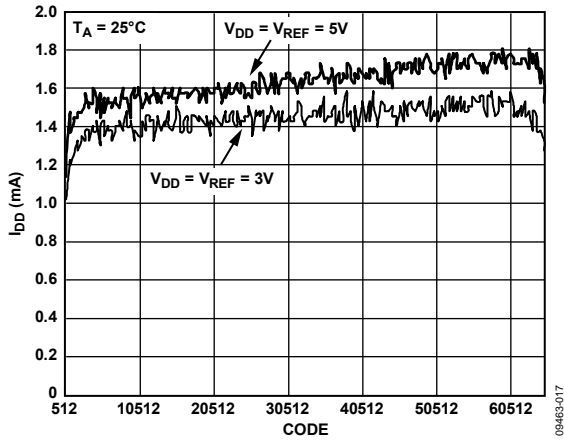


Figure 16. Supply Current vs. Code

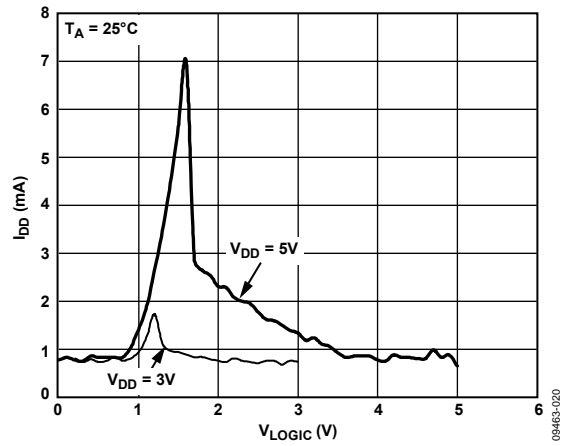


Figure 19. Supply Current vs. Logic Input Voltage

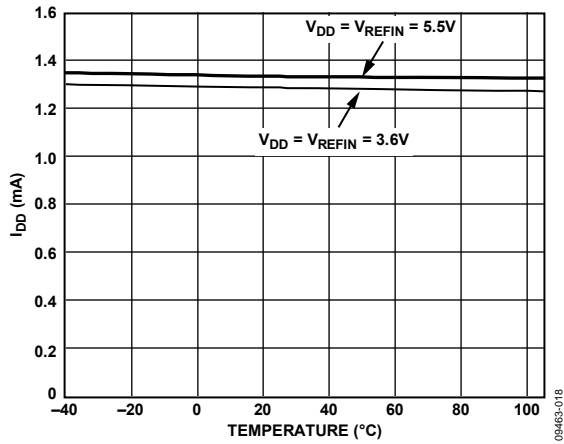


Figure 17. Supply Current vs. Temperature

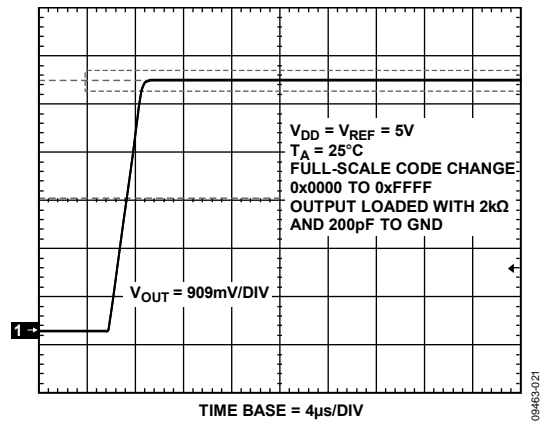


Figure 20. Full-Scale Settling Time, 5 V

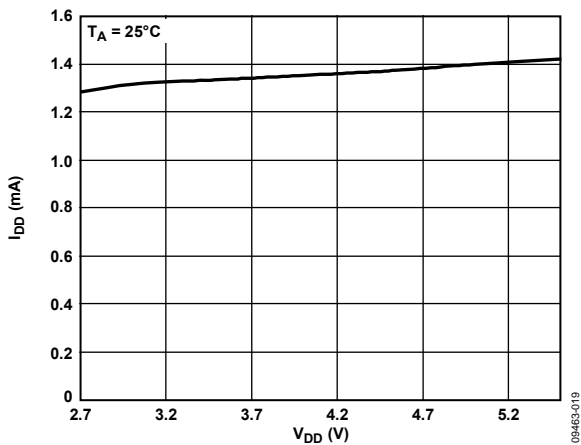


Figure 18. Supply Current vs. Supply Voltage

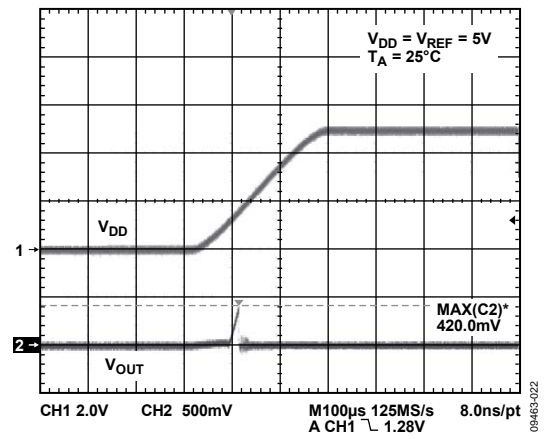


Figure 21. Power-On Reset to 0 V

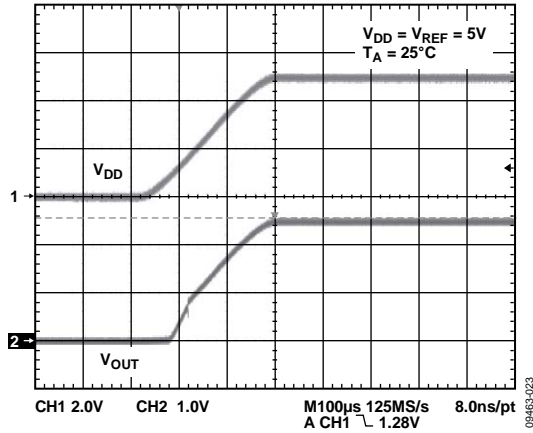


Figure 22. Power-On Reset to Midscale

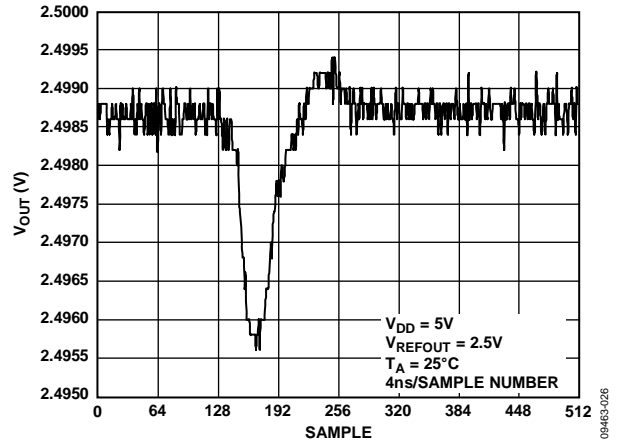


Figure 25. Analog Crosstalk

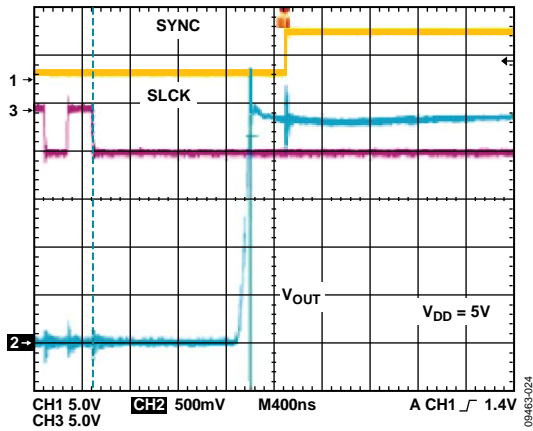


Figure 23. Exiting Power-Down to Midscale

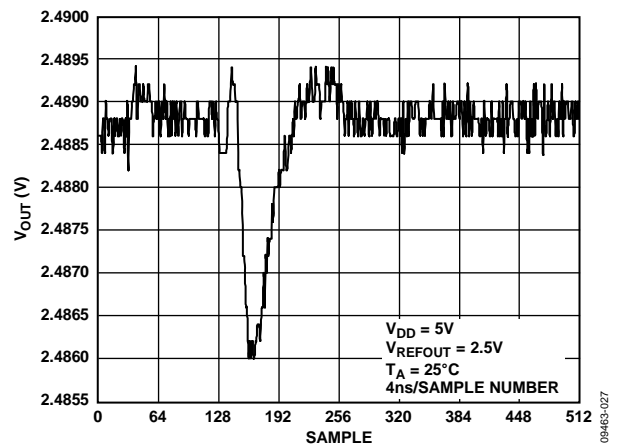


Figure 26. DAC-to-DAC Crosstalk

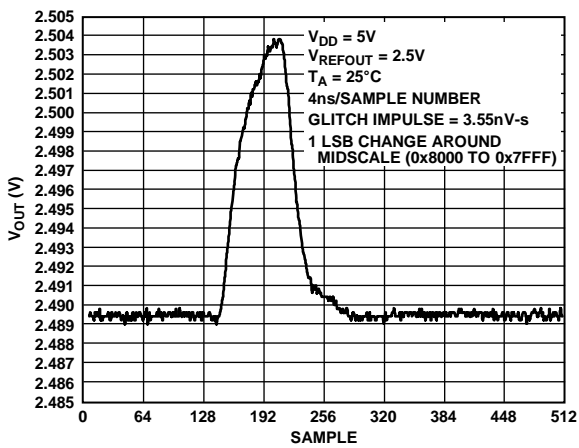


Figure 24. Digital-to-Analog Glitch Impulse (Negative)

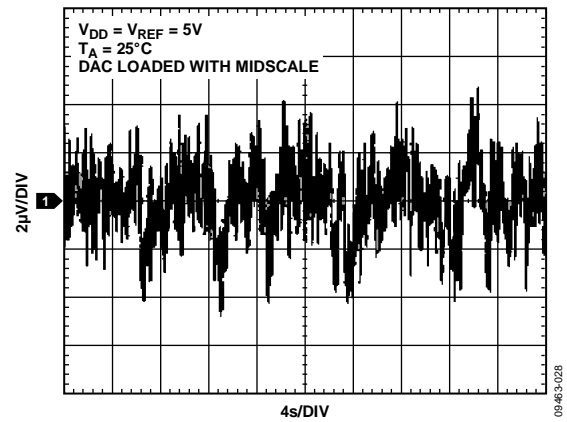


Figure 27. 0.1 Hz to 10 Hz Output Noise Plot, External Reference

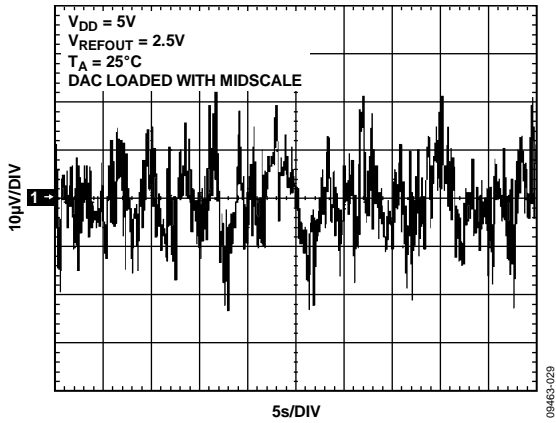


Figure 28. 0.1 Hz to 10 Hz Output Noise Plot, Internal Reference

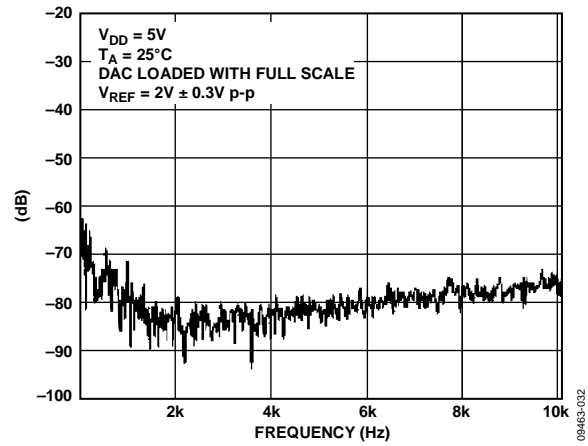


Figure 31. Total Harmonic Distortion

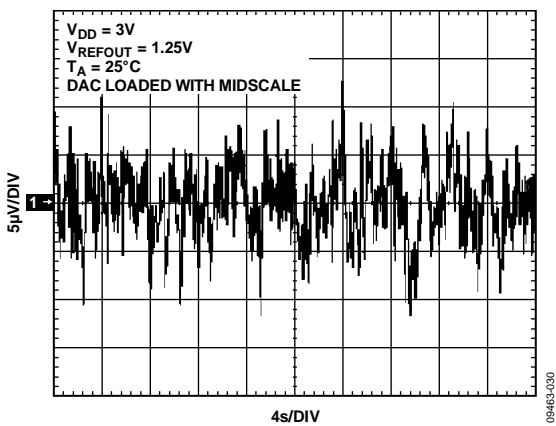


Figure 29. 0.1 Hz to 10 Hz Output Noise Plot, Internal Reference

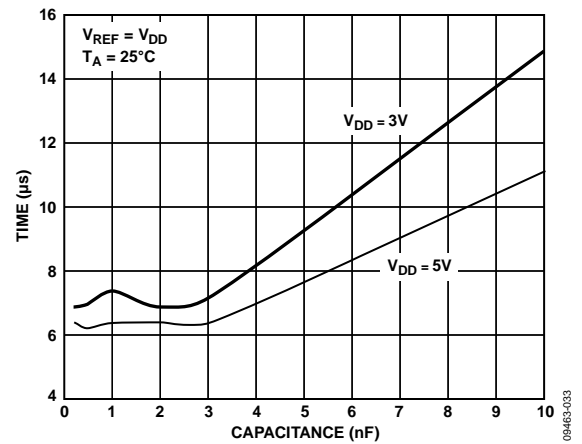


Figure 32. Settling Time vs. Capacitive Load

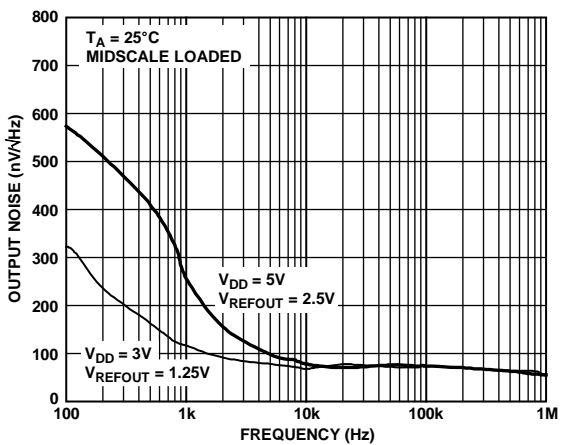


Figure 30. Noise Spectral Density, Internal Reference

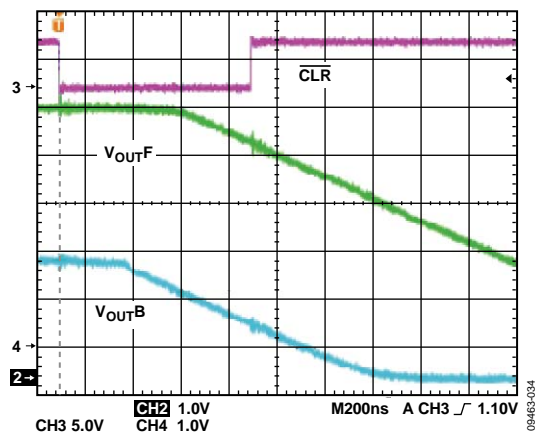


Figure 33. Hardware CLR

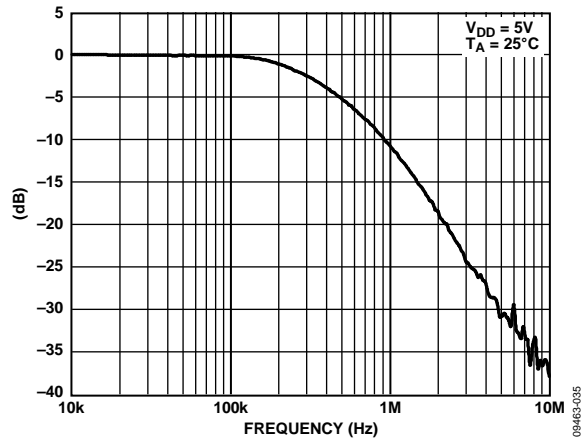
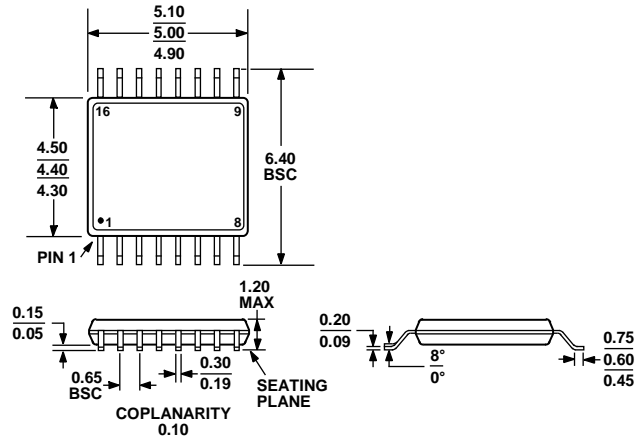


Figure 34. Multiplying Bandwidth

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 35. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Power-On Reset to Code | Accuracy | Internal Reference |
|-------------------|-------------------|---------------------|----------------|------------------------|-------------|--------------------|
| AD5668SRU-EP-1 | -55°C to +125°C | 16-Lead TSSOP | RU-16 | Zero | ±21 LSB INL | 1.25 V |
| AD5668SRU-EP-1RL7 | -55°C to +125°C | 16-Lead TSSOP | RU-16 | Zero | ±21 LSB INL | 1.25 V |