HV7351

8-Channel, ±70V, 3A Programmable High-Voltage Ultrasound-Transmit Beamformer

Features

- Eight Channels with Return-to-Zero (RTZ)
- Up to ±70V Output Voltage
- ±3.0A Output Current
- Stores up to Four Different Patterns
- Independent Programmable Delays
- 80-lead Single 11 x 11 mm VQFN Package

Applications

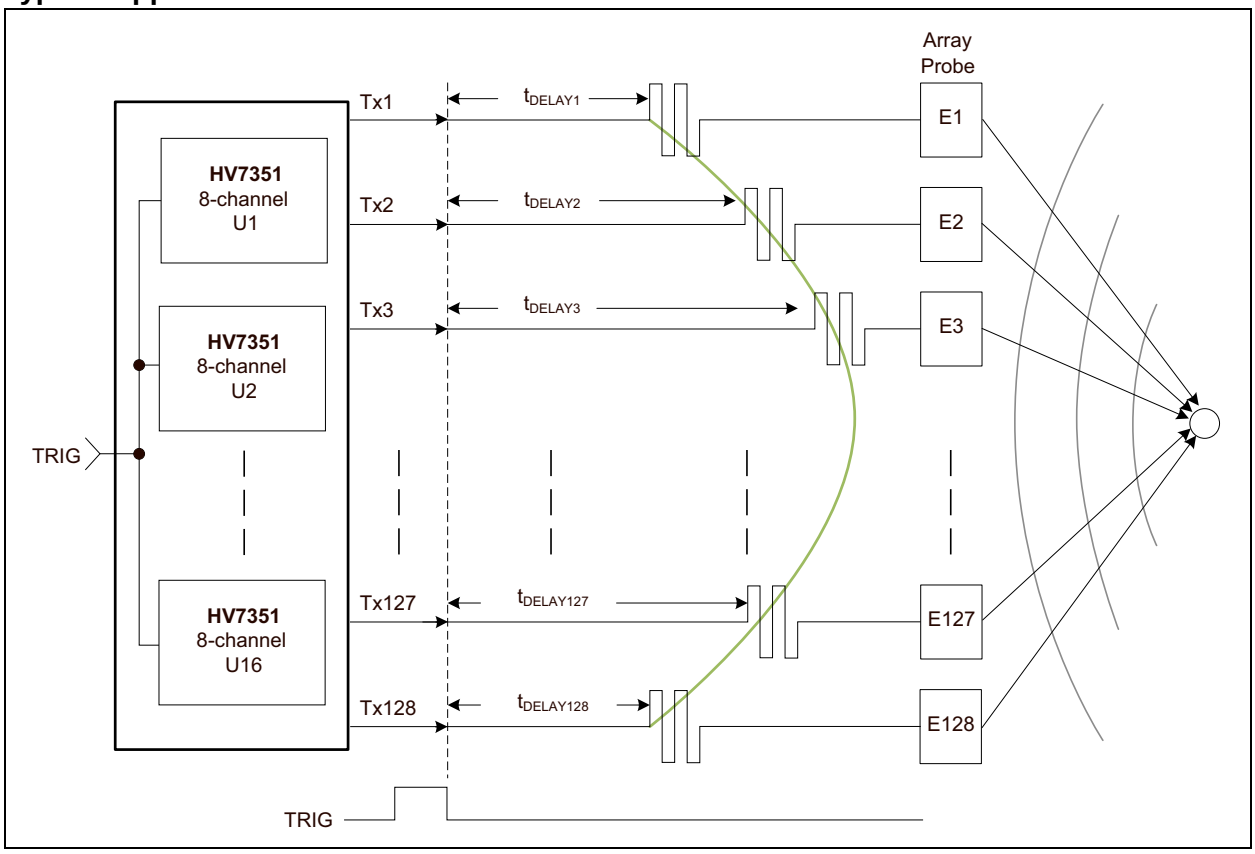
- Medical Ultrasound Imaging
- NDT, Non-Destructive Testing
- Arbitrary Pattern Generator
- High-Speed PIN Diode Driver

General Description

The HV7351 device is an 8-channel programmable high-voltage ultrasound-transmit beamformer. Each channel is capable of swinging up to ±70V with an active discharge back to 0V. The outputs can source and sink up to 3.0A to achieve fast output rise and fall times. The active discharge is also capable of sourcing and sinking 3.0A for a fast return to ground. The topology of the HV7351 will significantly reduce the number of I/O logic control lines needed.

Each pulser has four associated 64-bit shift registers for storing predetermined transmit patterns and a 10-bit delay counter for controlling the transmit time. One of four arbitrary patterns can be transmitted with adjustable delay, depending on the data loaded into these shift registers and the delay counter. The delay counter can be clocked up to 200 MHz, allowing incremental delays down to 5 ns.

Typical Application Circuit



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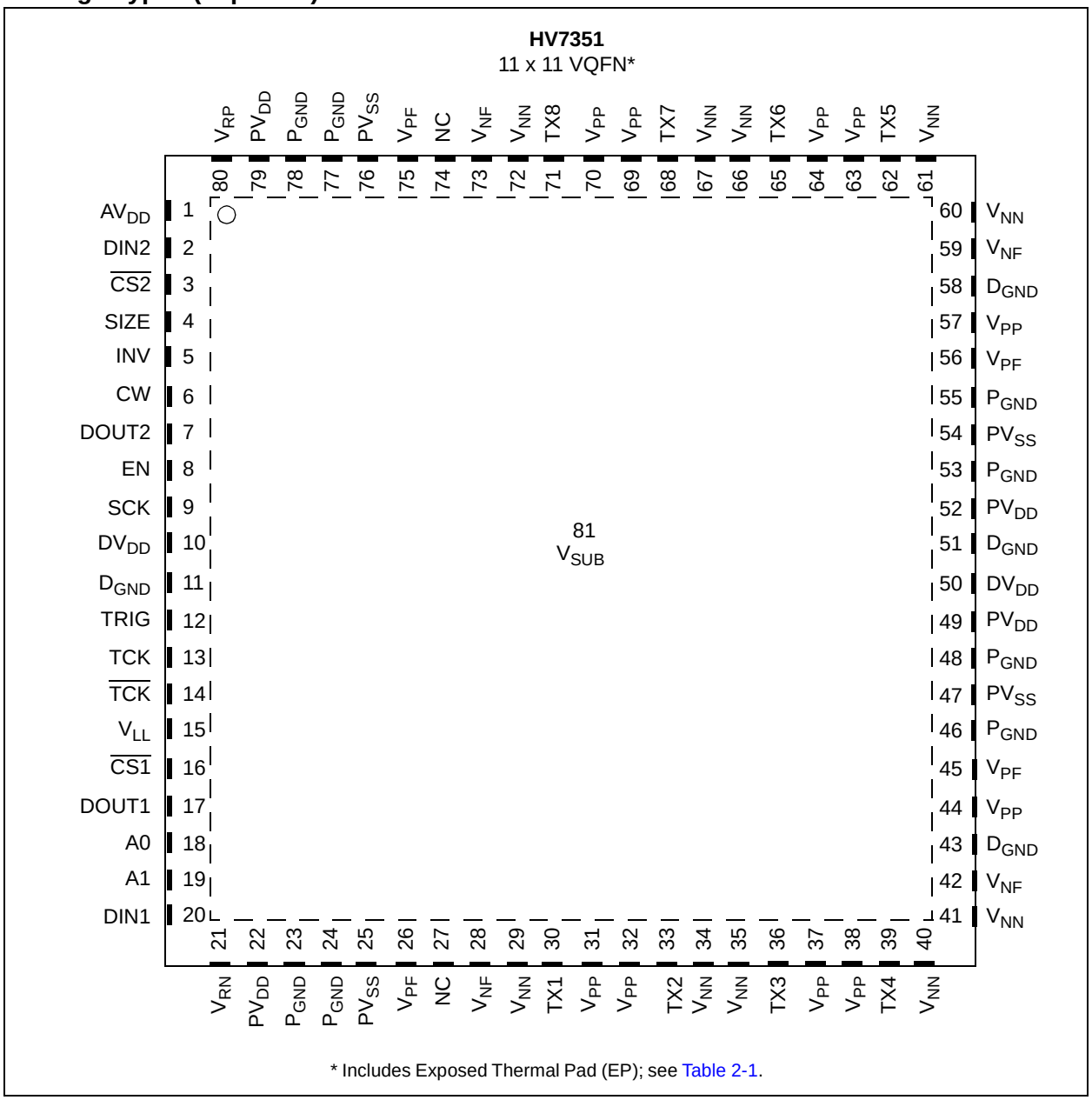
Package Types (Top View)



* Includes Exposed Thermal Pad (EP); see Table 2-1.

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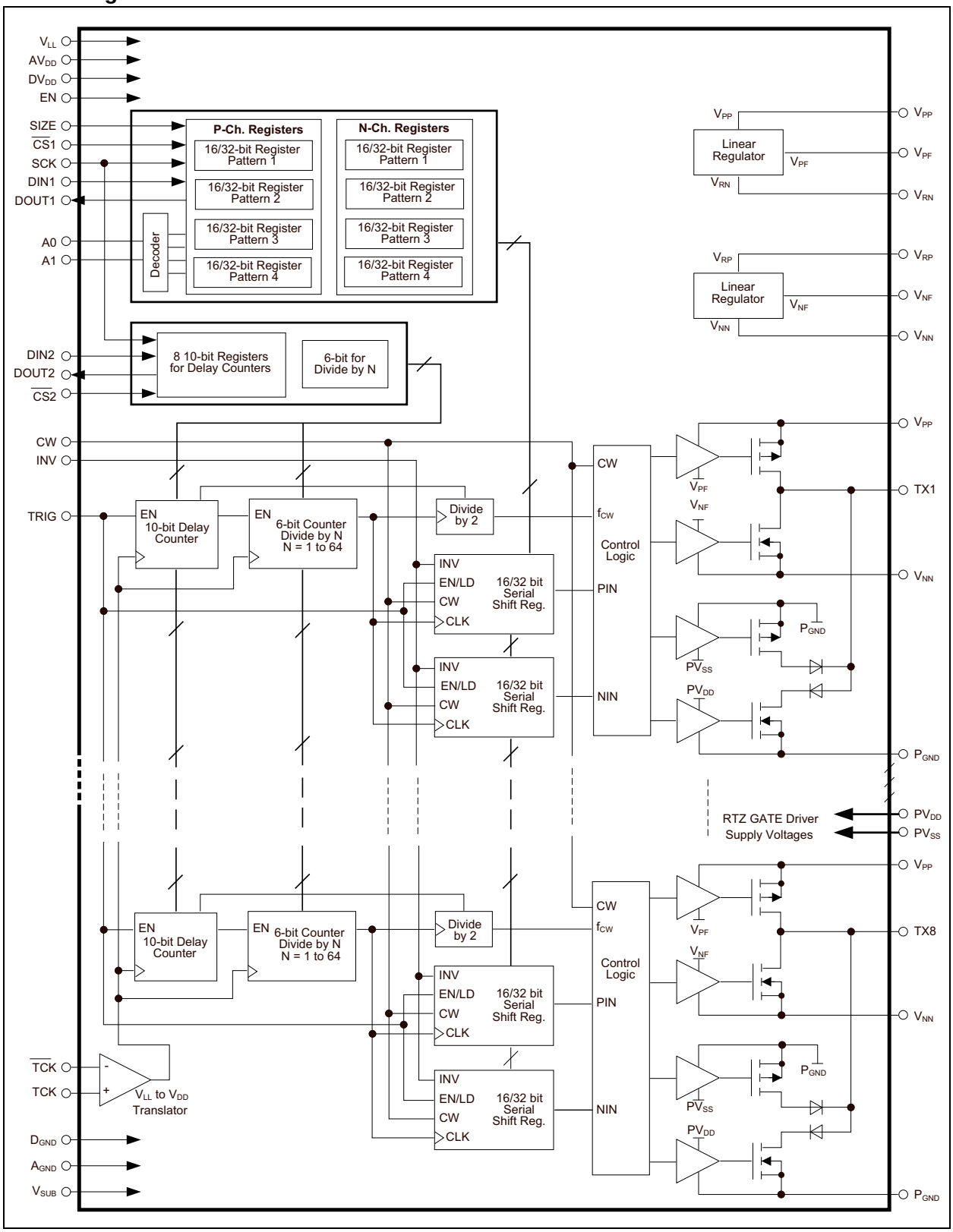
Block Diagram



NOTES:

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Positive logic supply (V_{LL}) ..... -0.5V to 5.5V
Positive logic supply voltage (DV_{DD}) ..... -0.5V to 5.5V
Positive gate drive supply voltage (PV_{DD}) ..... -0.5V to 5.5V
Positive analog supply voltage (AV_{DD}) ..... -0.5V to 5.5V
Negative gate drive supply voltage (PV_{SS}) ..... +0.5V to -5.5V
High-voltage positive supply voltage (V_{PP}) ..... -0.5V to +80V
High-voltage negative supply voltage (V_{NN}) ..... +0.5V to -80V
Differential high voltage supply (V_{PP} - V_{NN}) ..... +160V
Positive floating supply voltage (V_{PF}) ..... V_{PP} – 6.0V to V_{PP}
Negative floating supply voltage (V_{NF}) ..... V_{NN} to V_{NN} + 6.0V
Positive supply for V_{NF} regulator (V_{RP}) ..... 0V to 15V
Negative supply for V_{PF} regulator (V_{RN}) ..... 0V to -15V
Operating temperature ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
ESD Rating All Pins ..... 0.75 kV

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: OPERATING SUPPLY VOLTAGES

Electrical Specifications: Unless otherwise specified: T_A = +25°C. **Boldface** specifications apply over the T_A range of -20 to +85°C.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Positive High Voltage Supply	V_{PP}	**3.0**	—	**70**	V	**Note 1**
Negative High Voltage Supply	V_{NN}	**-70**	—	**-3.0**	V	
Logic Interface Voltage	V_{LL}	**2.85**	3.30	**3.6**	V	
Low-Voltage Positive Analog Supply Voltage	AV_{DD}	**4.75**	5.00	**5.25**	V	
Low-Voltage Positive Digital Supply Voltage	DV_{DD}	**4.75**	5.00	**5.25**	V	
Low-Voltage Positive Gate Drive Supply Voltage	PV_{DD}	**4.75**	5.00	**5.25**	V	
Low-Voltage Negative Gate Drive Supply Voltage	PV_{SS}	**-5.25**	-5.00	**-4.75**	V	
Low-Voltage Positive Supply for V_{NF} Regulator	V_{RP}	**4.75**	—	**12**	V	
Low-Voltage Negative Supply for V_{PF} Regulator	V_{RN}	**-12**	—	**-4.75**	V	
Reference Voltage Logic Trip Point for $\overline{TCK}$ Pin	$\overline{TCK}$	**0.4V_{LL}**	0.5V_{LL}	**0.6V_{LL}**	V	
TCK/$\overline{TCK}$ Input Current	I_{TCK}/$I_{\overline{TCK}}$	—	—	±10	µA	$I_{\overline{TCK}}$ = 0 to V_{LL}, T_A = +25°C (**Note 1**)

Note 1: Specification is obtained by characterization and is not 100% tested.

TABLE 1-2: REGULATOR OUTPUTS

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Positive Floating Gate Drive Voltage	V_{PF}	V_{PP} - 5.25	V_{PP} - 5.00	V_{PP} - 4.00	V	4x1 µF ceramic capacitors across V_{PF} and V_{PP}
Negative Floating Gate Drive Voltage	V_{NF}	V_{NN} + 4.00	V_{NN} + 5.00	V_{NN} + 5.25	V	4x1 µF ceramic capacitors across V_{NF} and V_{NN}

ELECTRICAL CHARACTERISTICS

Electrical Specifications: unless otherwise specified, V_{LL} = 3.3V, AV_{DD} = DV_{DD} = PV_{DD} = V_{RP} = 5.0V, PV_{SS} = V_{RN} = -5.0V, V_{PP} = +70V, V_{NN} = -70V, T_A = +25°C.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
V_{LL} Quiescent Current	I_{VLLQ}	—	384	500	µA	EN = Low, all inputs are static
AV_{DD} Quiescent Current	I_{AVDDQ}	—	12	30	µA	EN = Low, all inputs are static
DV_{DD} Quiescent Current	I_{DVDDQ}	—	12	30		
PV_{DD} Quiescent Current	I_{PVDDQ}	—	70	100		
V_{RP} Quiescent Current	I_{VRPQ}	—	0.3	6	µA	EN = Low, all inputs are static
V_{RN} Quiescent Current	I_{VRNQ}	—	-0.01	6		
PV_{SS} Quiescent Current	I_{PVSSQ}	-85	-45	—	µA	EN = Low, all inputs are static
V_{PP} Quiescent Current	I_{VPPQ}	—	2.6	6	µA	EN = Low, all inputs are static
V_{NN} Quiescent Current	I_{VNNQ}	—	-1.6	6		
V_{LL} Enabled Quiescent Current	I_{VLLEN}	—	390	500	µA	EN = High, all inputs are static
AV_{DD} Enabled Quiescent Current	I_{AVDDEN}	—	600	800	µA	EN = High, all inputs are static
DV_{DD} Enabled Quiescent Current	I_{DVDDEN}	—	22	55		
PV_{DD} Enabled Quiescent Current	I_{PVDDEN}	—	44	100	µA	EN = High, all inputs are static
V_{RP} Enabled Quiescent Current	I_{VRPEN}	—	450	650	µA	EN = High, all inputs are static
V_{RN} Enabled Quiescent Current	I_{VRNEN}	-650	-350	—		
PV_{SS} Enabled Quiescent Current	I_{PVSSEN}	-100	-44	—	µA	EN = High, all inputs are static
V_{PP} Enabled Quiescent Current	I_{VPPEN}	—	370	620	µA	EN = High, all inputs are static
V_{NN} Enabled Quiescent Current	I_{VNNEN}	-620	-420	—		
V_{LL} current at 80 MHz Clock	I_{VLLCW}	—	500	—	µA	V_{PP} = +5.0V, V_{NN} = -5.0V, EN = High, CW = High, 80 MHz on $\overline{TCK}$, 0.5V_{LL} on $\overline{TCK}$, all 8 channels active at 5.0 MHz, no load (**Note 1**)
DV_{DD} current at CW = 5 MHz	I_{DVDDCW}	—	25	—	mA	
V_{PP} current at CW = 5 MHz	I_{VPPCW}	—	141	—	mA	
V_{NN} current at CW = 5 MHz	I_{VNNCW}	—	98	—	mA	

Note 1: Specification is obtained by characterization and is not 100% tested.

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AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: unless otherwise specified, V_{LL} = 3.3V, AV_{DD} = DV_{DD} = PV_{DD} = V_{RP} = 5.0V, PV_{SS} = V_{RN} = -5.0V, V_{PP} = +70V, V_{NN} = -70V, T_A = +25°C.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Transmit Clock Frequency	f_{TCK}	0	—	200	MHz	
Serial Clock Frequency	f_{SCK}	0	—	80	MHz	No daisy chain
		0	—	70		Daisy chained (**Note 2**)
Set-up Time Data into SCK	t_{SU-DIN}	2	—	—	ns	**Note 1**
Hold Time SCK to Data In	t_{H-DIN}	2	—	—	ns	**Note 1**
Set-up Time $\overline{CS1}$ Low to SCK	t_{SU-CS1}	2	—	—	ns	**Note 2**
Set-up Time $\overline{CS2}$ Low to SCK	t_{SU-CS2}	2	—	—	ns	**Note 2**
Set-up Time from TRIG Fall to TCK Rise Edge	$t_{SU-TRIG}$	2	—	—	ns	**Note 2**
TRIG Pulse Width	t_{W-TRIG}	2 x TCK	—	—	Cycle	**Note 2**
SCK to Data Out Low to High Delay Time	t_{LHDO}	3	9	12	ns	For DOUT1 (**Note 1**)
		3	9	10		For DOUT2 (**Note 1**)
SCK to Data Out High to Low Delay Time	t_{HLDO}	3	9	12	ns	For DOUT1 (**Note 1**)
		3	9	10		For DOUT2 (**Note 1**)
A1A0 Pulse Width	t_{WA1A0}	t_{W-TRIG} + 40	—	—	ns	**Note 2**
Set-up Time A1A0 to TRIG Rising Edge	t_{SUA1A0}	—	20	—	ns	**Note 1**
Hold Time A1A0 to TRIG Falling Edge	t_{HA1A0}	—	20	—	ns	
Device Enable Time	t_{EN-ON}	—	1	—	ms	1.0 µF capacitor on every V_{PF} and V_{NF} pin (**Note 1**)
Device Disable Time	t_{EN-OFF}	—	—	100	ns	**Note 1**
Output Rise Time from 0V to +HV	t_{r1}	—	9	13	ns	Load = 330 pF||2.5 kΩ
Output Fall Time from 0V to -HV	t_{f1}	—	9	13	ns	
Damping Output Rise Time from -HV to 0V	t_{r2}	—	9	13	ns	
Damping Output Fall Time from +HV to 0V	t_{f2}	—	9	13	ns	
Output Rise Time from -HV to +HV	t_{r3}	—	17	23	ns	
Output Fall Time from +HV to -HV	t_{f3}	—	17	23	ns	
CW Output Rise Time	t_{rcw}	—	9	16	ns	V_{PP} = +5.0V, V_{NN} = -5.0V Load = 330 pF||2.5 kΩ
CW Output Fall Time	t_{fcw}	—	9	16	ns	

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2: Specification is for design guidance only.

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AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: unless otherwise specified, V_{LL} = 3.3V, AV_{DD} = DV_{DD} = PV_{DD} = V_{RP} = 5.0V, PV_{SS} = V_{RN} = -5.0V, V_{PP} = +70V, V_{NN} = -70V, T_A = +25°C.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Output Propagation Delay Rise Time 1	t_{dr1}	11	14	18	ns	No Load
Output Propagation Delay Fall Time 1	t_{df1}	11	14	18	ns	
Output Propagation Delay Rise Time 2	t_{dr2}	12	15	19	ns	
Output Propagation Delay Fall Time 2	t_{df2}	11	15	18	ns	
Output Propagation Delay Rise Time 3	t_{dr3}	12	15	19	ns	
Output Propagation Delay Fall Time 3	t_{df3}	11	15	18	ns	
CW Output Propagation Delay Time from Low to High	t_{dcwlh}	10	13	17	ns	V_{PP} = +5.0V, V_{NN} = -5.0V No Load
CW Output Propagation Delay Time from High to Low	t_{dcwhl}	10	14	17	ns	
Delay Time Matching	Δt_{dcwhl}	—	±0.7	—	ns	P to N, channel-to-channel matching
Delay Jitter On Rise or Fall	t_{JCW}	—	13	—	ps	V_{PP} = +5.0V, V_{NN} = -5.0V, Load = 50Ω (**Note 2**)
Latency	LAT		3.5		TCK	**Note 2**
Output P-Channel MOSFET to V_{PP}, CW = 0						
Output Saturation Current	I_{OUT}	2.2	3.2	—	A	
Output ON-Resistance	R_{ON}	—	4.2	—	Ω	I_{OUT} = 100 mA
Output Capacitance	C_{OSS}	—	62	—	pF	V_{PP} - V_{OUT} = 25V, f = 1.0 MHz (**Note 2**)
Output N-Channel MOSFET to V_{NN}, CW = 0						
Output Saturation Current	I_{OUT}	2.2	3.2	—	A	
Output ON-Resistance	R_{ON}	—	2.4	—	Ω	I_{OUT} = -100 mA
Output Capacitance	C_{OSS}	—	50	—	pF	V_{NN} - V_{OUT} = -25V, f = 1.0 MHz (**Note 2**)
Output P-Channel MOSFET to V_{PP}, CW = 1						
Output Saturation Current	I_{OUT}	1.2	1.5	—	A	
Output ON-Resistance	R_{ON}	—	8	—	Ω	I_{OUT} = 100 mA
Output Capacitance	C_{OSS}	—	62	—	pF	V_{PP} - V_{OUT} = 25V, f = 1.0 MHz (**Note 2**)

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AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: unless otherwise specified, V_{LL} = 3.3V, AV_{DD} = DV_{DD} = PV_{DD} = V_{RP} = 5.0V, PV_{SS} = V_{RN} = -5.0V, V_{PP} = +70V, V_{NN} = -70V, T_A = +25°C.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Output N-Channel MOSFET to V_{NN}, CW = 1						
Output Saturation Current	I_{OUT}	1.2	1.5	—	A	
Output ON-Resistance	R_{ON}	—	6.6	—	Ω	I_{OUT} = -100 mA
Output Capacitance	C_{OSS}	—	50	—	pF	V_{NN} - V_{OUT} = -25V, f = 1.0 MHz (**Note 2**)
Damping P-Channel MOSFET to P_{GND}						
Output Saturation Current	I_{OUT}	2.2	3.2	—	A	
Output ON-Resistance	R_{ON}	—	4	—	Ω	I_{OUT} = 100 mA
Output capacitance	C_{OSS}	—	62	—	pF	V_{PP} - V_{OUT} = 25V, f = 1.0 MHz (**Note 2**)
Damping N-Channel MOSFET to P_{GND}						
Output Saturation Current	I_{OUT}	2.2	3.2	—	A	
Output ON-Resistance	R_{ON}	—	2.3	—	Ω	I_{OUT} = -100 mA
Output Capacitance	C_{OSS}	—	50	—	pF	V_{NN} - V_{OUT} = -25V, f = 1.0 MHz (**Note 2**)
Logic Inputs						
Clock Input Current	$I_{\overline{TCK}}$	—	±1.0	—	µA	Voltage 0 to V_{LL}
Clock Input High Voltage	V_{IH_TCK}	$V_{\overline{TCK}}$ + 0.15	—	V_{LL}	V	$\overline{TCK}$ = 0.5V_{LL} (**Note 2**)
Clock Input Low Voltage	V_{IL_TCK}	0	—	$V_{\overline{TCK}}$ - 0.15	V	
Logic Input High Voltage	V_{IH}	0.8V_{LL}	—	V_{LL}	V	For all logic inputs except clock inputs
Logic Input Low Voltage	V_{IL}	0	—	0.2V_{LL}	V	
Input Logic High Current	I_{IH}	—	—	1	µA	
Input Logic Low Current	I_{IL}	-1	—	—	µA	
Output Logic Low Voltage	V_{OL}	0	—	0.7	V	I_{OUT} = 0 to -10 mA
Output Logic High Voltage	V_{OH}	V_{LL} - 0.7	—	V_{LL}	V	I_{OUT} = 0 to 10 mA
Input Logic Capacitance	C_{IN}	—	—	5.0	pF	**Note 2**

Note 1: Specification is obtained by characterization and is not 100% tested.

2: Specification is for design guidance only.

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TEMPERATURE SPECIFICATIONS

Electrical Specifications: unless otherwise specified, V_{LL} = 3.3V, AV_{DD} = DV_{DD} = PV_{DD} = V_{RP} = 5.0V, PV_{SS} = V_{RN} = -5.0V, V_{PP} = +70V, V_{NN} = -70V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Ambient Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Maximum Junction Temperature	T_J	-40	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 80L-11x11 VQFN	θ_{JA}	—	14	—	°C/W	

TABLE 1-3: LOGIC TRUTH TABLE

Mode	Inputs						Outputs			Comments
	EN	CW	10-bit Counter	INV	NIN	PIN	N-Ch.	P-Ch.	RTZ	
Non-CW mode. Outputs not inverted. Outputs are controlled by data in the shift registers	1	0	X	X	0	0	OFF	OFF	ON	Return-to-Zero (RTZ) is activated when NIN and PIN are both low. Output is pulled to ground through a series diode.
	1	0	X	0	0	1	OFF	ON	OFF	Not inverted. Logic 1 in the P-Channel register turns on the output P-Channel MOSFET.
	1	0	X	0	1	0	ON	OFF	OFF	Not inverted. Logic 1 in the N-Channel register turns on the output N-Channel MOSFET.
	1	0	X	X	1	1	OFF	OFF	OFF	Avoids cross overcurrent. A logic 1 in both P- and N-Channel registers will put the output in a High Z state.
Non-CW mode. Outputs are inverted. Outputs are controlled by data in the shift registers	1	0	X	1	0	1	ON	OFF	OFF	Transmit pattern is inverted
	1	0	X	1	1	0	OFF	ON	OFF	
CW mode. Output follows f_{CW}	1	X	All 1	X	X	X	OFF	OFF	OFF	If 10-bit counter reach all 1, then the channel will be turned OFF.
	1	1	Not all 1	X	X	X	OFF/ ON	ON/ OFF	OFF	The channel's output follows the f_{CW} signal. The shift registers for PIN and NIN remain static to save power.
Device Disabled	0	X	X	X	X	X	OFF	OFF	OFF	High Z state

Legend: X = Don't care.

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1.1 Timing Diagrams

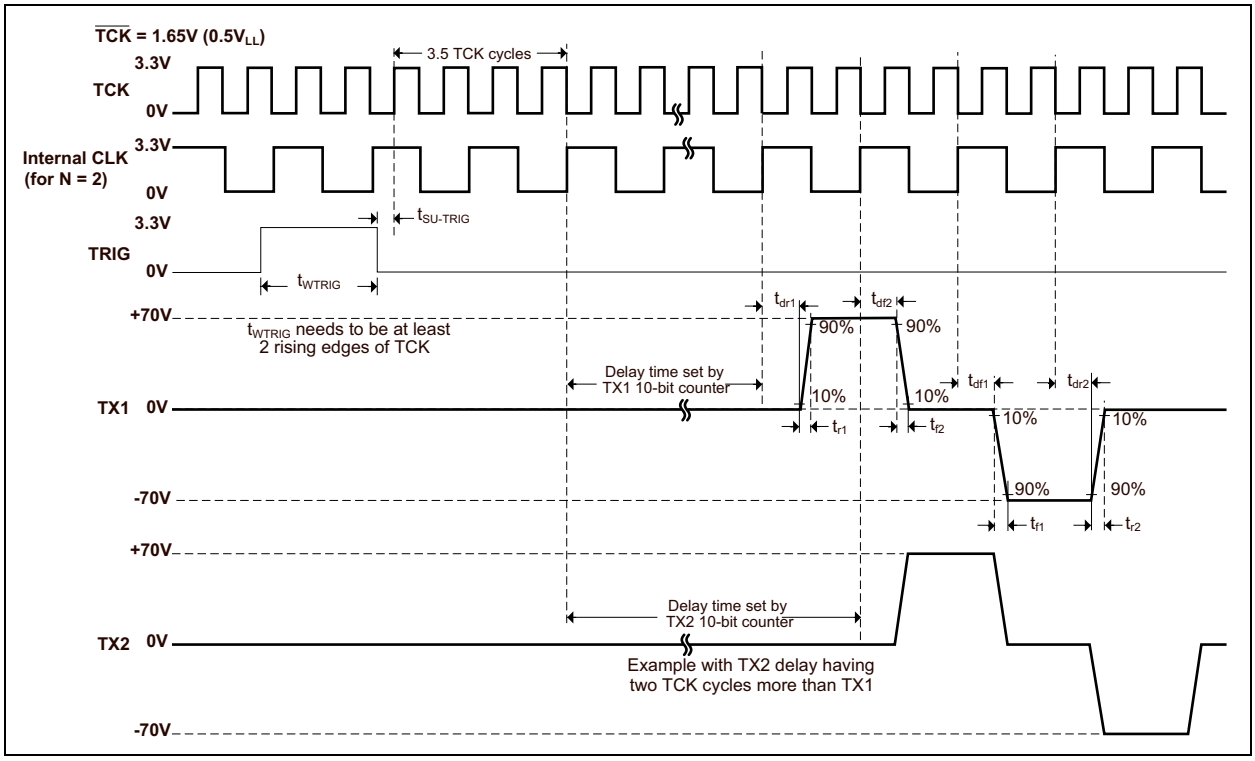

FIGURE 1-1: *Timing Diagram of 3-Level, 1-Cycle Bipolar RTZ TX Pulse.*

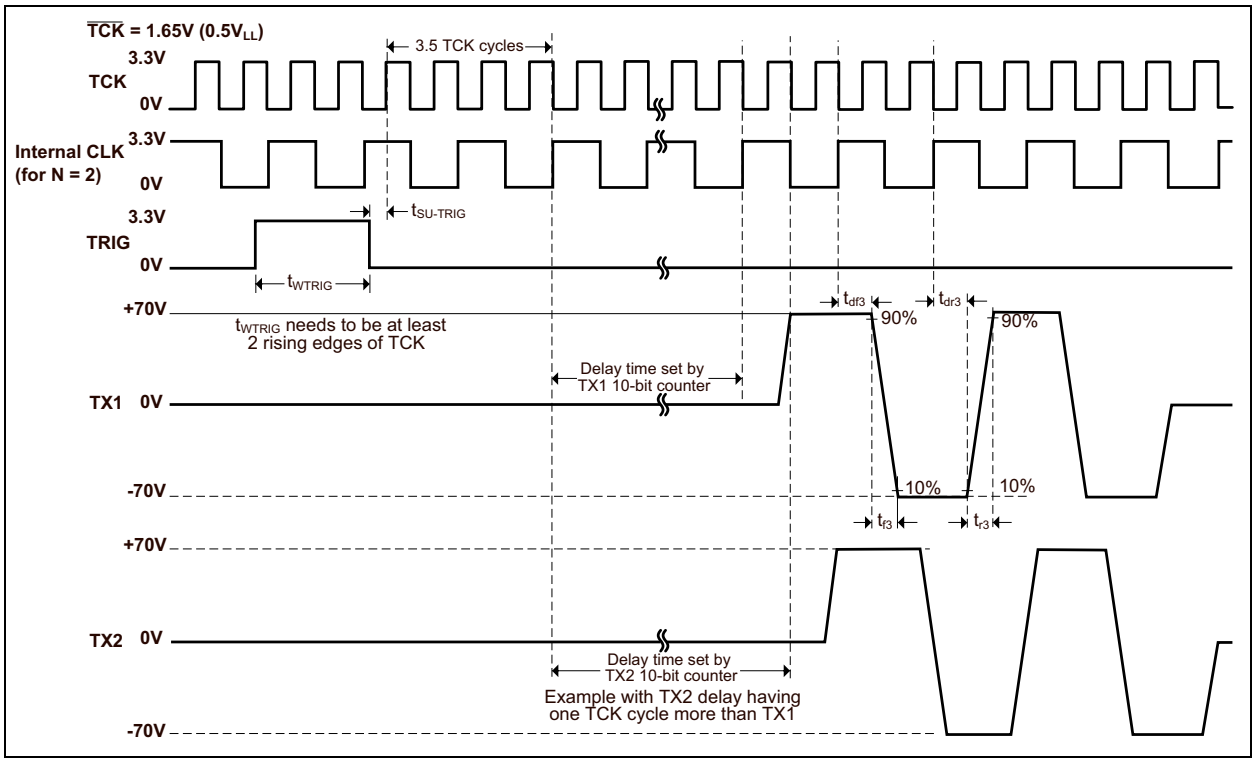

FIGURE 1-2: *Timing Diagram of 2-Level 2-Cycle Bipolar, non-RTZ TX Pulses with Damping.*

NOTES:

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2.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin	Symbol	Description
1	AV_{DD}	Positive analog supply voltage (+5.0V)
2	DIN2	Serial data in for delay counters and frequency divider
3	$\overline{CS2}$	Activates DIN2. Input logic high = off, input logic low = on.
4	SIZE	Sets pattern width to either 16-bits or 32-bits. Logic low = 16-bits, logic high = 32-bits.
5	INV	Inverts the TX output waveform. See Table 1-3 for details.
6	CW	Activates CW mode. Logic low = non-CW mode, logic high = CW mode. See Table 1-3 for details.
7	DOUT2	Data out for delay counters and frequency divider
8	EN	Enables and disables device. Logic low = off, logic high = on.
9	SCK	Serial clock input for serial shift registers
10, 50	DV_{DD}	Positive digital supply voltage (+5.0V)
11, 43, 51, 58	D_{GND}	Digital ground
12	TRIG	Toggles all TX outputs to transmit. Needs to be high for two rising edges of TCK. Delay counters will start on the rising edge of the TCK pin right after the falling edge of the TRIG signal. See **Section 1.1 "Timing Diagrams"** for details.
13	TCK	The TCK and $\overline{TCK}$ pins can be driven by LVDS or SSTL types of output in a differential manner. The TCK pin can be driven by LVCMOS single-ended output, while setting the $\overline{TCK}$ to GND (or DC value of 0.4V to 0.6V). The logic trip point is on the TCK rising edge and on the $\overline{TCK}$ falling edge, crossing in the differential manner. In the single-ended case, the trip point is on the TCK rising edge.
14	$\overline{TCK}$	
15	V_{LL}	Logic interface supply voltage (3.3V)
16	$\overline{CS1}$	Activates DIN1. Input logic high = off, input logic low = on
17	DOUT1	Data out for P-Channel and N-Channel pattern registers
18	A0	Decoded to select 1 of 4 patterns to be loaded
19	A1	
20	DIN1	Serial data in for P-Channel and N-Channel pattern registers
21	V_{RN}	Negative supply for V_{PF} regulator (-5.0V)
22, 49, 52, 79	PV_{DD}	Positive gate drive supply voltage for RTZ output transistors (+5.0V)
23, 24, 46, 48, 53, 55, 77, 78	P_{GND}	Power ground path for RTZ output transistors
25, 47, 54, 76	PV_{SS}	Negative gate drive supply voltage for RTZ output transistors (-5.0V)
26, 45, 56, 75	V_{PF}	Linear regulator output gate drive voltage for the P-Channel output transistors. A low voltage 1.0 µF ceramic capacitor needs to be connected across every V_{PF} and V_{PP} pins. There are four capacitors required in total.
27	NC	No connection
28, 42, 59, 73	V_{NF}	Linear regulator output gate drive voltage for the N-Channel output transistors. A low voltage 1.0 µF ceramic capacitor needs to be connected across every V_{NF} to V_{NN} pins. There are four capacitors required in total.
29, 34, 35, 40, 41, 60, 61, 66, 67, 72	V_{NN}	Negative high voltage supply (-3.0V to -70V)
30	TX1	Transmit pulser outputs for channel 1
31, 32, 37, 38, 44, 57, 63, 64, 69, 70	V_{PP}	Positive high voltage supply (+3.0V to +70V)

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TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin	Symbol	Description
33	TX2	Transmit pulser outputs for channel 2
36	TX3	Transmit pulser outputs for channel 3
39	TX4	Transmit pulser outputs for channel 4
62	TX5	Transmit pulser outputs for channel 5
65	TX6	Transmit pulser outputs for channel 6
68	TX7	Transmit pulser outputs for channel 7
71	TX8	Transmit pulser outputs for channel 8
74	NC	No connection
80	V_{RP}	Positive supply for V_{NF} regulator (+5.0V)
81	V_{SUB}	Exposed center pad must be externally connected to the ground (GND, 0V) on PCB. (D_{GND}).

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3.0 DEVICE DESCRIPTION

3.1 Loading Data into the Four 16/32 bit Pattern Registers

A detailed circuit diagram of the pattern registers is shown in Figure 3-1. There are four programmable patterns that can be stored. One of four patterns can be selected via the two input logic decoder pins, A1 and A0. Data can be loaded on the selected pattern. Each pattern can be either 16- or 32-bits wide. The SIZE pin determines whether they are 16- or 32-bits wide. SIZE = H will set the pattern to be 32-bits wide while SIZE = L will set it to 16-bits wide. DIN1 is the input data for the register. When $\overline{CS1}$ is high, data will not be shifted in. Data is shifted in only when $\overline{CS1}$ is low.

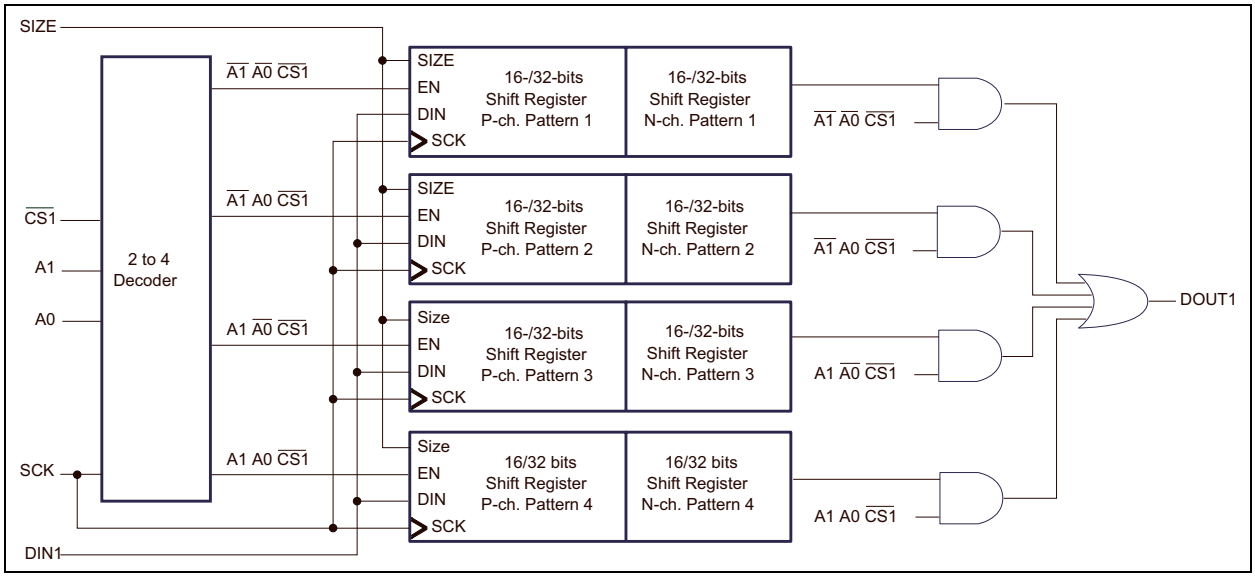

FIGURE 3-1: *Pattern Register Circuit Diagram.*

With SIZE = H, the circuit is effectively a 64-bit serial shift register. The data first enters into the P-Channel register and continues to be shifted though to the N-Channel register. Data is clocked in during the rising edge of the clock. There is no activity during the falling edge of the clock. The DIN1 data enters into the S64 of P-Channel register and exits the S1 of N-Channel register from DOUT1. The SPI writing operation of the waveform pattern registers are LSB first.

EXAMPLE 3-1:

For:	SIZE	=	High, 32-bits wide
	(SIZE	=	Low, 16-bits wide)
	A1	=	A0 = Low, Pattern 1 selected
	$\overline{CS1}$	=	Low, data can be shifted in
64-bit Serial Shift Register:			
	32 bits for the P-Channel		
	and		
	32 bits for the N-Channel		

Data is shifted in during the rising edge of the clock. S1 is the first bit shifted in, entering the P-Channel register. After 64 clock cycles, S1 will be located in the N-Channel register, as shown in Figure 3-2. It will also be clocked out to DOUT1.

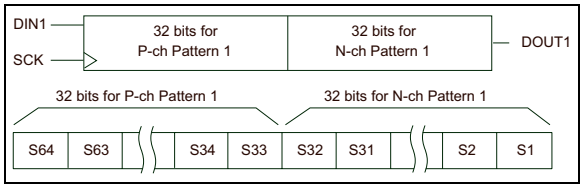

FIGURE 3-2: *Waveform Pattern Register.*

A 2-to-4 decoder is provided to select which of the four patterns is to be used for all of the outputs. Logic inputs A1 and A0 determine which patterns are selected, following Table 3-1. Once A1 and A0 are set, a rising edge on the trigger logic input pin will automatically load the selected pattern to all of the outputs.

TABLE 3-1: DECODER TRUTH TABLE

Logic Decoder Input		Pattern Selected
A1	A2	
0	0	1
0	1	2
1	0	3
1	1	4

3.2 Loading Data into the Delay Counters and the Divide-by-N Counter

Each output channel (TX) has its own programmable 10-bit delay counter. For 8 channels, 80 bits are needed. A 6-bit divide-by-N counter is also provided to program the desired TX frequency. To program all the individual delay counters and the divide-by-N counter, an 86-bit serial shift register is provided. It uses the same clock input that the pattern registers uses. DIN2 is the input data for this register. When $\overline{CS2}$ is high, data will not be shifted in. Data is shifted in only when $\overline{CS2}$ is low.

As shown in Figure 3-3, the data first enters into the 10-bit register for the TX8 delay counter and continues to be shifted through to the 6-bit register for the divide-by-N counter. Data is clocked in during the rising edge of the clock. There is no activity during the falling edge of the clock. The MSB bit in the 6-bit divide-by-N register is clocked out into DOUT2 for cascading multiple devices, if desired.

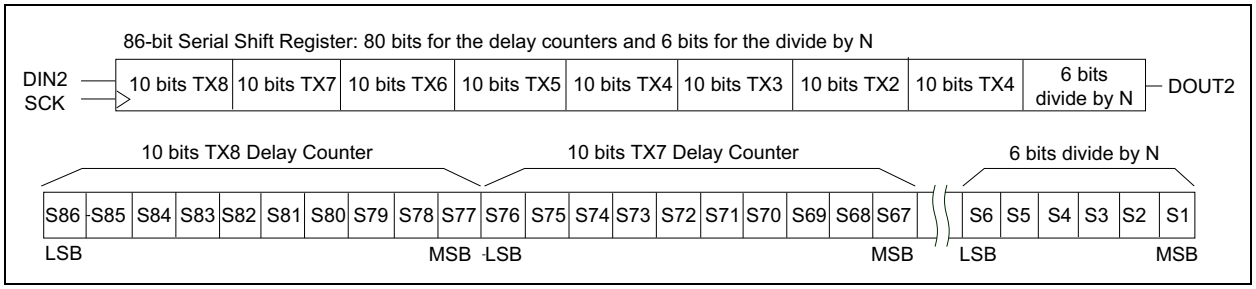

FIGURE 3-3: *Delay and Divide-by-N Registers.*

3.3 10-Bit Delay Counter

The TCK and $\overline{TCK}$ pins are the input clock for the 10-bit delay counter. The maximum capable clock frequency is up to 200 MHz. The counter counts upward.

TABLE 3-2: DELAY COUNTER

MSB									LSB	Delay Time
0	0	0	0	0	0	0	0	0	0	1023 TCK cycles
0	0	0	0	0	0	0	0	0	1	1022 TCK cycles
0	0	0	0	0	0	0	0	1	0	1021 TCK cycles
0	0	0	0	0	0	0	0	1	1	1020 TCK cycles
• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •
1	1	1	1	1	1	1	1	0	0	3 TCK cycles
1	1	1	1	1	1	1	1	0	1	2 TCK cycles
1	1	1	1	1	1	1	1	1	0	1 TCK cycle
1	1	1	1	1	1	1	1	1	1	No trigger

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3.4 6-Bit Divide-by-N Counter

The TCK and $\overline{TCK}$ pins are the input clock for the 6-bit divide-by-N counter. It generates the clock frequency for the 16-/32-bit serial shift register for the output P- and N-Channel patterns. Each clock cycle will set the TX output to be either at V_{PP}, V_{NN}, ground or high-impedance, depending on what was preprogrammed in their corresponding registers.

TABLE 3-3: 6-BIT DIVIDE-BY-N COUNTER REGISTER

MSB					LSB	Output Shift Register Clock Frequency
0	0	0	0	0	0	$f_{TCK} \div 64$
0	0	0	0	0	1	$f_{TCK} \div 63$
0	0	0	0	1	0	$f_{TCK} \div 62$
0	0	0	0	1	1	$f_{TCK} \div 61$
• • •	• • •	• • •	• • •	• • •	• • •	• • •
1	1	1	1	0	0	$f_{TCK} \div 4$
1	1	1	1	0	1	$f_{TCK} \div 3$
1	1	1	1	1	0	$f_{TCK} \div 2$
1	1	1	1	1	1	$f_{TCK} \div 1$

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NOTES:

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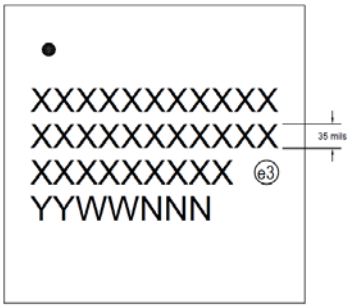
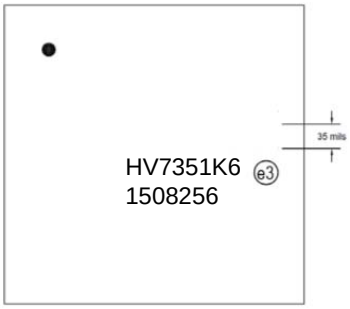
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

80-Lead VQFN (11x11x1.0 mm)



Example

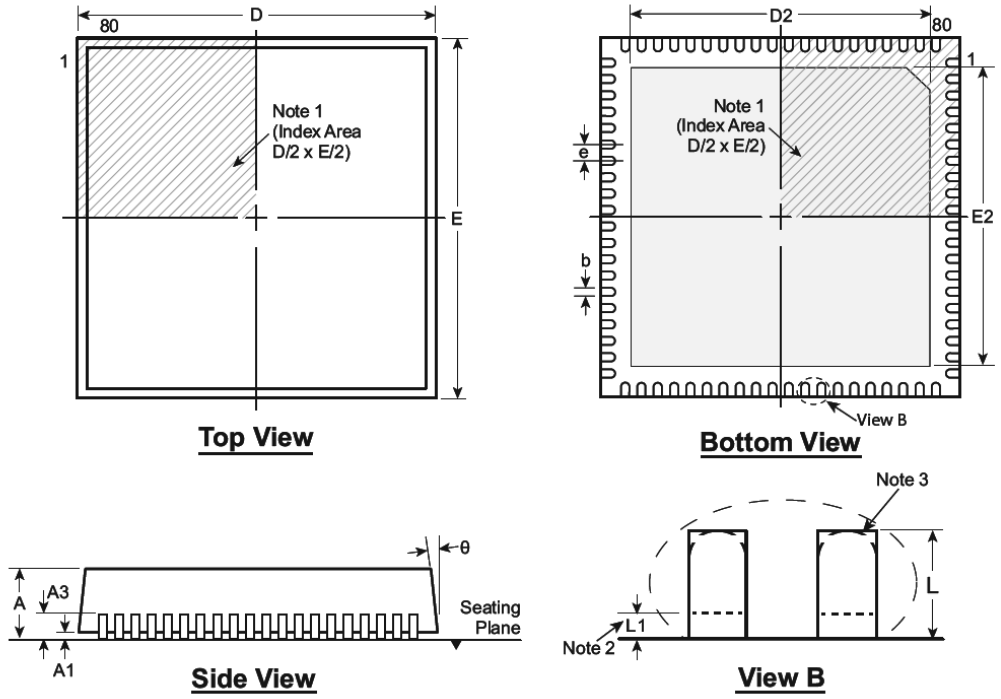


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

80-Lead QFN Package Outline (K6)

11.00x11.00mm body, 1.00mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	10.90	9.50	10.90	9.50	0.50 BSC	0.30	0.00	0°
	NOM	0.90	0.02		0.25	11.00	9.65	11.00	9.65		0.40	-	-
	MAX	1.00	0.05		0.30	11.10	9.75	11.10	9.75		0.50	0.15	14°

Drawings are not to scale.

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APPENDIX A: REVISION HISTORY

Revision A (June 2015)

- Original Release of this Document.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	-X
Device	Package	Environmental

Device:	HV7351:	Programmable High-Voltage, Ultrasound-Transmit Beamformer
Package:	K6 =	Very Thin Plastic Quad Flat Pack, No Lead Package – 11.00x11.00x1.0 mm Body, 0.50 mm Pitch, 80-Lead (VQFN)
Environmental:	G =	Lead (Pb)-free/ROHS-compliant package

Examples:

a) HV7351K6-G: Programmable High-Voltage Ultrasound-Transmit Beamformer, 80LD 11x11 mm VQFN package

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