NCP59800

1 A Low Noise, RF LDO Voltage Regulator

The NCP59800 is a family of 1 A low−dropout linear regulators (LDOs) offering high power−supply ripple rejection (PSRR) and ultra−low output noise. This series of LDOs uses an advanced BiCMOS process to achieve very good electrical performance. It is an ideal choice for noise sensitive Analog RF Front−Ends used in Telecom Equipment. The NCP59800 is available in the 3 mm x 3 mm DFN8 package.

Features

- Operating Input Voltage Range: 2.2 V to 6.0 V
- Output Voltage Range:
  - Fixed V_{OUT}: 0.8 to 5 V (0.1 V steps)
  - Adjustable V_{OUT}: 0.8 V to 5 V
- Quiescent Current typ. 60 μA
- Low Dropout: 200 mV typ. at 1 A, V_{OUT} = 2.5 V
- ±2.5% V_{OUT} Accuracy across Load/Line/Temperature
- Stable with Small 4.7 μF Ceramic Capacitors
- Very−Low Noise: Typically 15 μV_{RMS} from 100 Hz to 100 kHz
- Over−Current and Thermal Shutdown Protection
- Available in 3 x 3 mm DFN8 Package

Typical Applications

- Telecom Infrastructure
- Audio
- High−Speed I/F (PLL/VCO)

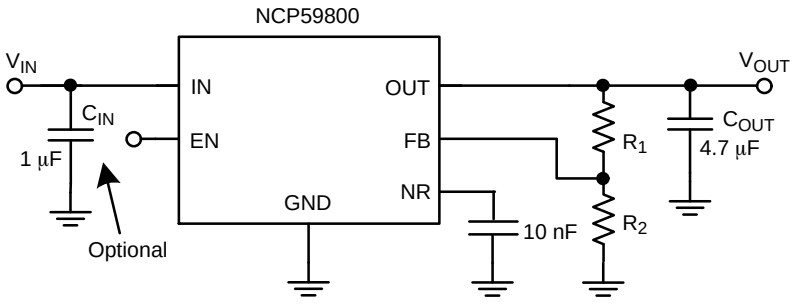

Figure 1. Typical Application Schematics Adjustable Voltage Option

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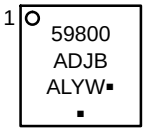
DFN8
3 x 3 mm
CASE 506DB

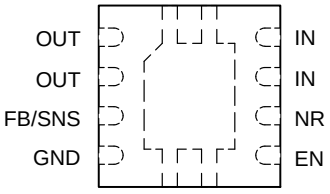
MARKING DIAGRAM



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

3 mm x 3 mm DFN8 0.65 P

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

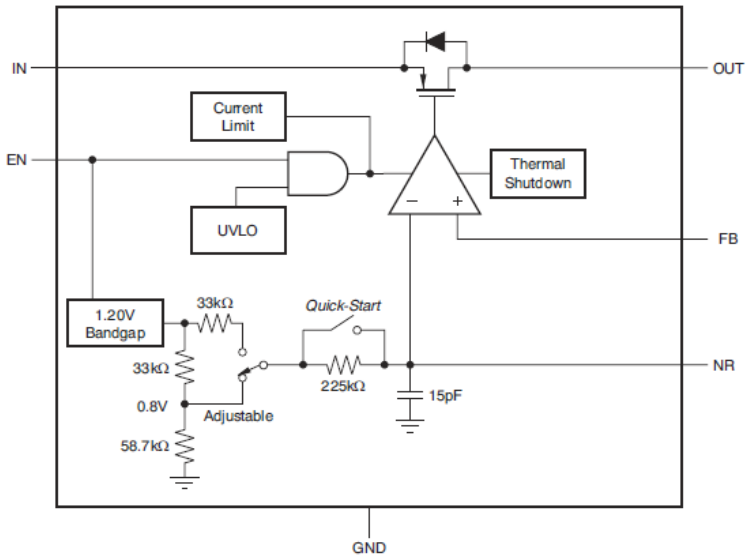


Figure 2. Internal Block Diagram − Adjustable Voltage Option

Table 1. PIN FUNCTION DESCRIPTION

Pin No. DFN8	Pin Name	Description
7,8	IN	Unregulated input supply.
4, EPAD	GND	Ground.
5	EN	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode.
6	NR	Connect an external capacitor between this pin and ground to reduce the output noise to very low levels. The capacitor slows down the V_{OUT} ramp as well (soft−start). Max recommended C_{NR} value is 0.47 μF
3 (Adjustable devices)	FB	This pin is the input to the control loop error amplifier and is used to set the output voltage of the device.
3 (Fixed Volt devices)	SNS	This pin is the input to the control loop error amplifier and is used to set the output voltage of the device. This pin is to be joined with OUT at load devices.
1,2	OUT	Regulator output. A 4.7 μF to 100 μF capacitor of any type is required for stability. $R_{ESR} \leq 1\ \Omega$

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	IN	6.5	V
Output, Sense Voltage	OUT, SNS	−0.3 to (V_{IN} + 0.3) ≤ 6.5	V
Enable Input	EN	−0.3 to 6.5	V
Other Voltages	FB, NR	−0.3 to 3.6	V
Output Current	I_{OUT}	Internally Limited	mA
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, DFN8 3 mm x 3 mm Thermal Resistance, Junction−to−Air (Note 3)	$R_{\theta JA}$	52	°C/W

3. The junction−to−ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC−standard, high−K board, as specified in JESD51−7, in an environment described in JESD51−2a.

Table 4. ELECTRICAL CHARACTERISTICS Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = ($V_{OUT(NOM)}$ + 0.5 V) or 2.2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = 2.2 V, C_{OUT} = 4.7 μF, and C_{NR} = 0.01 μF, unless otherwise noted. NCP59800 Adjustable Option is tested at V_{OUT} = 0.8 V and V_{OUT} = 5.0 V. Typical values are at T_J = +25°C.

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Input Voltage Range			V_{IN}	(V_{OUT}+V_{DO}) ≥ 2.2		6.0	V
Internal Reference			V_{NR}		0.8		V
Output Voltage	Fixed Voltage Options		V_{OUT}	0.8		5.0	V
	Adjustable Option			0.8		5.0	V
Output Voltage Accuracy (Note 4)	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 6.0 V, V_{IN} ≥ 2.2 V 1 mA ≤ I_{OUT} ≤ 1 A		V_{OUT}	−2.5	±0.3	+2.5	%
Line Regulation	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 6.0 V, V_{IN} ≥ 2.2 V I_{OUT} = 1 mA		$\Delta V_{OUT}/\Delta V_{IN}$		150		μV/V
Load Regulation	1 mA ≤ I_{OUT} ≤ 1 A		$\Delta V_{OUT}/\Delta I_{OUT}$		2.0		μV/mA
Dropout Voltage (Note 5)	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 6.0 V, V_{IN} ≥ 2.2 V I_{OUT} = 500 mA, V_{FB} = GND or V_{SNS} = GND		V_{DO}			250	mV
	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 6.0 V, V_{IN} ≥ 2.5 V I_{OUT} = 750 mA, V_{FB} = GND or V_{SNS} = GND					350	mV
	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 6.0 V, V_{IN} ≥ 2.5 V I_{OUT} = 1 A, V_{FB} = GND or V_{SNS} = GND					500	mV
Output Current Limit	V_{OUT} = 0.85 $V_{OUT(NOM)}$, V_{IN} ≥ 3.3 V		I_{CL}	1.1	1.6	2.5	A
Ground Pin Current	I_{OUT} = 0.1 mA		I_{GND}		60	100	μA
	I_{OUT} = 1 A					450	μA
Shutdown Current (I_{GND})	V_{EN} ≤ 0.4 V, V_{IN} ≥ 2.2 V, R_L = 1 kΩ, 0°C ≤ T_J ≤ 85°C		I_{SHDN}		0.2	2.0	μA
Feedback Pin Current	V_{IN} = 6.0 V, V_{FB} = 0.8 V (Adjustable Option)				0.02	1.0	μA
Sense Pin Current	V_{IN} = 6.0 V, V_{SNS} = $V_{OUT(NOM)}$ (Fixed Option)				3.0		μA
Power Supply Rejection Ratio	I_{OUT} = 750 mA, V_{OUT} = 3.3 V, V_{IN} = 4.3 V	f = 100 Hz f = 1 kHz f = 1 MHz	PSRR		77 63 27		dB
Output Noise Voltage	BW = 100 Hz−100 kHz, I_{OUT} = 100 mA, C_{NR} = 100 nF, V_{IN} = 4.3 V, V_{OUT} = 3.3 V		V_N		15 x V_{OUT}		μV_{RMS}
Enable Input Current	V_{IN} = V_{EN} = 6.0 V		I_{EN}		0.02	1.0	μA
Soft−Start Charging Current	V_{NR} = 0.5 V		I_{SS}		7.2		μA
EN Pin Threshold Voltage	EN Input Voltage “H”		V_{ENH}	1.2			V
	EN Input Voltage “L”		V_{ENL}			0.4	
Start−Up Time	$V_{OUT(NOM)}$ = 3.3 V V_{OUT} = 0% to 90% $V_{OUT(NOM)}$ R_L = 3.3kΩ, C_{OUT}=4.7 μF	C_{NR} = 10 nF	t_{STR}		1.0		ms
		C_{NR} = 100 nF			10		ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. As for NCP59800 (adjustable); it does not include external resistor tolerances and it is not tested at this condition: V_{OUT} = 0.8 V, 4.5 V ≤ V_{IN} ≤ 6.0 V, and 750 mA ≤ I_{OUT} ≤ 1 A because of power dissipation higher than maximum rating of the package.
5. V_{DO} is not measured for fixed output voltage devices with V_{OUT} < 1.7 V because minimum V_{IN} = 2.2 V.

Table 4. ELECTRICAL CHARACTERISTICS Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = ($V_{OUT(NOM)}$ + 0.5 V) or 2.2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = 2.2 V, C_{OUT} = 4.7 μF, and C_{NR} = 0.01 μF, unless otherwise noted. NCP59800 Adjustable Option is tested at V_{OUT} = 0.8 V and V_{OUT} = 5.0 V. Typical values are at T_J = +25°C.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Undervoltage Lockout	V_{IN} rising, R_L = 1 kΩ	UVLO	1.86	2.0	2.1	V
UVLO Hysteresis	V_{IN} falling, R_L = 1 kΩ			75		mV
Thermal Shutdown	Shutdown, temperature increasing	T_{SD_TEMP}		160		°C
Thermal Shutdown Recovery	Reset, temperature decreasing	T_{SD_HYST}		140		
T_J Operating Range			−40		+125	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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5. V_{DO} is not measured for fixed output voltage devices with V_{OUT} < 1.7 V because minimum V_{IN} = 2.2 V.

APPLICATIONS INFORMATION

General Information

The NCP59800 regulator is equipped with Noise Reduction pin (NR) for noise sensitive applications. A noise reduction capacitor (C_{NR}) at the NR pin bypasses noise generated by the bandgap reference. This family of regulators offers sub−bandgap output voltages, current limit, and thermal protection, and is fully specified from –40°C to +125°C. assuming resistors with zero error. For the actual design, pay attention to any resistor error factors. Figure 3 gives the connections for the adjustable output version (NCP59800BMNADJTBG).

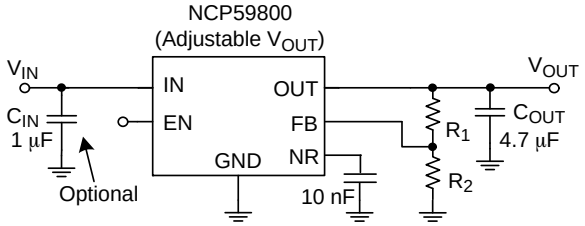


Figure 3. Typical Application Schematics

Output Voltage Setting

For the adjustable version (NCP59800BMNADJTBG), the voltage on the FB pin sets the output voltage and is determined by the values of R1 and R2. The values of R1 and R2 can be calculated for any voltage using the following formula:

$$V_{OUT} = 0.8\ V \left(1 + \frac{R_1}{R_2}\right)$$

Capacitors Selection

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1 μF to 1.0 μF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. The NCP59800 is designed to be stable with standard ceramic output capacitors of capacitance values 4.7 μF up to 100 μF. This device is evaluated using a 4.7 μF/10 V, 10% tolerance, X5R type Ceramic Capacitors of 0805 size.

X5R− and X7R−type capacitors are highly recommended because they have minimal variation in value and ESR over temperature. Maximum ESR should be < 1.0 Ω.

Startup Response

The C_{NR} serves not only for noise reduction. Slow ramping of Voltage Reference (adjustable Soft−Start) is reducing the Inrush Current as well.

Recommended 1% Feedback Resistor Values for Frequently Used Nominal Output Voltages

V_{OUT}	R_1	R_2
0.8 V	0 Ω (Short)	10.0 kΩ
1.0 V	2.49 kΩ	10.0 kΩ
1.2 V	4.99 kΩ	10.0 kΩ
1.5 V	8.87 kΩ	10.0 kΩ
1.8 V	12.5 kΩ	10.0 kΩ
2.5 V	21.0 kΩ	10.0 kΩ
3.3 V	30.9 kΩ	10.0 kΩ
5.0 V	52.3 kΩ	10.0 kΩ

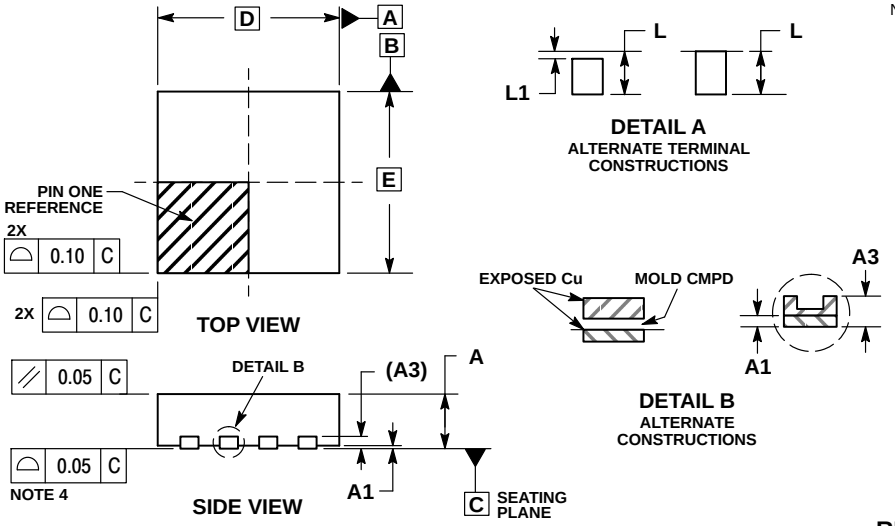
Table 5. ORDERING INFORMATION

Device	Output Voltage	Marking	Package	Shipping†
NCP59800BMNADJTBG	ADJ	59800 ADJB	DFN8 3x3 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*To order other package and voltage variants, please contact your ON sales representative.

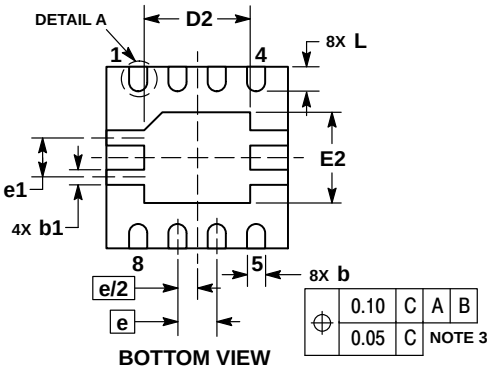
PACKAGE DIMENSIONS

DFN8, 3x3, 0.65P
CASE 506DB
ISSUE O

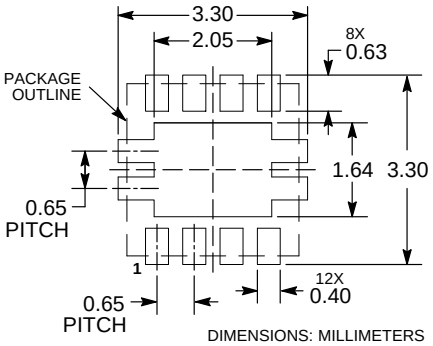


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
b1	0.20	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.40	1.60
e	0.65 BSC	
e1	0.65 REF	
L	0.30	0.50
L1	0.00	0.15



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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