FDMC010N08LC

N-Channel Shielded Gate POWERTRENCH® MOSFET

80 V, 50 A, 10.9 mΩ

ON Semiconductor®

www.onsemi.com

General Description

This N-Channel MV MOSFET is produced using ON Semiconductor's advanced PowerTrench process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

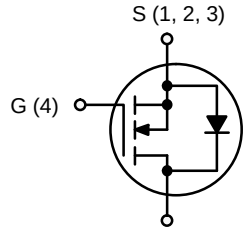
Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 10.9 mΩ at V_{GS} = 10 V, I_D = 16 A
- Max $R_{DS(on)}$ = 18.4 mΩ at V_{GS} = 4.5 V, I_D = 13 A
- 50% Lower Q_{rr} than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

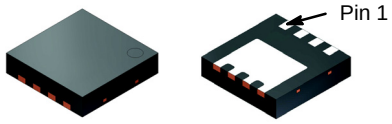
Applications

- Primary DC−DC MOSFET
- Synchronous Rectifier in DC−DC and AC−DC
- Motor Drive
- Solar

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
80 V	10.9 mΩ @ 10 V	50 A
	18.4 mΩ @ 4.5 V	



N-CHANNEL MOSFET



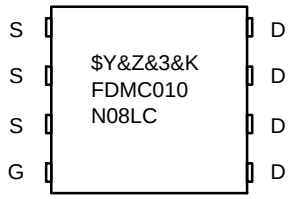
Power 33
(PQFN8)
CASE 483AX

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	80	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current: Continuous, T_C = 25°C (Note 5) Continuous, T_C = 100°C (Note 5) Continuous, T_A = 25°C (Note 1a) Pulsed (Note 4)	 50 32 11 200	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	96	mJ
P_D	Power Dissipation: T_C = 25°C T_A = 25°C (Note 1a)	 52 2.3	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDMC010N08LC	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	80			V
ΔBV_{DSS} /ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		76		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 90 μA	1.0	1.3	3.0	V
$\Delta V_{GS(th)}$ /ΔT_J	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 90 μA, referenced to 25°C		−5		mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 16 A		8.9	10.9	mΩ
		V_{GS} = 4.5 V, I_D = 13 A		12.5	18.4	
		V_{GS} = 10 V, I_D = 16 A, T_J = 125°C		15.0	17.6	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 16 A		55		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz		1525	2135	pF
C_{oss}	Output Capacitance			369	515	pF
C_{rss}	Reverse Transfer Capacitance			20	30	pF
R_g	Gate Resistance		0.1	0.3	0.7	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 40 V, I_D = 16 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		8	16	ns
t_r	Rise Time			3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			27	44	ns
t_f	Fall Time			5	10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 40 V, I_D = 16 A		22	31	nC
		V_{GS} = 0 V to 4.5 V, V_{DD} = 40 V, I_D = 16 A		11	15	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 40 V, I_D = 16 A		3		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 40 V, I_D = 16 A		3		nC
Q_{oss}	Output Charge	V_{DD} = 40 V, V_{GS} = 0 V		21		nC
Q_{sync}	Total Gate Charge Sync	V_{DS} = 0 V, I_D = 16 A		19.5		nC

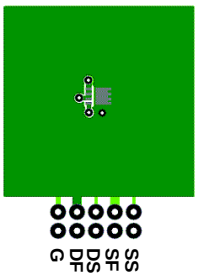
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2)		0.7	1.2	V
		V_{GS} = 0 V, I_S = 16 A (Note 2)		0.8	1.3	
t_{rr}	Reverse Recovery Time	I_F = 16 A, di/dt = 300 A/μs		15	27	ns
Q_{rr}	Reverse Recovery Charge			18	33	nC
t_{rr}	Reverse Recovery Time	I_F = 16 A, di/dt = 1000 A/μs		12	21	ns
Q_{rr}	Reverse Recovery Charge			38	61	nC

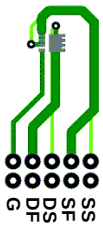
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta CA}$ is determined by the user's board design.

NOTES:



a) 53°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 96 mJ is based on starting T_J = 25°C; N-ch: L = 3 mH, I_{AS} = 8 A, V_{DD} = 80 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 24 A.
4. Pulsed Id please refer to Figure 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

ORDERING INFORMATION

Device	Marking	Package	Reel Size	Tape Width	Quantity
FDMC010N08LC	FDMC010N08LC	Power 33 (PQFN8) (Pb-Free / Halogen Free)	13″	12 mm	3000 Units

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

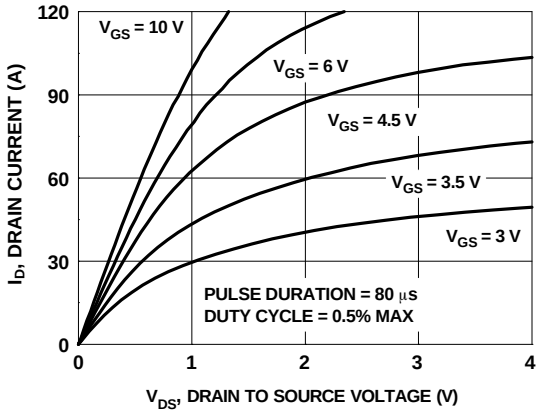


Figure 1. On Region Characteristics

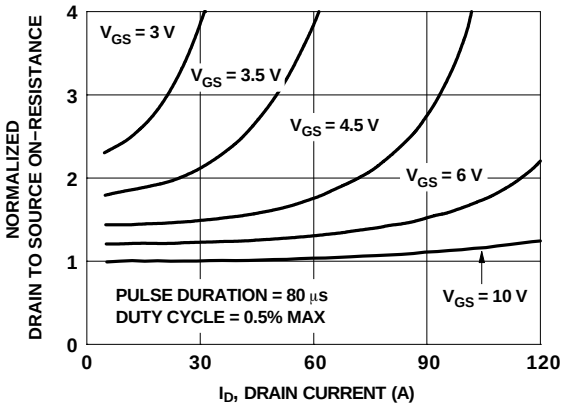


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

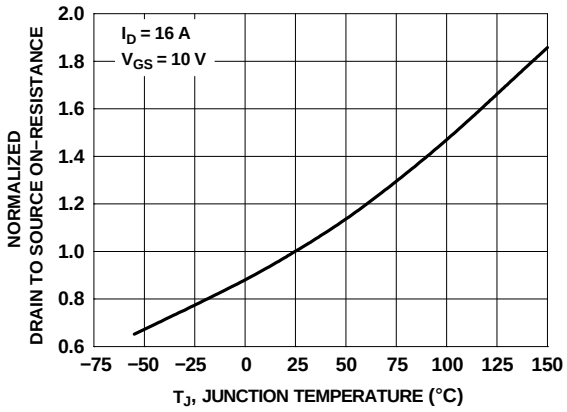


Figure 3. Normalized On-Resistance vs. Junction Temperature

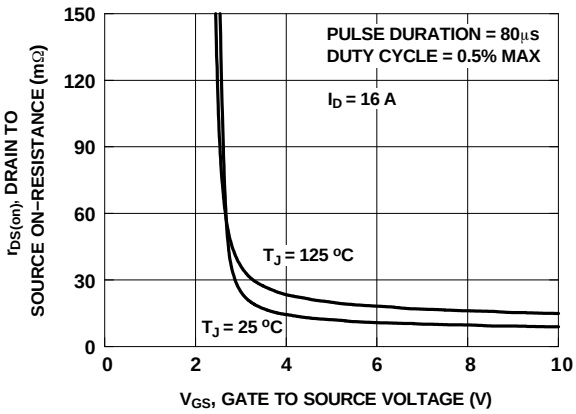


Figure 4. On-Resistance vs. Gate to Source Voltage

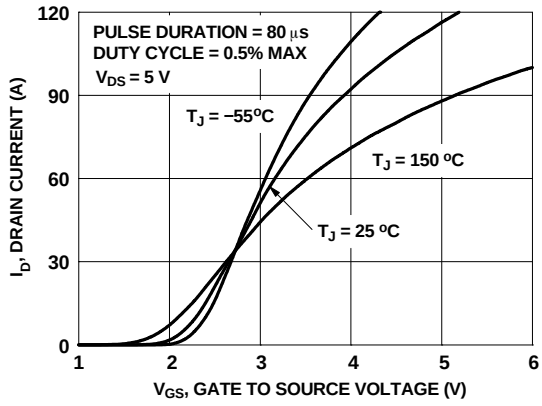


Figure 5. Transfer Characteristics

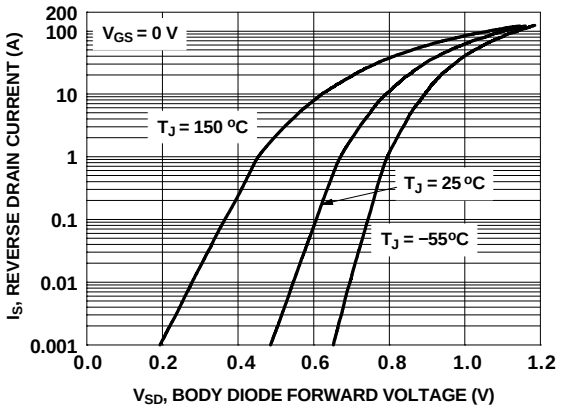


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

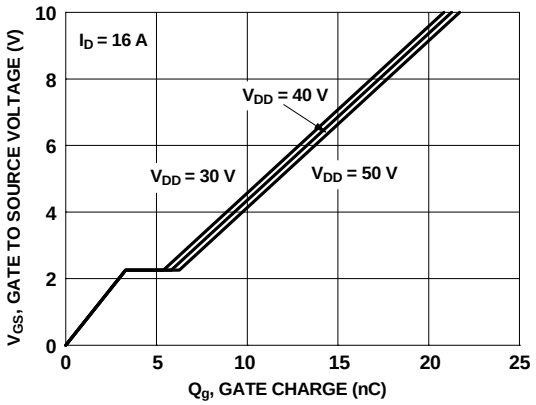


Figure 7. Gate Charge Characteristics

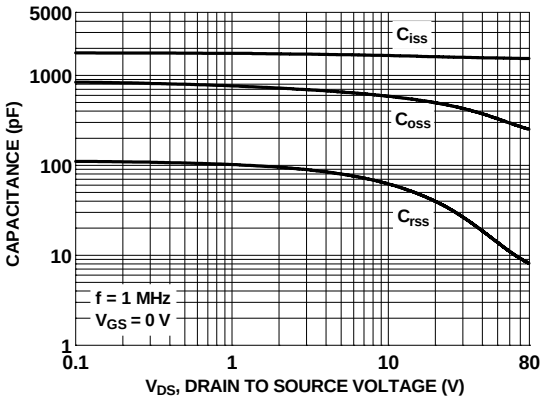


Figure 8. Capacitance vs. Drain to Source Voltage

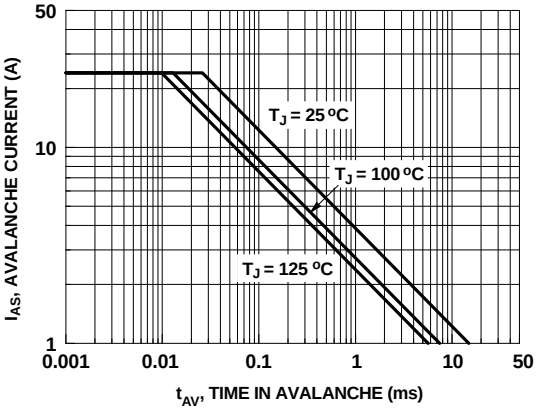


Figure 9. Unclamped Inductive Switching Capability

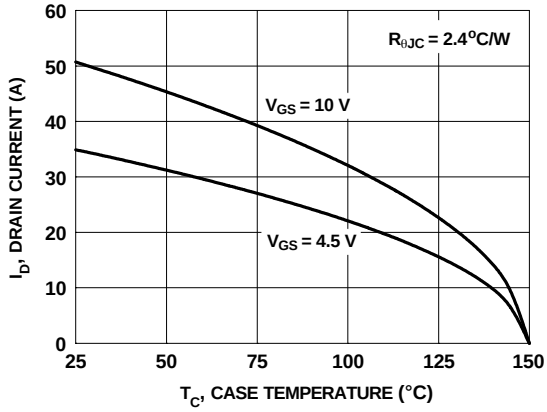


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

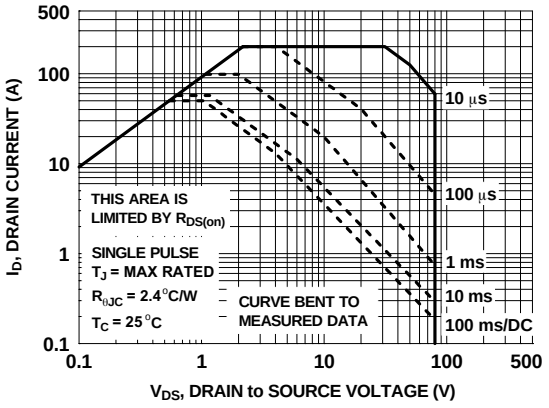


Figure 11. Forward Bias Safe Operating Area

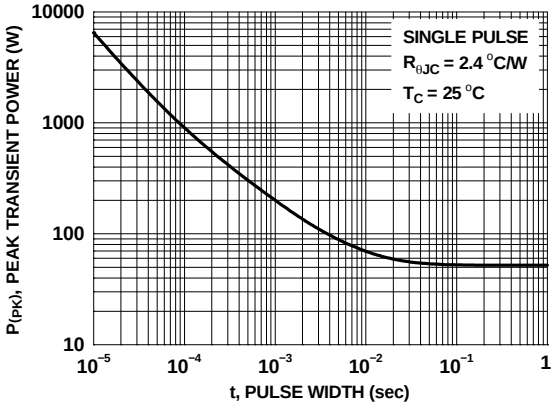


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

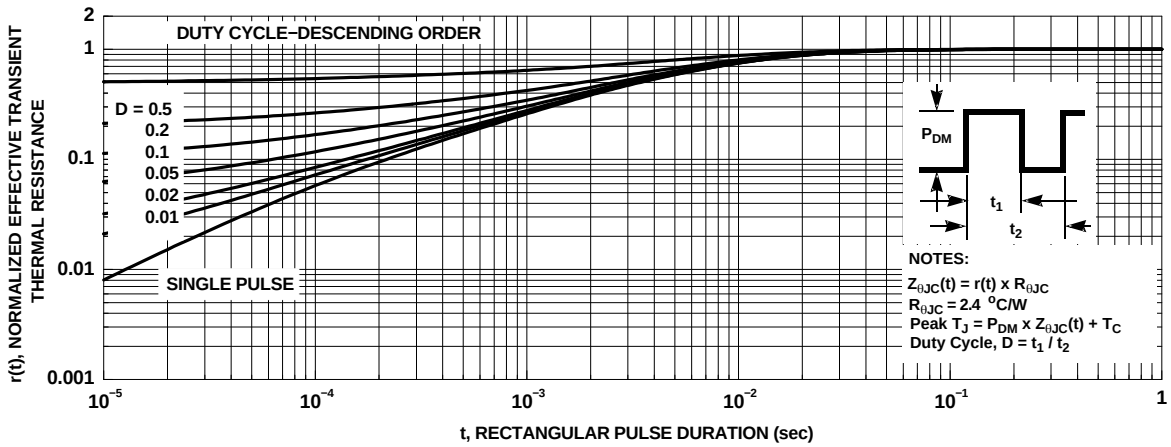
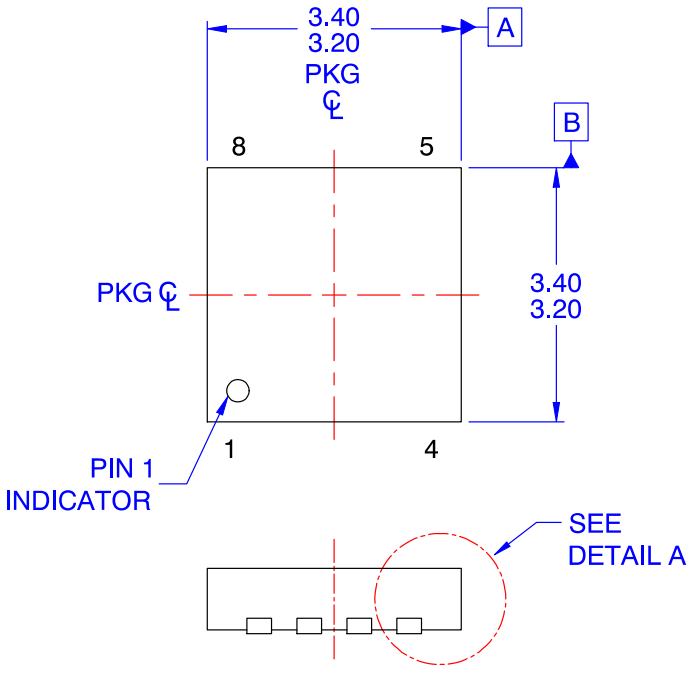
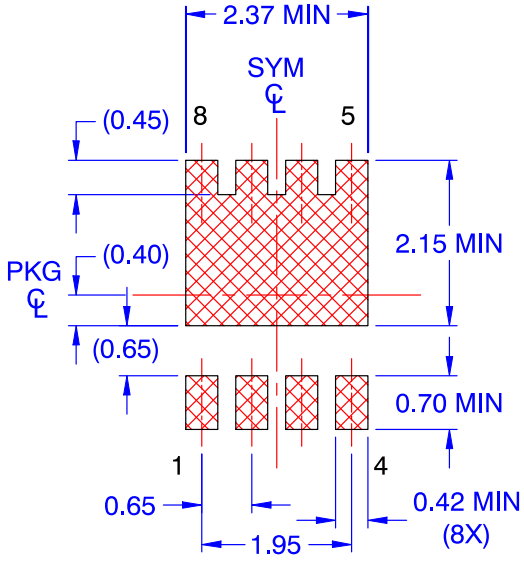


Figure 13. Junction-to-Case Transient Thermal Response Curve

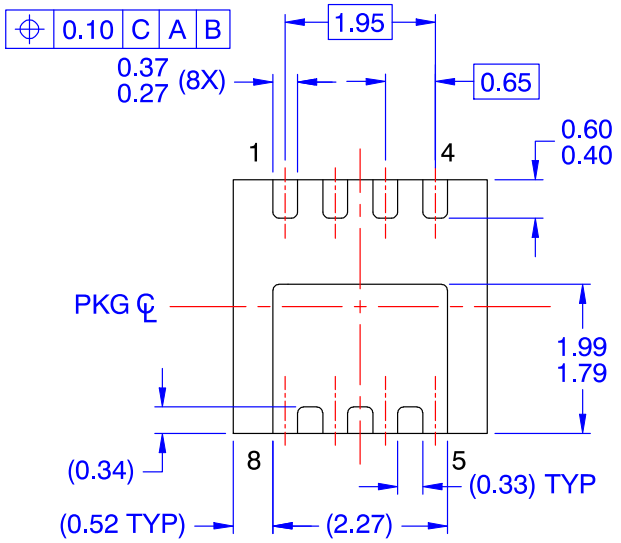
PACKAGE DIMENSIONS

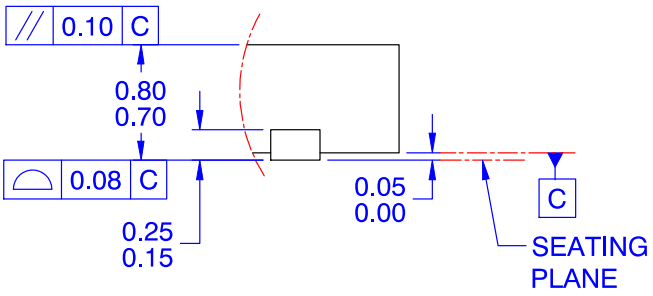
PQFN8 3.3X3.3, 0.65P
CASE 483AX
ISSUE O





LAND PATTERN
RECOMMENDATION





DETAIL A
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
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