

N-Channel Power MOSFET

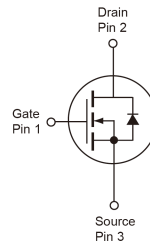
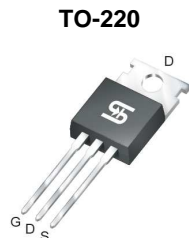
100V, 160A, 5.5mΩ

FEATURES

- Advanced Trench Technology
- Low $R_{DS(ON)}$ 5.5mΩ (Max.)
- Low gate charge typical @ 154nC (Typ.)
- Low Crss typical @ 260pF (Typ.)

KEY PERFORMANCE PARAMETERS

PARAMETER	VALUE	UNIT
V_{DS}	100	V
$R_{DS(on)}$ (max)	5.5	mΩ
Q_g	154	nC



Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^(Note 1)	I_D	$T_C = 25^\circ\text{C}$	160
		$T_C = 70^\circ\text{C}$	127
		$T_A = 25^\circ\text{C}$	14.2
		$T_A = 70^\circ\text{C}$	11.4
Pulsed Drain Current ^(Note 2)	I_{DM}	620	A
Total Power Dissipation	P_{DTOT}	$T_C = 25^\circ\text{C}$	300
		$T_C = 70^\circ\text{C}$	210
		$T_A = 25^\circ\text{C}$	2.4
		$T_A = 70^\circ\text{C}$	1.68
Single Pulsed Avalanche Energy ^(Note 3)	E_{AS}, E_{AR}	400	mJ
Single Pulsed Avalanche Current ^(Note 3)	I_{AS}, I_{AR}	40	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +175	$^\circ\text{C}$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	0.5	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62.5	°C/W

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	100	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	2	3	4	V
Zero Gate Voltage Drain Current	$V_{DS} = 80V, V_{GS} = 0V$	I_{DSS}	--	--	1	μA
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 30A$	$R_{DS(on)}$	--	4.5	5.5	m Ω
Dynamic (Note 5)						
Total Gate Charge	$V_{DS} = 30V, I_D = 30A, V_{GS} = 10V$	Q_g	--	154	--	nC
Gate-Source Charge		Q_{gs}	--	35	--	
Gate-Drain Charge		Q_{gd}	--	40	--	
Input Capacitance	$V_{DS} = 30V, V_{GS} = 0V, F = 1.0\text{MHz}$	C_{iss}	--	9840	--	pF
Output Capacitance		C_{oss}	--	750	--	
Reverse Transfer Capacitance		C_{rss}	--	260	--	
Switching (Note 6)						
Turn-On Delay Time	$V_{GS} = 10V, V_{DS} = 30V, R_G = 3.3\Omega$	$t_{d(on)}$	--	25	--	ns
Turn-On Rise Time		t_r	--	40	--	
Turn-Off Delay Time		$t_{d(off)}$	--	85	--	
Turn-Off Fall Time		t_f	--	45	--	
Source-Drain Diode (Note 4)						
Forward Voltage	$V_{GS}=0V, I_S=30A$	V_{SD}	-	0.8	1.3	V
Reverse Recovery Time	$I_S = 30A, T_J = 25^\circ\text{C}$ $di/dt = 100A/\mu s$	t_{rr}		120		nS
Reverse Recovery Charge		Q_{rr}		160		nC

Notes:

1. Current limited by package.
2. Pulse width limited by the maximum junction temperature.
3. $L = 0.5\text{mH}, I_{AS} = 40A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
4. Pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$.
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM160N10CZ C0G	TO-220	50pcs / Tube

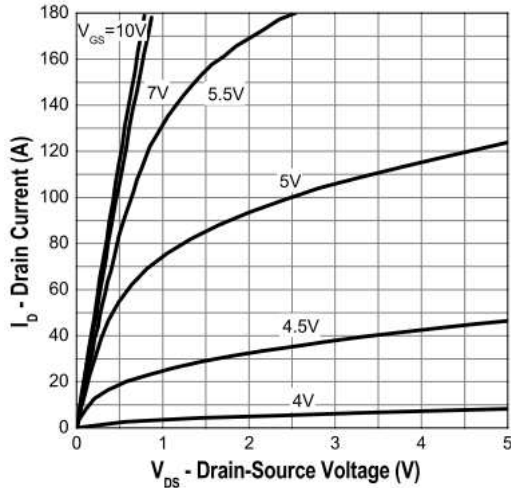
Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

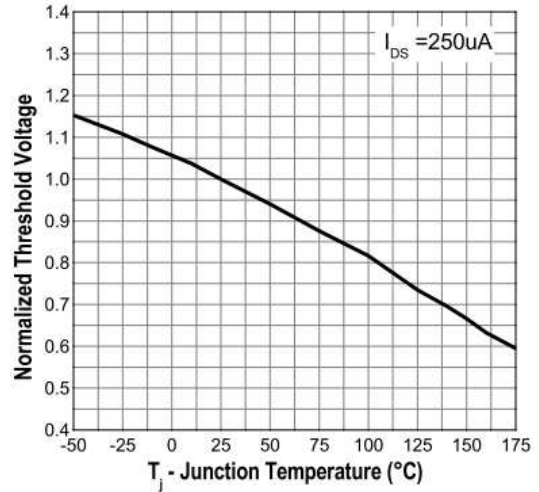
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

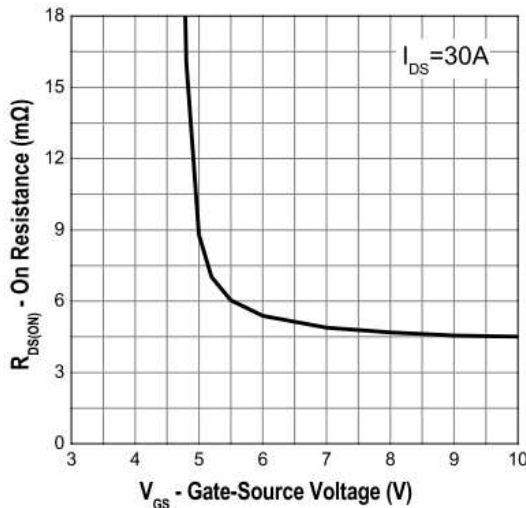
Output Characteristics



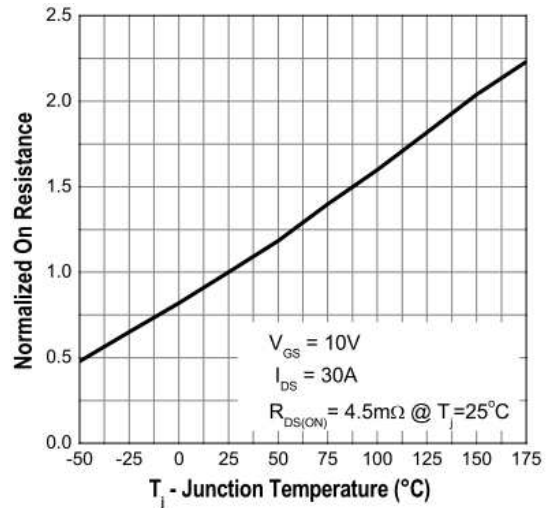
Gate Threshold Voltage



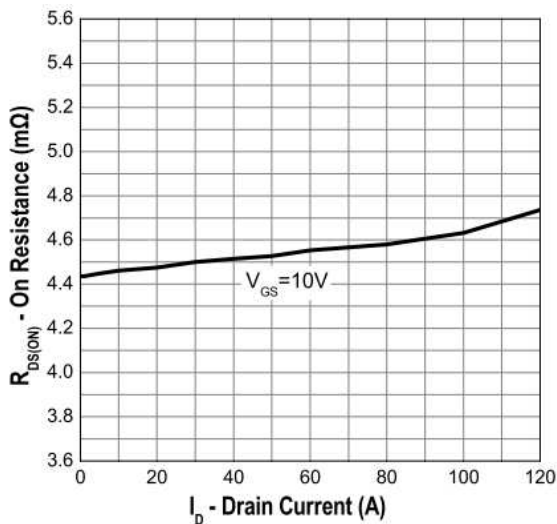
Gate Source On Resistance



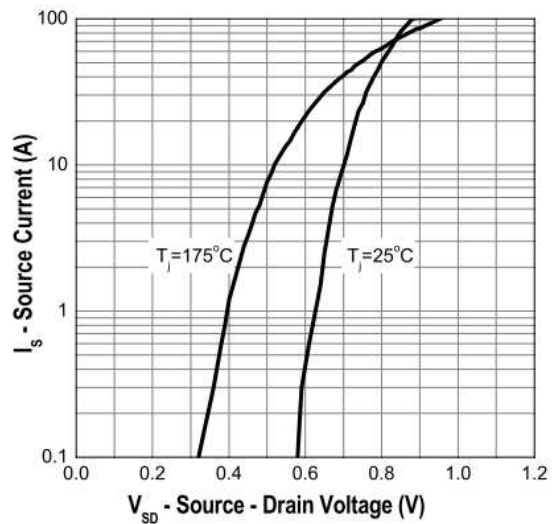
Drain-Source On Resistance



Drain-Source On-Resistance



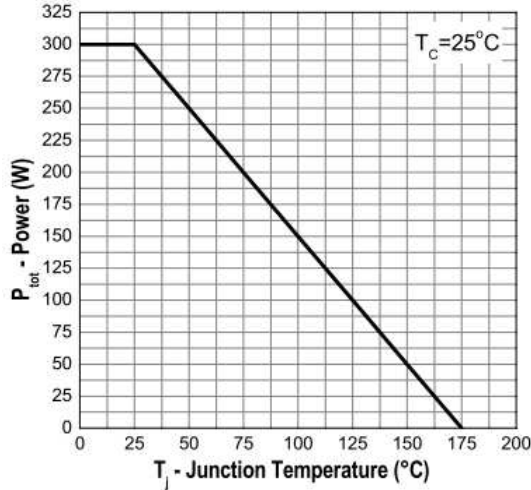
Source-Drain Diode Forward Voltage



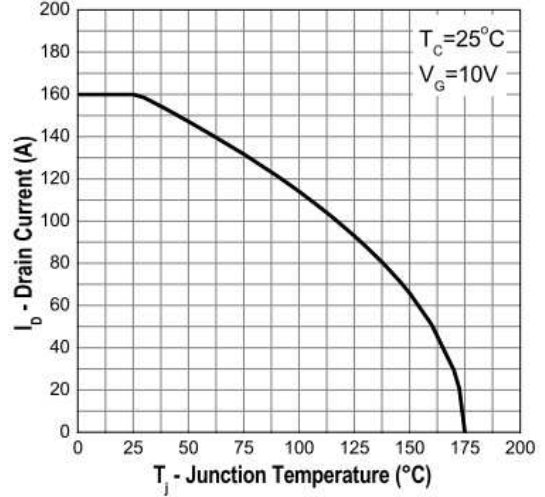
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

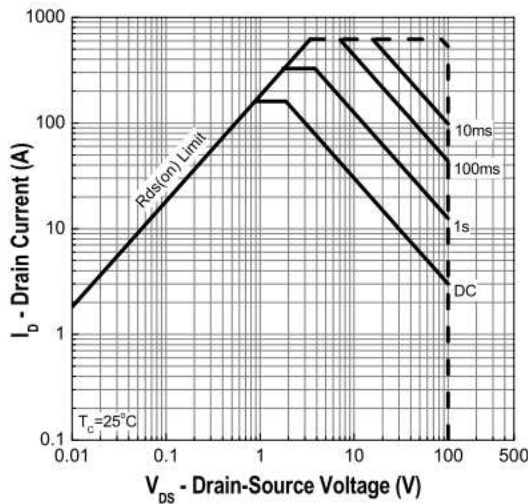
Power Derating



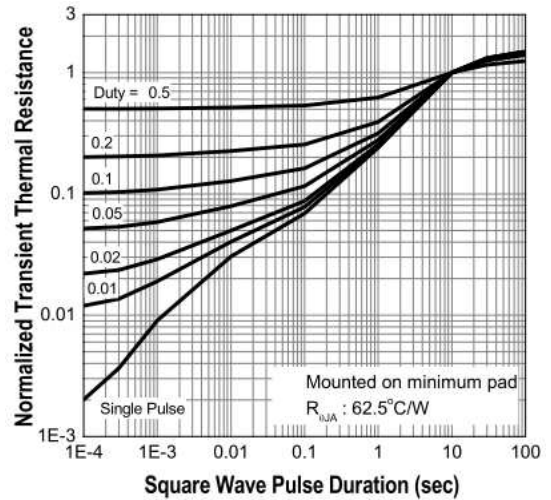
Drain Current vs. Junction Temperature



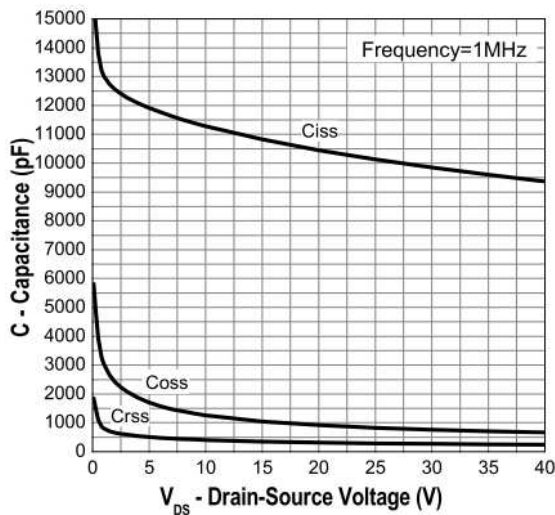
Safe Operation Area



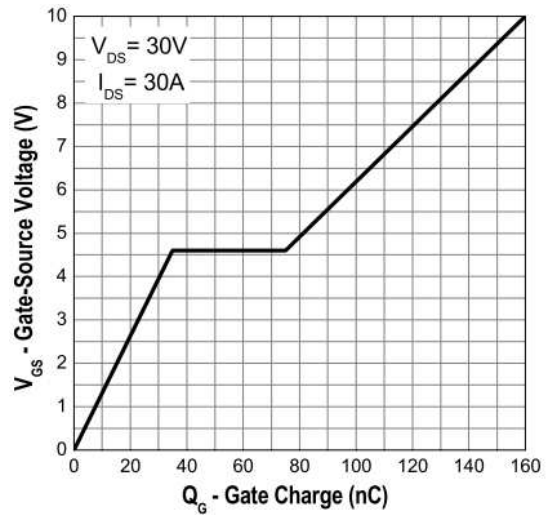
Transient Thermal Impedance



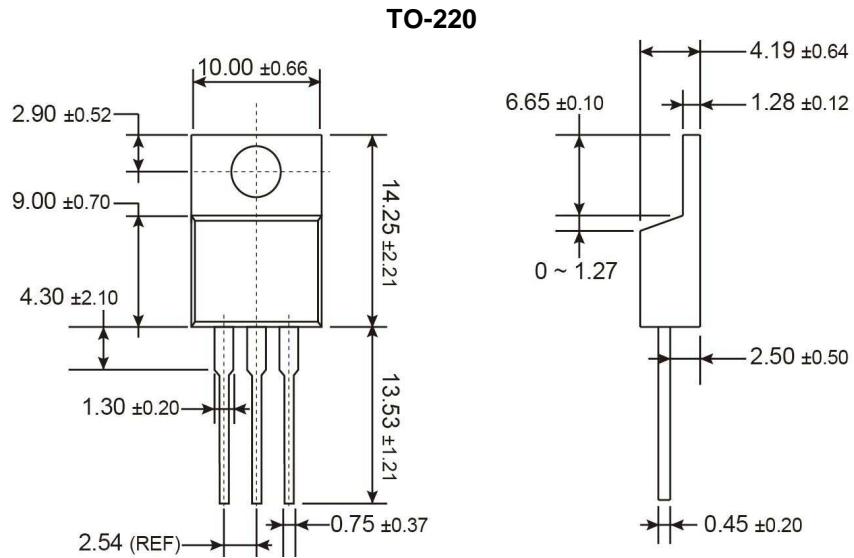
Capacitance



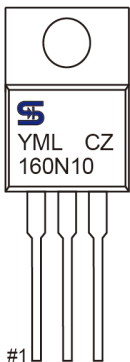
Gate Charge



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



Marking Diagram



- Y** = Year Code
- M** = Month Code for Halogen Free Product
 - O** =Jan **P** =Feb **Q** =Mar **R** =Apr
 - S** =May **T** =Jun **U** =Jul **V** =Aug
 - W** =Sep **X** =Oct **Y** =Nov **Z** =Dec
- L** = Lot Code (1~9, A~Z)

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