PIC18(L)F27/47/57K42 Family Silicon Errata and Data Sheet Clarification

The PIC18(L)F27/47/57K42 family devices that you have received conform functionally to the current Device Data Sheet (DS40001919**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18(L)F27/47/57K42 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections start on page 4, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, contact your local Microchip sales office for assistance.

The DEVREV/REVID values for the various PIC18(L)F27/47/57K42 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID<13:0>(1), (2)	Revision ID for Silicon Revision
		A1
PIC18F27K42	6C40h	A001
PIC18F47K42	6BE0h	A001
PIC18F57K42	6B80h	A001
PIC18LF27K42	6D80h	A001
PIC18LF47K42	6D20h	A001
PIC18LF57K42	6CC0h	A001

Note 1: The Revision ID is located in addresses 3FFFFCh-3FFFFDh and Device ID is located in addresses 3FFFFEh-3FFFFFh.

2: Refer to the *"PIC18(L)F27/47/57K42 Memory Programming Specification"* (DS40001886) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item No.	Issue Summary	Affected Revisions(1)
				A1
Electrical Specifications	SMBus 3.0	1.1	SMBus 3.0 logic levels.	X
	Min V_{DD} Specification for LF Devices	1.2	V_{DDMIN} for LF devices is 2.0V.	X
DMA	DMA Reads from Data EEPROM	2.1	DMA reads from Data EEPROM does not operate.	X
ADC	ADC Conversion in FOSC Mode	3.1	ADC does not complete conversion successfully in FOSC mode with non-zero clock divider.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1**).

1. Module: Electrical Specifications

1.1 SMBus 3.0

The SMBus 3.0 V_{IL} specification (Parameter D305) is temperature and V_{DD} dependent. Refer to the table below.

Temperature	V_{DD}	D305 SMBus 3.0 V_{IL} Specification
-40°C	1.8V	0.6V
-40°C	5.5V	0.8V
25°C	1.8V	0.6V
25°C	5.5V	0.8V
85°C	1.8V	0.6V
85°C	5.5V	0.7V
125°C	1.8V	0.5V
125°C	5.5V	0.7V

Work around

None.

Affected Silicon Revisions

A1							
X							

1.2 Min VDD Specification for LF Devices

V_{DDMIN} for LF devices (Parameter D002) is 2.0V.

Work around

None.

Affected Silicon Revisions

A1							
X							

2. Module: DMA

2.1 DMA Reads from Data EEPROM

The DMA modules do not operate when configured to access the Data EEPROM (i.e., SMR[1:0] = 1x). The destination gets written to `0x00`.

Work around

None. NVMCON reads work as described.

Affected Silicon Revisions

A1							
X							

3. Module: ADC

3.1 ADC Conversion in FOSC Mode

The ADCON0.GO bit remains set and the conversion does not complete successfully when configured to operate in FOSC mode (ADCON0.CS=0) with non-zero clock divider (ADCLK register).

Work around

a) Use F_{OSC} as the clock source (ADCON0.CS=0) and set the clock divider (ADCLK register) to zero. Ensure that the F_{OSC} frequency does not violate timing requirements for the ADC.

b) Use ADCRC as the clock source (ADCON0.CS=1).

Affected Silicon Revisions

A1							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001919**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Specifications

1.1 Power-Down Current

Table 44-5 contains incorrect ADC power-down current. The corrected table is as follows:

TABLE 44-5 POWER-DOWN CURRENT (I_{PD})(1,2)

PIC18LF27/47/57K42				**Standard Operating Conditions (unless otherwise stated)**					
PIC18F27/47/57K42				**Standard Operating Conditions (unless otherwise stated)** VREGPM = 1					
Param. No.	**Symbol**	**Device Characteristics**	**Min.**	**Typ.†**	**Max. +85°C**	**Max. +125°C**	**Units**	**Conditions**	
								VDD	**Note**
D200	IPD	IPD Base	—	0.07	2	10.5	µA	3.0V	
D200 D200A	IPD	IPD Base	—	0.4	4	12	µA	3.0V	
			—	20	38	42	µA	3.0V	VREGPM = 0
D201	IPD_WDT	Low-Frequency Internal Oscillator/ WDT	—	0.9	3.2	11.2	µA	3.0V	
D201	IPD_WDT	Low-Frequency Internal Oscillator/ WDT	—	1.1	3.2	13	µA	3.0V	
D202	IPD_SOSC	Secondary Oscillator (SOSC)	—	0.75	6	14	µA	3.0V	LP mode
D202	IPD_SOSC	Secondary Oscillator (SOSC)	—	1.0	7	15	µA	3.0V	LP mode
D203	IPD_FVR	FVR	—	45	74	75	µA	3.0V	FVRCON = 0x81 or 0x84
D203	IPD_FVR	FVR	—	40	70	76	µA	3.0V	FVRCON = 0x81 or 0x84
D204	IPD_BOR	Brown-out Reset (BOR)	—	9.4	14	18	µA	3.0V	
D204	IPD_BOR	Brown-out Reset (BOR)	—	9.4	15	18	µA	3.0V	
D205	IPD_LPBOR	Low-Power Brown-out Reset (LPBOR)	—	0.2	3	11	µA	3.0V	
D206	IPD_HLVD	High/Low Voltage Detect (HLVD)	—	9.5	14.8	18	µA	3.0V	
D206	IPD_HLVD	High/Low Voltage Detect (HLVD)	—	9.7	14.2	17	µA	3.0V	
D207	**IPD_ADCA**	**ADC - Converting**	**—**	**0.1**	**2**	**10.5**	**µA**	**3.0V**	**ADC not converting (4)**
D207	IPD_ADCA	ADC - Converting	—	0.1	4	12	µA	3.0V	ADC not converting (4)
D208	IPD_CMP	Comparator	—	33	49	50	µA	3.0V	
D208	IPD_CMP	Comparator	—	30	49	50	µA	3.0V	

† Data in “Typ.” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max. values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode with all I/O pins in high-impedance state and tied to VSS.

3: All peripheral currents listed are on a per-peripheral basis if more than one instance of a peripheral is available.

4: ADC clock source is FRC.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (01/2018)

Initial release of this document.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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